OmniVision™

datasheet

PRODUCT SPECIFICATION

CMOS digital / analog NTSC/PAL image sensor
with OmniPixel3-HS™ technology for security applications

OV7962/OV7461

CMOS digital / analog NTSC/PAL image sensor with OmniPixel3-HS™ technology

datasheet (CSP4)
PRODUCT SPECIFICATION

version 2.31
august 2013

To learn more about OmniVision Technologies, visit www.ovt.com.
OmniVision Technologies is publicly traded on NASDAQ under the symbol OVTI.

applications

- security and surveillance cameras

ordering information

- **OV07962-E62A** (color, lead-free)
  62-pin CSP4
- **OV07461-E62A** (b&w, lead-free)
  62-pin CSP4

features

- parallel DVP interface
- high sensitivity
- automatic exposure/gain with 16 zone control
- horizontal and vertical windowing capability
- auto white balance control
- aperture/gamma correction
- external frame sync capability (Genlock)
- slave compatible serial camera control bus (SCCB) control interface for register programming (SCCB is I2C compatible)
- low power consumption
- extremely low dark current for high temperature applications
- 50/60 Hz flicker cancellation
- overlay with four layers, 16 colors and eight transparencies each
- 16 bytes of one time programmable memory (OTP)
- SPI master for single static overlay and loading setting
- dynamic overlay controls
- video feedback loop
- defective pixel correction

key specifications (typical)

- **active array size:**
  digital: 752 x 480
- **power supply:**
  core: 1.5V ± 5%
  analog: 3.14 ~ 3.47V
  I/O: 1.7 ~ 3.47V
- **power requirements:**
  active: 245 mW
  standby: 20 µA
- **temperature range:**
  operating: -20°C to +70°C junction temperature (see **table 8-2**)
  stable image: 0°C to +50°C junction temperature (see **table 8-2**)
- **optical size:**
  752x480: 1/3.2"
  640x480: 1/4"
- **output formats:** NTSC/PAL, RAW RGB, RGB565, RGB666, YUV422, CCIR656
- **maximum image transfer rate:**
  752x480: 30 frames per second
  640x480: 30 frames per second
  320x240: 60 frames per second
- **sensitivity:** 12 V/Lux-sec
- **shutter:** rolling shutter (see **sidebar note**)
- **max S/N ratio:** 38 dB
- **dynamic range:** 70 dB @ 8x gain
- **scan mode:** interlace
- **pixel size:** 6.0 µm x 6.0 µm
- **dark current:** 50 mV/s @ 60°C junction temperature
- **image area:** 4752 µm x 3552 µm
- **package dimensions:** 6680 µm x 7130 µm

note
Sensors with rolling shutter and high sensitivity can produce images with banding under certain fluorescent lighting conditions.

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1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pin numbers for the OV7962/OV7461 image sensor. The package information is shown in section 9.

table 1-1 signal descriptions (sheet 1 of 3)

pin number	signal name	pin type	description
A1	NC	–	no connect
A2	AVDD	power	3.3V power
A3	AGND	ground	analog ground
A4	VREFH	analog	internal reference
A5	SVDD	power	3.3V power
A6	SGND	ground	sensor array ground
A7	VREFN	reference	internal reference
A8	COLOR/BW	input	color or black and white switch
A9	NC	–	no connect
B1	NC	–	no connect
B2	VREFB	reference	internal reference
B3	VREFD	analog	internal reference
B4	NC	–	no connect
B5	SVDD	power	3.3V power
B6	NC	–	no connect
B7	NC	–	no connect
B8	CS	output	SPI chip select
B9	NC	–	no connect
C1	NC	–	no connect
C2	NC	–	no connect
C8	NC	–	no connect
C9	OVLEN	input	overlay ON/OFF
D1	PWDN	input	power down input (active high with pull down resistor)
D2	PAL/NTSC	input	PAL/NTSC switch
D8	SDA	I/O	SCCB interface data pin

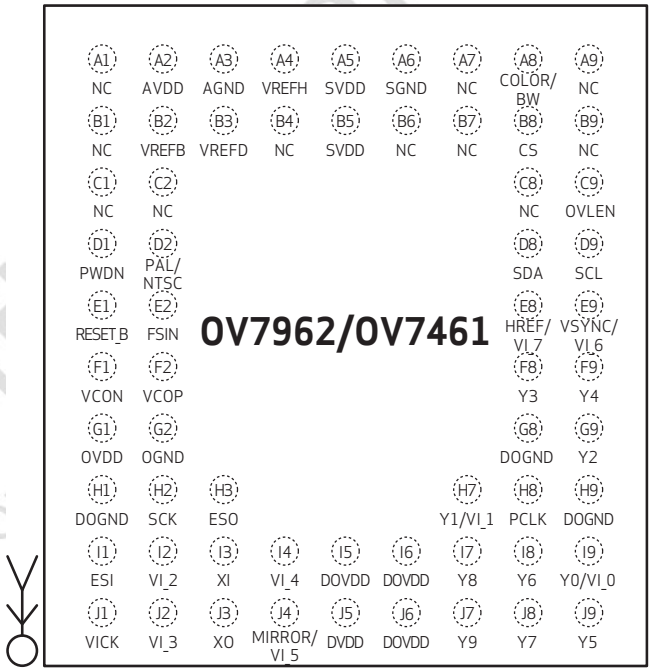
table 1-1 signal descriptions (sheet 2 of 3)

pin number	signal name	pin type	description
D9	SCL	input	SCCB interface input clock
E1	RESET_B	input	reset input (active low with pull up resistor)
E2	FSIN	I/O	frame sync signal
E8	HREF/VI_7	I/O	video output horizontal signal or video data input[7]
E9	VSYNC/VI_6	I/O	video output vertical signal or video data input[6]
F1	VCON	output	composite video output negative
F2	VCOP	output	composite video output positive
F8	Y3	output	video data output[3]
F9	Y4	output	video data output[4]
G1	OVDD	power	3.3V power
G2	OGND	ground	ground
G8	DOGND	ground	digital ground
G9	Y2	output	video data output[2]
H1	DOGND	ground	digital ground
H2	SCK	output	SPI clock
H3	ESO	output	SPI data output
H7	Y1/VI_1	I/O	video data output[1] or video data input[1]
H8	PCLK	I/O	video output clock
H9	DOGND	ground	digital ground
I1	ESI	input	SPI data input
I2	VI_2	I/O	video data input[2]
I3	XI	input	clock input
I4	VI_4	I/O	video data input[4]
I5	DOVDD	power	1.7 ~ 3.47V power
I6	DOVDD	power	1.7 ~ 3.47V power
I7	Y8	output	video data output[8]
I8	Y6	output	video data output[6]
I9	Y0/VI_0	I/O	video data output[0] or video data input[0]
J1	VICK	I/O	video input clock
J2	VI_3	I/O	video data input[3]

table 1-1 signal descriptions (sheet 3 of 3)

pin number	signal name	pin type	description
J3	XO	output	clock output
J4	MIRROR/VI_5	I/O	image mirror control in normal mode/video data input[5] in video feedback mode
J5	DVDD	power	1.5V power
J6	DOVDD	power	1.7 ~ 3.47V power
J7	Y9	output	video data output[9]
J8	Y7	output	video data output[7]
J9	Y5	output	video data output[5]

figure 1-1 pin diagram



top view

2 system level description

2.1 overview

The OV7962 (color) and OV7461 (b&w) image sensors are low voltage, high performance CMOS image analog sensors that provide the full functionality of a single chip digital / analog NTSC/PAL image sensor using OmniPixel3-HS™ technology in a small footprint package. They provide full-frame images via the control of the Serial Camera Control Bus (SCCB) interface.

The OV7962/OV7461 has an image array capable of operating at 30 frames per second in VGA mode. This product is ideal for applications requiring a small footprint, low voltage, low power and low cost color video camera.

2.2 architecture

The OV7962/OV7461 sensor core generates streaming pixel data at a constant frame rate with analog output.

The timing generator outputs clocks to access the rows of the imaging array, precharging and sampling the rows of the array sequentially. In the time between precharging and sampling a row, the charge in the pixels decrease with exposure to incident light. This is the exposure time in rolling shutter architecture.

The exposure time is controlled by adjusting the time interval between pre-charging and sampling. After the data of the pixels in the row has been sampled, it is processed through analog circuitry which corrects for offset and multiplies the data with corresponding gain. Following analog processing is the ADC, which outputs 10-bit data for each pixel in the array.

figure 2-1 OV7962/OV7461 block diagram

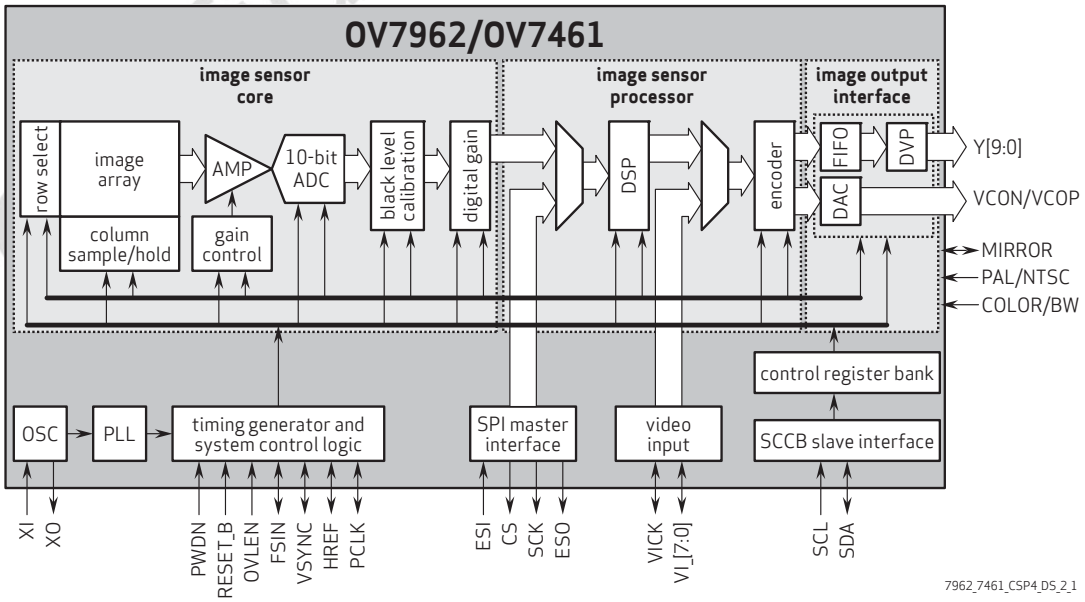
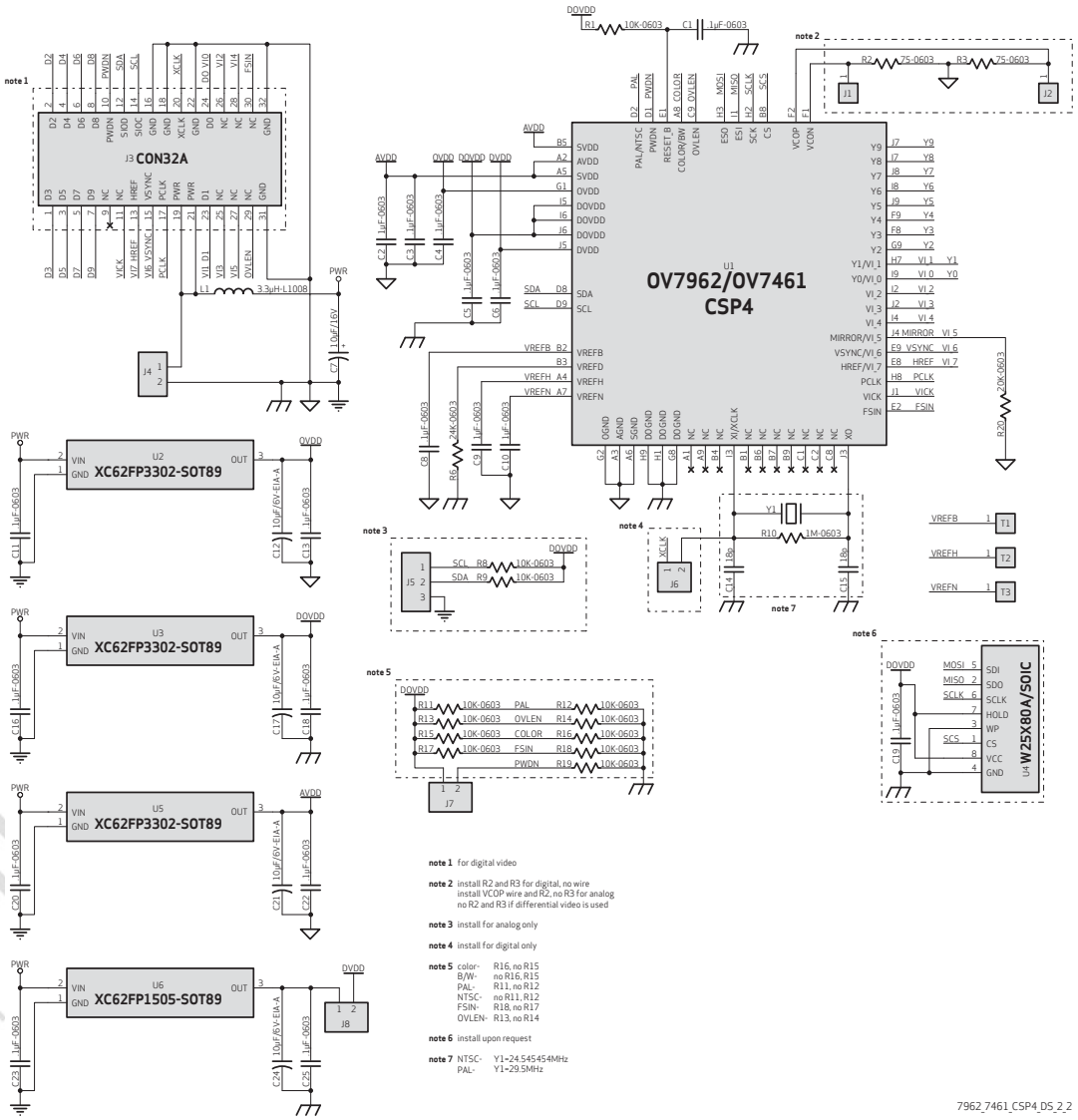


figure 2-2 OV7962/OV7461 reference schematic



2.3 PLL control

The OV7962/OV7461 PLL allows input clock frequencies ranging from 6~27 MHz and has a maximum VCO frequency of 500 MHz. PLLOUT is the input clock for the digital part of the sensor. For NTSC output, the input clock frequency should be 24.545452 MHz. For PAL output, the input clock frequency should be 29.5 MHz.

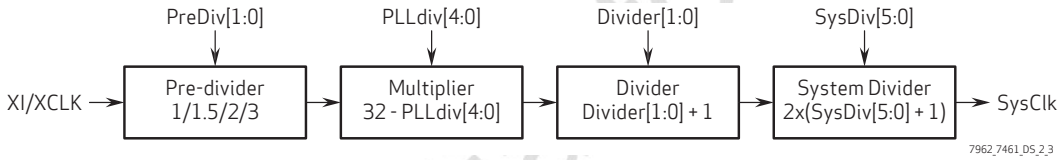
Divider[1:0] (**0x3096**[6:5]) 00 – /1, 01 – /2, 10 – /3, 11 – /4

PreDiv[1:0] (**0x3095**[6:5]) 00 – /1, 01 – /1.5, 10 – /2, 11 – /3

PLLdiv[4:0] (**0x3095**) is the multiplier parameter: multiplier = (32 - PLLdiv)

SysDiv[5:0] (**0x3011**) is the system divider: system divider = 2x(SysDiv[5:0] +1)

figure 2-3 PLL control diagram



2.4 I/O control

The OV7962/OV7461 I/O pad direction and driving capability can be easily adjusted. **table 2-1** lists the driving capability and direction control registers of the I/O pads.

2.4.1 TV output mode (NTSC or PAL)

VCON and VCOP composite video output signals are from DAC.

table 2-1 driving capability and direction control for I/O pads (sheet 1 of 2)

function	register	description
drive capability select for the output pads	0x300E	Bit[1:0]: output drive capability 00: 1x 01: 2x 10: 3x 11: 4x
I/O direction control	0x3093	Bit[7:0]: I/O direction control of Y[9:2] pin 0: Input 1: Output

table 2-1 driving capability and direction control for I/O pads (sheet 2 of 2)

function	register	description
I/O direction control	0x3094	Bit[4]: I/O direction control of HREF/VI_7 pin 0: Input 1: Output Bit[3]: I/O direction control of PCLK pin 0: Input 1: Output Bit[2]: I/O direction control of VSYNC/VI_6 pin 0: Input 1: Output Bit[1:0]: I/O direction control of Y[1:0] / VI_[1:0] 0: Input 1: Output

2.5 system control

2.5.1 external components

An external 3.13 ~ 3.47V power supply is used for array power. Pad power can range from 1.7 to 3.47V. 1.5V core power is converted from pad power by the internal regulator.

The OV7962/OV7461 needs at least three external passive devices to reduce noise. The capacitor value should be at least 0.1µF.

A resistor is required for TV out DAC power reference.

2.5.2 power management

Suspend mode is controlled by the PWDN pin. In suspend mode, the internal clocks are stopped, sensor modules are powered off, and logic control blocks clock input from internal circuitry by logic control. Register values are saved while the sensor is in suspend mode.

Sleep mode can be controlled by register. During sleep mode, the SCCB clock keeps running. Register values can still be accessed while the sensor is in this mode.

In both suspend and sleep modes, the TV output pin state is turned OFF and the 75 ohm termination is connected to GND.

2.5.3 system clock

The on-chip PLL takes 24.545452 MHz (NTSC), 29.5 MHz (PAL) or 6~27 MHz clock signals from an external crystal or oscillator. A clock divider is provided to generate different system frequencies.

2.6 SCCB interface

The Serial Camera Control Bus (SCCB) interface controls the image sensor operation. Refer to the *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for detailed usage of the serial control port.

figure 2-4 data transfer on the SCCB diagram

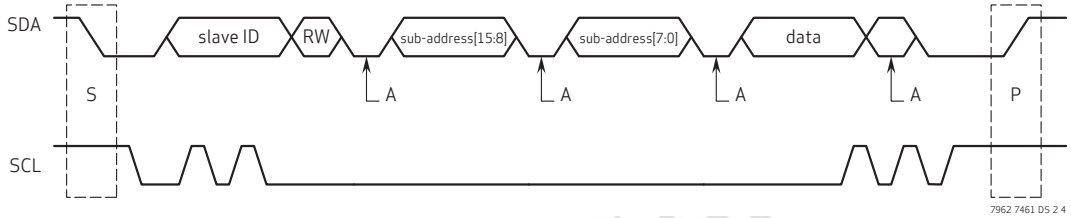


figure 2-5 SCCB protocol format diagram

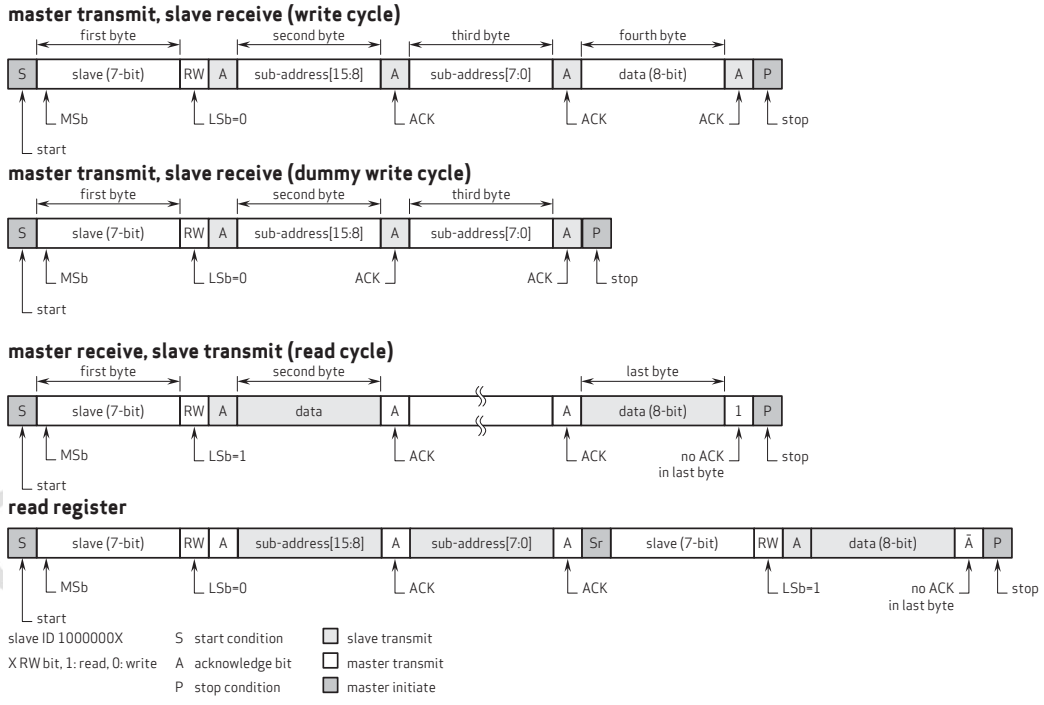


figure 2-6 SCCB timing diagram

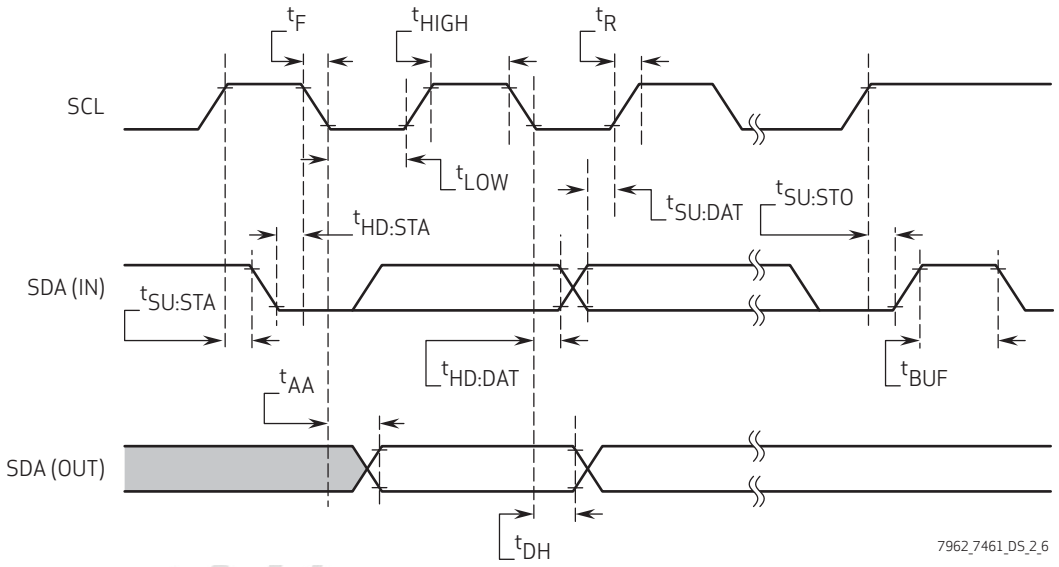
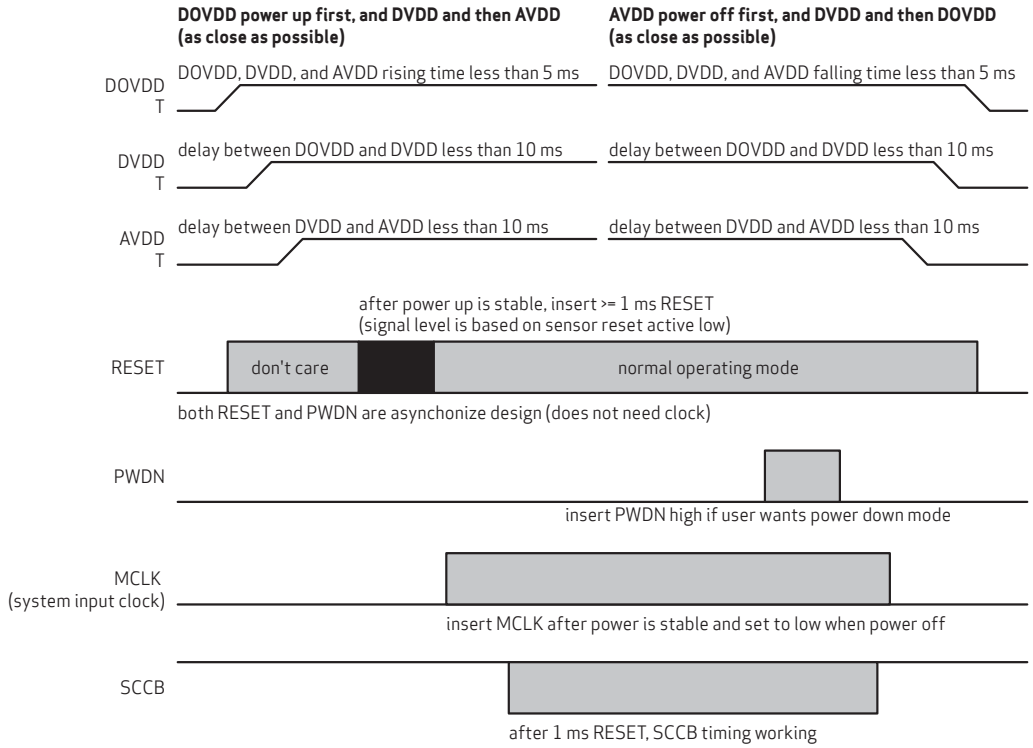


table 2-2 SCCB timing specification

symbol	parameter	min	typ	max	unit
f_{SCL}	clock frequency			400	kHz
t_{LOW}	clock low period	1.3			µs
t_{HIGH}	clock high period	600			ns
t_{AA}	SCL low to data out valid	100		900	ns
t_{BUF}	bus free time before new START	1.3			µs
$t_{HD:STA}$	START condition hold time	600			ns
$t_{SU:STA}$	START condition setup time	600			ns
$t_{HD:DAT}$	data in hold time	0			µs
$t_{SU:DAT}$	data in setup time	100			ns
$t_{SU:STO}$	STOP condition setup time	600			ns
t_R,t_F	SCCB rise/fall times			300	ns
t_{DH}	data out hold time	50			ns

2.7 power up and off sequence

figure 2-7 power up and off sequence diagram



note this is a recommended sequence; when all power supplies are turned on/off within very short period, power supplies sequence can be changed for system design

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2.8 group register write

Control values of multiple registers can be written at the same time by using the group register write function. The procedure is as follows:

1. Set the group write enable bit (register 0x3094[5] = 1)
2. Write register values (up to 16 registers, including the register write, set 0x3094[5] to 0, to disable group write if necessary)
3. Write group write latch register 0x30EE = 0xFF
4. The group of registers are updated at the same time.

To disable this function:

1. Clear the group write enable bit (register 0x3094[5] = 0)
2. Write group write latch register 0x30EE = 0xFF

2.9 hardware and software standby

Two suspend modes are available for the OV7962/OV7461:

- hardware standby
- software standby

To initiate hardware standby mode, the PWDN pin must be tied to high. When this occurs, the OV7962/OV7461 internal device clock is halted and all internal counters are reset and registers are maintained.

Executing a software standby through the SCCB interface suspends internal circuit activity but does not halt the device clock. All register content is maintained in standby mode.

2.10 video feedback mode

- output 8-bit data: Y9,Y8,Y7,Y6,Y5,Y4,Y3,Y2 pins
- output pixel clock: PCLK pin
- input 8-bit data: HERF/VI_7, VSYNC/VI_6, MIRROR/VI_5, VI_4, VI_3, VI_2 Y1/VI_1, Y0/VI_0 pins
- input pixel clock: VICK
- input /output sync: CCIR656

2.11 FSIN

For DVP mode, slave chip FSIN gets VSYNC signal.

table 2-3 FSIN control register

function	register	description
FSIN I/O control	0x3062	Bit[2]: input/output selections of FSIN pin 0: input 1: output

2.11.1 DVP slave mode

- input PCLK: PCLK pin
- input HREF: VSYNC pin
- output 10-bit data: Y9,Y8,Y7,Y6,Y5,Y4,Y3,Y2,Y1,Y0 pins

table 2-4 video feedback mode

function	register	description
video feedback IO control	0x3062	Bit[1]: input/output selections of VICK, VI0, VI1, VI2, VI3 pins 0: input 1: output

2.12 formats

2.12.1 analog formats

table 2-5 analog format and frame rate

function	format	resolution	field rate	input clock
analog output	NTSC	656x492	60 fields/sec	24.545452 MHz
	PAL	768x576	50 fields/sec	29.5 MHz

2.12.2 digital formats

table 2-6 progressive format and frame rate

function	resolution	frame rate	input clock	output clock	
				RAW	YUV422
DVP output	WVGA (752x480)	30 fps	6~29.5 MHz	≥13.5 MHz ≤14.5 MHz	≥27 MHz ≤29 MHz
	VGA (640x480)	30 fps	6~29.5 MHz	≥12 MHz ≤14.5 MHz	≥24 MHz ≤29 MHz
	QVGA (320x240)	60 fps	6~29.5 MHz	≥12 MHz ≤14.5 MHz	≥24 MHz ≤29 MHz

3 block level description

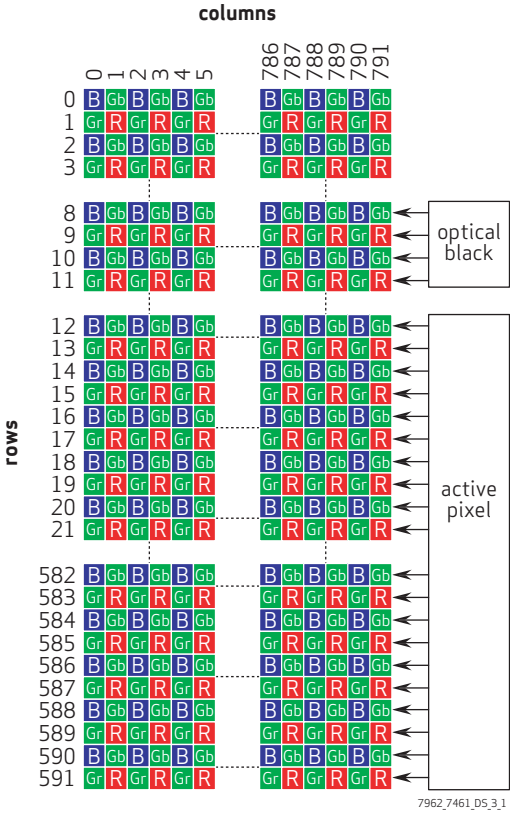
3.1 pixel array structure

The OV7962/OV7461 sensor has an image array of 792 columns by 592 rows (468,864 pixels). **figure 3-1** shows a cross-section of the image sensor array.

The color filters are arranged in a Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 468,864 pixels, 768 x 576 (442,368) are active pixels and can be output. The other pixels are used for black level calibration and interpolation.

The sensor array design is based on a field integration read-out system with line-by-line transfer and an electronic shutter with a synchronous pixel read-out scheme.

figure 3-1 sensor array region color filter layout



4 image sensor core digital functions

4.1 mirror and flip

The OV7962/OV7461 provides mirror mode, which reverses the sensor data read-out order horizontally, and flip mode which reverses it vertically (see **figure 4-1**). In mirror mode, since the Bayer order changes from BGBG... to GBGB..., the read-out sequence will be adjusted automatically when the mirror function is on. In flip mode, the VREF starting line needs to be adjusted, then the ISP block will auto-detect whether the pixel is in red line or blue line and make necessary adjustments. For proper mirror and flip mode operation, please refer to the *OmniVision 7960-62 NTSC Window Application Note*. There are offset registers that must be changed to ensure a centered image.

figure 4-1 mirror and flip samples

original image | mirrored image | flipped image | mirrored and flipped image

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table 4-1 mirror and flip function control

function	register	description
mirror	0x300C	Bit[6]: mirror ON/OFF select 0: mirror OFF 1: mirror ON
flip	0x300C	Bit[7]: flip ON/OFF select 0: flip OFF 1: flip ON

4.2 test pattern

For testing purposes, the OV7962/OV7461 offers one type of test pattern: color bar. There are four color bar modes (see **figure 4-2**). The color bar mode can be set with register 0x5004[1:0]. In each mode, the color bar can be moved from bottom to top if the bar rolling function is enabled by setting register 0x5004[2] to 1. The moving step can be configured by setting the register 0x5051[3:1] (see **table 4-2**).

figure 4-2 test pattern

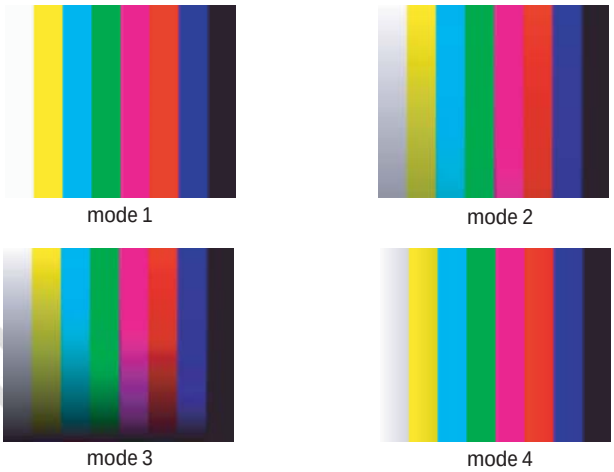


table 4-2 test pattern registers

function	register	description
color bar	0x5003	Bit[0]: color bar enable 0: normal image 1: color bar
color bar pattern select	0x5004	Bit[1:0]: four types of color bar patterns
color bar rolling selection	0x5004	Bit[2]: color bar rolling enable 0: still color bar 1: rolling color bar (from down to up)
color bar rolling step	0x5051	Bit[3:0]: color bar rolling step

4.3 AEC/AGC algorithms

The auto exposure control (AEC) and auto gain control (AGC) allow the image sensor to adjust the image brightness to a desired range by setting the proper exposure time and gain for the image. Besides automatic control, exposure time and gain can be set manually from external control. The related registers are listed in **table 4-3**.

table 4-3 AEC/AGC function controls

function	register	description
AEC enable	0x3013	Bit[0]: AEC enable 0: manual 1: auto
AEC (exposure time)	{0x300F, 0x3010}	0x300F = AEC[15:8] 0x3010 = AEC[7:0]
AGC (gain)	{0x3015[1:0], 0x3000}	0x3015[1:0] = AGC[9:8] 0x3000 = AGC[7:0]
AGC enable	0x3013	Bit[2]: AGC enable 0: manual 1: auto

There are two different algorithms to tell whether the current frame is too bright or too dark and determine if the exposure time/gain should increase or decrease for the next frame. The Histogram algorithm is based on the statistics of the percentage of high/low luminance pixels. The other is based on the weighted average of a frame.

4.3.1 average-based algorithm

The average-based AEC controls image luminance using registers WPT (0x3024) and BPT (0x3025). In average-based mode the value of register WPT (0x3024) indicates the high threshold value, and the value of register BPT (0x3025) indicates the low threshold value. When the target image luminance average value YAVG (0x302F) is within the range specified by registers WPT (0x3024) and BPT (0x3025), the AEC keeps the image exposure. When register YAVG (0x302F) is greater than the value in register WPT (0x3024), the AEC will decrease the image exposure. When register YAVG (0x302F) is less than the value in register BPT (0x3025), the AEC will increase the image exposure. Accordingly, the value in register WPT (0x3024) should be greater than the value in register BPT (0x3025). The gap between the values of WPT (0x3024) and BPT (0x3025) controls the image stability.

The AEC function supports both normal and fast speed selections in order to bring the image exposure into the range set by the values in registers WPT (0x3024) and BPT (0x3025). AEC set to normal mode will allow for single-step increase or decrease in the image exposure to maintain the specified range. A value of 0 in register FASTEN (0x3013[7]) will result in normal speed operation, and a 1 will result in fast speed operation.

Register VPT (0x3026) controls the fast AEC range. If the target image YAVG (0x302F) is greater than VPT[7:4] x 16, AEC will decrease by half the current exposure time. If register YAVG (0x302F) is less than VPT[3:0] x 16, AEC will increase to double the current exposure time.

As shown in **figure 4-3**, the AEC/AGC convergence uses two regions, the inner stable operating region and the outer control zone, which defines the convergence step size change as follows:

outside control zone

step size: 2 × (AEC[15:0])

t_{STEP}: t_{ROW} × (2 × AEC[15:0])

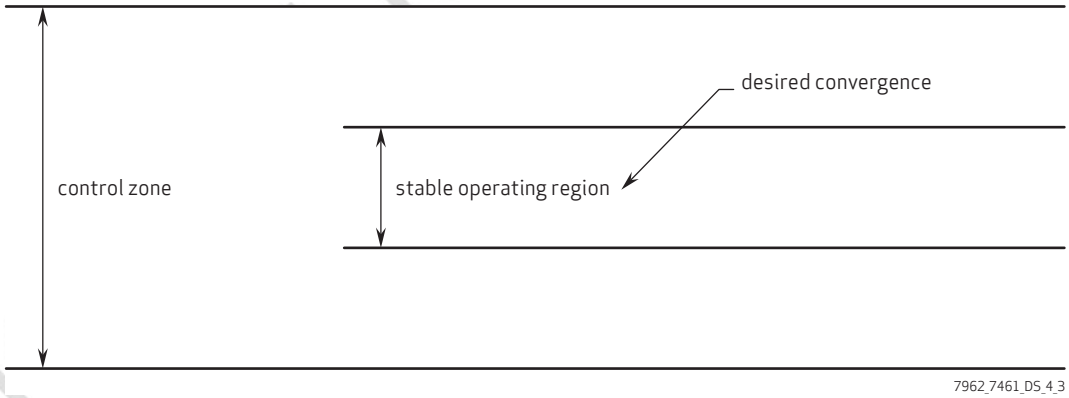
inside control zone

step size: 2 × (AEC[15:0]) ÷ 16)

t_{STEP}: t_{ROW} × (2 × AEC[15:0] ÷ 16)

Once the current value is inside the stable operating region, the AEC/AGC value has converged.

figure 4-3 desired convergence



control zone upper limit: {VPT[7:4] (0x3026[7:4]), 4'b0000}

control zone lower limit: {VPT[3:0] (0x3026[3:0]), 4'b0000}

stable operating region upper limit: WPT[7:0] (0x3024)

stable operating region lower limit: BPT[7:0] (0x3025)

For the average-based AEC/AGC algorithm, the measured window is horizontally and vertically adjustable and divided into sixteen (4 x 4) zones (see **figure 4-4**). Each zone (or block) is 1/16th of the image and has a 4-bit weight in calculating the average luminance (YAVG). The 4-bit weight could be n/16 where n is from 0 to 15. The final YAVG is the weighted average of the sixteen zones. For more details on adjusting horizontal and vertical windows and weight for each window, refer to **section 4.3.3,** average luminance (YAVG).

4.3.2 histogram-based algorithm

The histogram-based AEC controls image luminance using registers LVLB, LVLVB, LVLW, LVLVW, NUMB, NUMVB, NUMW and NUMVW. In histogram-based mode, the registers LVLB, LVLVB, LVLW and LVLVW indicate the luminance level that a pixel is considered dark, very dark, bright, and very bright. NUMB indicates the low threshold value and

NUMW indicates the high threshold value of the statistic. When the number of dark pixels is greater than the value specified by register NUMB, the AEC will increase the image exposure. When the number of bright pixels is greater than the value specified by the register NUMW, the AEC will decrease the image exposure.

The histogram-based algorithm supports both normal and fast speed selection in order to bring the image exposure into the proper level.

If the number of very dark pixels exceeds the value specified by register NUMVB or the number of very bright pixels exceeds the value specified by register NUMVW, AEC will enter the fast mode if FASTEN (0x3013[7]) is set to 1. Otherwise, the histogram-based algorithm works in normal mode.

table 4-4 AEC/AGC histogram algorithms

function	register	description
AEC enable	0x3013	Bit[0]: AEC enable 0: manual 1: auto
AEC (exposure time)	{0x300F, 0x3010}	0x300F = AEC[15:8] 0x3010 = AEC[7:0]
LAEC (less than 1 row exposure time)	{0x301F, 0x3030}	0x301F = LAEC[7:0] 0x3030 = LAEC[15:8]
AGC (gain)	{0x3015[1:0], 0x3000}	0x3015[1:0] = AGC[9:8] 0x3000 = AGC[7:0]
AGC enable	0x3013	Bit[2]: AGC enable 0: manual 1: auto

4.3.3 average luminance (YAVG)

Auto exposure time calculation is based on a frame brightness average value. A 4x4 grid average window is defined. The average value is the weighted average of the 16 sections.

There are two window modes: auto window mode and sub window mode. In auto window mode (default mode), the 4x4 grid average window is defined by input image sizes (HW and VH) of the YAVG module. In the sub window mode (register 0x5690[7] set to 1), the window is defined by AVG_X_START, AVG_X_END, AVG_Y_START and AVG_Y_END registers. **figure 4-4** shows the sizes of definition window. **table 4-5** lists the corresponding registers.

figure 4-4 average-based window definition

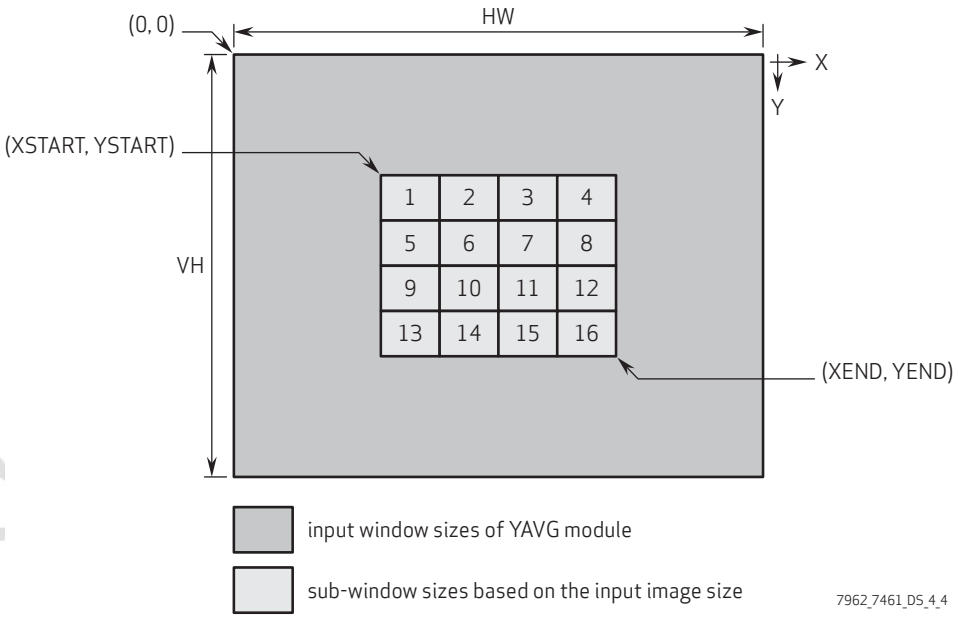


table 4-5 YAVG window and weight registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5680	AVG XSTART	0x00	RW	Bit[3:0]: Avg x start[11:8] Horizontal start position for average window
0x5681	AVG XSTART	0x00	RW	Bit[7:0]: Avg x start[7:0] Horizontal start position for average window
0x5682	AVG XEND	0x08	RW	Bit[3:0]: Avg x end[11:8] Horizontal end position for average window

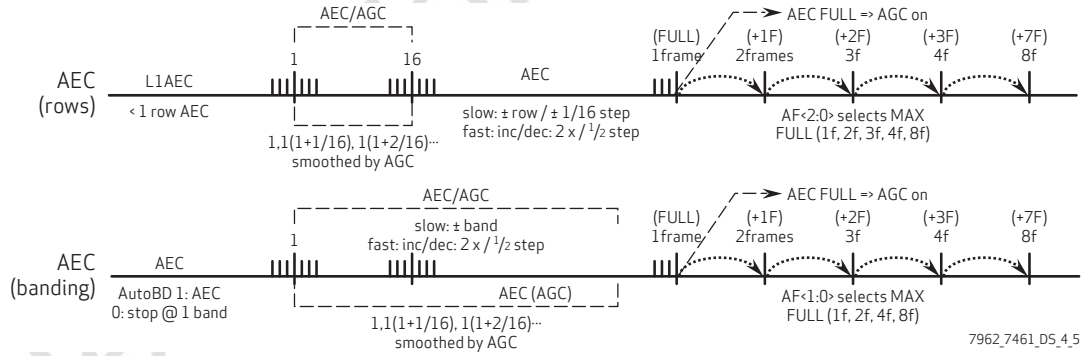
table 4-5 YAVG window and weight registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5683	AVG XEND	0x00	RW	Bit[7:0]: Avg x end[7:0] Horizontal end position for average window
0x5684	AVG YSTART	0x00	RW	Bit[2:0]: Avg y start[10:8] Vertical start position for average window
0x5685	AVG YSTART	0x00	RW	Bit[7:0]: Avg y start[7:0] Vertical start position for average window
0x5686	AVG YEND	0x06	RW	Bit[2:0]: Avg y end[10:8] Vertical end position for average window
0x5687	AVG YEND	0x00	RW	Bit[7:0]: Avg y end[7:0] Vertical end position for average window
0x5688	AVG R8	0xFF	RW	Bit[5:4]: window1_weight Bit[1:0]: window0_weight
0x5689	AVG R9	0xFF	RW	Bit[5:4]: window3_weight Bit[1:0]: window2_weight
0x568A	AVG RA	0xFF	RW	Bit[5:4]: window5_weight Bit[1:0]: window4_weight
0x568B	AVG RB	0xFF	RW	Bit[5:4]: window7_weight Bit[1:0]: window6_weight
0x568C	AVG RC	0xFF	RW	Bit[5:4]: window9_weight Bit[1:0]: window8_weight
0x568D	AVG RD	0xFF	RW	Bit[5:4]: window11_weight Bit[1:0]: window10_weight
0x568E	AVG RE	0xFF	RW	Bit[5:4]: window13_weight Bit[1:0]: window12_weight
0x568F	AVG RF7	0xFF	RW	Bit[5:4]: window15_weight Bit[1:0]: window14_weight

4.4 AEC/AGC steps

figure 4-5 shows how the AEC and AGC work together to obtain adequate exposure/gain based on the current environment's illumination. The upper one illustrates the non-banding operation which time unit is based on Tline. The lower one shows exposure in banding. The x-axis represents the length of exposure in time scale. In normal light circumstances, the length of exposure will fall into a range from 1 Tline to 1 Tframe. In extremely bright or dark circumstances, exposure time less than 1 Tline/Tband or greater than 1 Tframe may be required accordingly. In order to achieve the best signal-to-noise ratio (SNR), extending the exposure time is always preferred to raising the analog gain when the illumination level is decreasing. Similarly, with increasing illumination it is preferred to decrease the gain prior to shortening the exposure time.

figure 4-5 darker and brighter illumination situations



4.4.1 auto exposure control (AEC)

The function of the AEC is to calculate integration time of the next frame and send the information to the timing control block. Based on the statistics of previous frames, the AEC is able to determine whether the integration time should increase, decrease, fast increase, fast decrease, or remain the same.

LAEC activates in extremely bright situations, allowing integration time to be less than one row. In extremely dark situations the VAEC activates, allowing integration time to be larger than one frame.

To avoid image flickering under a periodic light source, the integration time step can be adjusted as an integer multiple of the period of the light source. This new AEC step system is called banding, suggesting that the steps are not continuous but fall within bands.

4.4.1.1 LAEC

If the integration time is only one row but the image is too bright, AEC will enter LAEC mode. Within LAEC, the integration time can be further decreased to a minimum of 1/16 row or so. LAEC ON/OFF can be set in 0x5013[3].

4.4.1.2 banding filter

AC powered light sources usually have a frequency of 60Hz or 50Hz. When the sensor integration time is not an integer multiple to the light frequency, the image will flicker (horizontal banding). When auto detection mode is on,

the banding filter will automatically detect current light frequency and provide a rolling horizontal band eliminate function in auto exposure mode. The banding filter is deployed to filter out the banding effect caused by the 50/60 Hz lighting.

For a given operating frequency, band step can be expressed in terms of row timing.

In a 50Hz or 60Hz light flicker situation the exposure time must be a multiple of the flicker interval to avoid a band showing up on the image. For 50Hz light, the exposure time must be:

$t_{Exposure} = N \div 100$

For 60Hz light, the exposure time must be:

$t_{Exposure} = N \div 120$

where N is positive integer.

Since the exposure time, AEC[15:0], is based on row interval, it needs to be preset on how many rows is equal to 1/100 second and 1/120 second. Banding filter registers BD50ST and BD60ST, are used to set the number of rows of 1/100 and 1/120 second respectively. The banding filter can be calculated by:

BD60ST, 60Hz banding filter value $= 1 \div (120 \times t_{row}$ interval)

$=$ (frame rate $\times$ maximum exposure) $\div 120$

BD50ST, 50Hz banding filter value $= 1 \div (100 \times t_{row}$ interval)

$=$ (frame rate $\times$ maximum exposure) $\div 100$

where maximum exposure equals the number of line per frame, plus the number of dummy lines.

The band steps for 50Hz and 60Hz light sources can be set in registers 0x3052, 0x3054, and 0x3055.

Under strong brightness conditions, there is an option to allow the exposure time to go below the minimum banding filter value (1/120 or 1/100) to prevent overexposure. When the option is ON, if the next integration time is less than the minimum band step, banding will automatically turn OFF. It will turn ON again when the next integration time becomes larger than the minimum band. If this option is disabled, the minimum integration time is one minimal band. The option can be set in register 0x3013[4].

4.4.1.2 automatic 50/60Hz banding detection

The OV7962/OV7461 supports automatic 50/60Hz banding detection function; current light frequency will be detected, and the exposure time will be automatically adjusted.

The auto mode can be enabled by setting 0x30EC[7].

4.4.1.3 banding mode OFF with AEC

When banding is OFF, integration time increases/decreases by 1/16 of the previous step in slow mode, or becomes twice/half of the previous step in fast mode.

4.4.1.4 VAEC

In extremely dark situations, the integration time must be longer than one frame.

The OV7962/OV7461 supports long integration time such as 1 frame, 2 frames, 3 frames and 7 frames. This is achieved by slowing down original frame rate and waiting for exposure. VAEC ceiling can be set in register 0x3015[6:4]. VAEC can be disabled by setting register 0x3015[7] to 0.

table 4-6 AEC and banding filter registers

function	register	description
LAEC ON/OFF	0x3013	Bit[3]: LAEC ON/OFF select 0: OFF 1: ON
banding filter enable	0x3013	Bit[5]: banding filter enable 0: disable banding filter 1: enable banding filter
banding filter option	0x3013	Bit[4]: below banding step value enable 0: limit the minimum exposure time to 1/100 or 1/120 seconds under any light conditions when banding filter is enabled 1: allow exposure time to be less than 1/100 or 1/120 seconds under strong light conditions when banding filter is enabled
banding filter mode	0x30EC	Bit[7]: banding filter mode, effective when banding filter is enabled 0: manual mode 1: auto mode
banding filter manual mode	0x30EC	Bit[6]: light source frequency manual selection 0: 60Hz 1: 50Hz
banding filter step value (60Hz)	{0x3052, 0x3055}	banding filter step value for 60Hz light source (10 bits) 0x3052[7:6]: MSBs 0x3055[7:0]: LSBs
banding filter step value (50Hz)	{0x3052, 0x3054}	banding filter step value for 50Hz light source (10 bits) 0x3052[5:4]: MSBs 0x3054[7:0]: LSBs
maximum banding filter step (60Hz)	{0x3020, 0x3021}	banding filter maximum allowable number of steps for 60Hz light source (5 bits) 0x3020[7]: MSB 0x3021[3:0]: LSBs
maximum banding filter step (50 Hz)	{0x3020, 0x3021}	banding filter maximum allowable number of steps for 50Hz light source (5 bits) 0x3020[6]: MSB 0x3021[7:4]: LSBs

4.4.2 auto gain control (AGC)

Unlike prolonging integration time, increasing gain will amplify both signal and noise between two gaps of banding exposure time. Thus, AGC usually starts after AEC is full. However, in same cases where adjacent AEC step changes are too large (>1/16), AGC step should be inserted in between; otherwise, the integration time will keep switching from two adjacent steps and the image flickers.

4.4.2.1 integration time between 1~16 rows

When integration time is less than 16 rows, the changes between adjacent AEC steps are larger than 1/16, which may possibly make the image oscillate between two AEC levels; thus, some AGC steps are added in between. For example, from AEC = 2 rows to AEC = 3 rows, there are 7 more AGC steps (1+ x/16, x=1~7) inserted, which ensures every step change is less than 1/16.

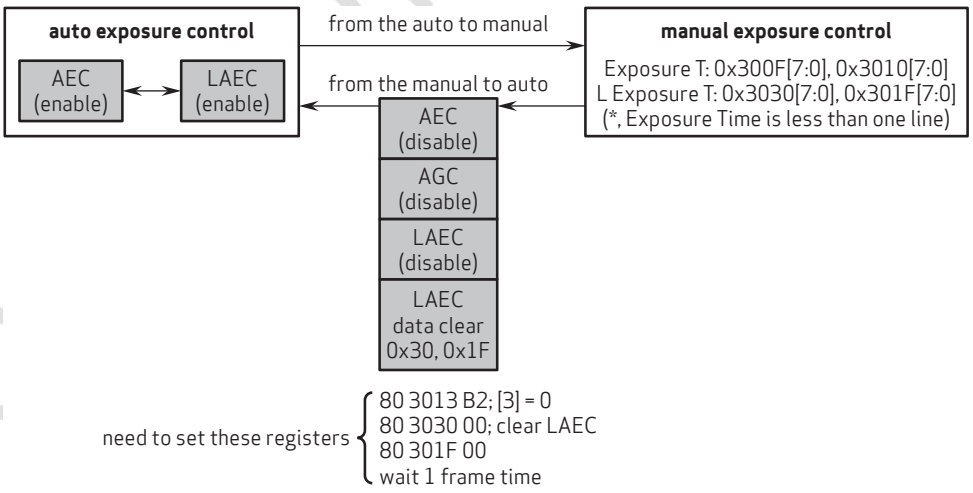
4.4.2.2 gain insertion between AEC banding steps

In banding ON mode, the minimum integration time change is the period of light intensity (10ms for 50Hz, 16.67ms for 60Hz). For the first 16 band steps, since the change between adjacent steps is larger than 1/16, AGC steps are inserted to ensure image stability.

4.4.2.3 gain insertion between VAEC steps

Between VAEC steps (e.g., integration time = 1 frame and 2 frames), AGC steps are inserted to ensure no adjacent step change is larger than 1/16 (6.25%).

figure 4-6 auto exposure and manual exposure control



note there are two exposure control mechanisms in the OV7962/OV7461; one is AEC by row timing and the other is LAEC by sub-row timing. Normally, AEC is used. If the environment is bright enough, it will trigger the sensor into sub-row exposure to enter LAEC status. The OV7962/OV7461 will either be in AEC mode or LAEC mode. The OV7962/OV7461 cannot work under both control loops at the same time. Before changing exposure control from manual to auto, please clear register 0x3030 and 0x301F to 0x00.

7962_7461_CSP4_DS_4_6

4.5 black level calibration (BLC)

The pixel array contains six optically shielded (black) rows. These rows are used to provide the data for offset cancellation algorithms (black level calibration).

Digital image processing starts with black level subtraction. The BLC algorithm estimates the offset of the black level from the data provided by black rows. These offsets of different color channels will be subtracted from values of the color pixels. If the subtraction produces a negative result for a particular pixel, the value of this pixel is set to 0. By default, BLC will be triggered when gain changes.

table 4-7 BLC control functions

function	register	description
target	0x3067	Bit[3:0]: 8-bit target black level value that is used in the algorithm. For 10-bit data, the target is {0x3067[3:0],0,0}
BLC_B, BLC_R	0x300E	Bit[6:5]: BLC_B, BLC_R 00: use all 4 channel offsets 01: use R/Gr channel offset for all channels 10: use B/Gb channel offset for all channels 11: use all 4 channel offsets
BLC always ON	0x3008	Bit[2]: BLC offsets be adjusted every frame
MBLC	0x3008	Bit[3]: trigger BLC manually for 64 frames
R offset	{0x309D[7:6], 0x309C}	BLC offset for R channel
B offset	{0x309D[5:4], 0x309B}	BLC offset for B channel
Gr offset	{0x309D[3:2], 0x309A}	BLC offset for Gr channel
Gb offset	{0x309D[1:0], 0x3099}	BLC offset for Gb channel

4.6 digital gain

After black level subtraction, an optional digital gain can apply a multiplication to all pixel values. By default, the sensor will use analog gain up to its maximum before applying digital gain to the pixels.

table 4-8 digital gain control functions

function	register	description
DGAIN	0x3015	Bit[1:0]: digital gain 00: 1x digital gain 01: 2x digital gain 10: 2x digital gain 11: 4x digital gain

4.7 one-time programmable (OTP) memory

The OV7962/OV7461 has a one-time programmable (OTP) memory to store chip identification and manufacturing information. This OTP memory is organized as 128-bit by 1 one-time programmable electrical fuse with random access interface. The main function is to store chip identification and manufacturing information.

The OTP has three operation modes: program (PGM), READ, and inactive. Normally, it is in inactive mode. By setting 0x30EF to 0xAA, it enters program mode, which will sequentially burn data into the OTP macro. By setting 0x30EF to 0x55, the OTP enters read mode, which will load the OTP data into registers. **table 4-9** summarizes the corresponding registers.

table 4-9 OTP registers

function	register	description
OTP program data	0x30F0~0x30FF	data to be programmed/read into/from OTP memory
OTP program/read enable	0x30EF	0x55: read OTP memory 0xAA: program OTP memory

5 image sensor processor digital functions

5.1 DSP_top

The main purposes of DSP_top are:

- integrate all sub-modules
- create necessary control signals

table 5-1 DSP top registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0x4F	RW	ISP Control 00 Bit[7]: LENC correction enable 0: Disable 1: Enable Bit[6]: Gamma (in YUV domain) enable 0: Disable 1: Enable Bit[5]: RAW gamma enable 0: Disable 1: Enable Bit[4]: Debug control Changing this value is not recommended Bit[3]: De-noise enable 0: Disable 1: Enable Bit[2]: Black pixel cancellation enable 0: Disable 1: Enable Bit[1]: White pixel cancellation enable 0: Disable 1: Enable Bit[0]: Color interpolation (CIP) enable 0: Disable 1: Enable

table 5-1 DSP top registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x5001	ISP CTRL01	0x4F	RW	ISP Control 01 Bit[7]: Special digital effects (SDE) enable 0: Disable 1: Enable Bit[6]: Auto color saturation adjust enable 0: Disable 1: Enable Bit[5]: Vertical scaling enable 0: Disable 1: Enable Bit[4]: Horizontal scaling enable 0: Disable 1: Enable Bit[3]: Auto contrast enable 0: Disable 1: Enable Bit[2]: UV average enable 0: Disable 1: Enable Bit[1]: Color matrix enable 0: Disable 1: Enable Bit[0]: Auto white balance (AWB) enable 0: Disable 1: Enable
0x5003	ISP CTRL03	0x08	RW	ISP Control 03 Bit[7]: Pad in buffer control enable 0: Buffer control boundary padded external 1: Buffer control pad boundary internal Bit[3]: YUV to YCbCr enable 0: Disable 1: Enable Bit[0]: Color bar test pattern enable 0: Disable 1: Enable
0x5004	ISP CTRL04	0x00	RW	ISP Control 04 Bit[2]: Bar move enable 0: Disable 1: Enable Bit[1:0]: Color bar style

table 5-1 DSP top registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x5005	ISP CTRL05	0xDC	RW	ISP Control 05 Bit[7]: Raw gamma option 1 0: Does not add back BLC bias after raw gamma correction 1: Adds back BLC bias after raw gamma correction Bit[6]: Raw gamma option 2 0: Raw gamma applied on input data directly regardless of the black level 1: Subtract black level before applying raw gamma Bit[5]: UV average old style enable 0: Disable 1: Enable Bit[4]: Advanced AWB option 1 0: Do not subtract black level 1: Subtract black level before statistics and apply gain Bit[3]: Lens correction option 1 0: Does not add back BLC bias after lens correction 1: Adds back BLC bias after lens correction Bit[2]: Lens correction option 2 0: Lens correction applied on input data directly regardless of the black level 1: Subtract black level before applying lens correction
0x5024	ISP CTRL36	0x80	RW	ISP Control 36 Bit[6]: Rgma manual mode 0: Use internal divider result for SLPH 1: Use register for SLPH
0x5040	ISP CTRL64	0x00	RW	Bit[7:0]: isp_sccb_offset
0x5041	ISP CTRL65	0x16	RW	Bit[5]: bcc_en Bit[4]: yavg_en Bit[2]: isp_en Bit[1]: yclp_en

table 5-1 DSP top registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x5042	ISP CTRL66	0x03	RW	Bit[7]: old_lenc_mode Bit[3]: out_size_mode Bit[1:0]: yavg_source
0x5043	ISP CTRL67	0x00	RW	Bit[2]: gma_off_man_en Bit[1]: awb_off_man_en Bit[0]: lenc_off_man_en
0x5044	ISP CTRL68	0x00	RW	Bit[7:0]: sensor_bias_man
0x5045	ISP CTRL69	0x00	RW	Bit[3]: interlace_man Bit[2]: interlace_man_en Bit[1]: bw_man Bit[0]: bw_man_en
0x5046	ISP CTRL70	0x30	RW	Bit[7]: dpc_h_swap Bit[5:0]: color_noise_alpha
0x5047	ISP CTRL71	0x01	RW	Bit[0]: cont_cip_sync
0x5048	ISP CTRL72	0x00	RW	Bit[7:4]: lenc_ystart_adj Bit[3:0]: lenc_xstart_adj
0x5003	ISP CTRL03	0x08	RW	Bit[0]: Color bar test pattern enable 0: Disable 1: Enable
0x5004	ISP CTRL04	0x00	RW	ISP Control 04 Bit[2]: Bar move enable 0: Disable 1: Enable Bit[1:0]: Color bar style
0x5051	BAR STEP	0x00	RW	Bit[3:0]: bar_step

5.2 sync

The sync module merges two data paths into one data path to the ISP.

table 5-2 SYNC registers

address	register name	default value	R/W	description
0x5050	SYNC CTRL00	0x00	RW	Bit[3]: rblue_rvs Bit[2]: first_pix_rmv Bit[1]: second_edge Bit[0]: neg_edge

5.3 lens correction (LENC)

The lens correction (LENC) algorithm compensates for the illumination drop off in the corners due to the lens. Based on the radius of each pixel to the lens, the algorithm calculates a gain for each pixel and then corrects each pixel with the calculated gain to compensate for the light distribution due to the lens curvature.

table 5-3 LENC registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	1'b1	RW	Bit[7]: LENC correction enable 0: Disable 1: Enable
0x5005	ISP CTRL05	1'b1 1'b1	RW	Bit[3]: Lens correction option 1 0: Does not add back BLC bias after lens correction 1: Adds back BLC bias after lens correction Bit[2]: Lens correction option 2 0: Lens correction applied on input data directly regardless of the black level 1: Subtract black level before applying lens correction
0x5042	ISP CTRL66	1'b0	RW	Bit[7]: old_lenc_mode
0x5043	ISP CTRL67	1'b0	RW	Bit[0]: lenc_off_man_en
0x5048	ISP CTRL72	0x00	RW	Bit[7:4]: lenc_ystart_adj Bit[3:0]: lenc_xstart_adj
0x5100	LENC RED X0	0x04	RW	Bit[1:0]: red_x0[9:8] X coordinate of the lens optical center for red channel relative to the left-top corner of the ISP input image. Range is 0 ~ 2047
0x5101	LENC RED X0	0x0C	RW	Bit[7:0]: red_x0[7:0] X coordinate of the lens optical center for red channel relative to the left-top corner of the ISP input image. Range is 0 ~ 2047

table 5-3 LENC registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x5102	LENC RED Y0	0x03	RW	Bit[1:0]: red_y0[9:8] Y coordinate of the lens optical center for red channel relative to the left-top corner of the ISP input image. Range is 0 ~ 1535
0x5103	LENC RED Y0	0x06	RW	Bit[7:0]: red_y0[7:0] Y coordinate of the lens optical center for red channel relative to the left-top corner of the ISP input image. Range is 0 ~ 1535
0x5104	LENC RED A1	0x22	RW	LENC Control 04 Bit[6:0]: red_a1[6:0] Composed of the first group of factors used in the LENC correction of the red color channels
0x5105	LENC RED A2	0x07	RW	LENC Control 05 Bit[3:0]: red_a2[3:0] Composed of the first group of factors used in the LENC correction of the red color channels
0x5106	LENC RED B1	0xC2	RW	LENC Control 06 Bit[7:0]: red_b1[7:0] Composed of the second group of factors used in the LENC correction of the red color channels
0x5107	LENC RED B2	0x08	RW	LENC Control 07 Bit[3:0]: red_b2[3:0] Composed of the second group of factors used in the LENC correction of the red color channels
0x5108	LENC GRN X0	0x04	RW	Bit[1:0]: green_x0[9:8] X coordinate of the lens optical center for green channel relative to the left-top corner of the ISP input image. Range is 0 ~ 2047

table 5-3 LENC registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x5109	LENC GRN X0	0x0C	RW	Bit[7:0]: green_x0[7:0] X coordinate of the lens optical center for green channel relative to the left-top corner of the ISP input image. Range is 0 ~ 2047
0x510A	LENC GRN Y0	0x03	RW	Bit[1:0]: green_y0[9:8] Y coordinate of the lens optical center for green channel relative to the left-top corner of the ISP input image. Range is 0 ~ 1535
0x510B	LENC GRN Y0	0x06	RW	Bit[7:0]: green_y0[7:0] Y coordinate of the lens optical center for green channel relative to the left-top corner of the ISP input image. Range is 0 ~ 1535
0x510C	LENC GRN A1	0x22	RW	LENC Control 12 Bit[6:0]: green_a1[6:0] Composed of the first group of factors used in the LENC correction of the green color channels
0x510D	LENC GRN A2	0x07	RW	LENC Control 13 Bit[3:0]: green_a2[3:0] Composed of the first group of factors used in the LENC correction of the green color channels
0x510E	LENC GRN B1	0xC2	RW	LENC Control 14 Bit[7:0]: green_b1[7:0] Composed of the second group of factors used in the LENC correction of the green color channels
0x510F	LENC GRN B2	0x08	RW	LENC Control 15 Bit[3:0]: green_b2[3:0] Composed of the second group of factors used in the LENC correction of the green color channels

table 5-3 LENC registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x5110	LENC BLU X0	0x04	RW	Bit[1:0]: blue_x0[9:8] X coordinate of the lens optical center for blue channel relative to the left-top corner of the ISP input image. Range is 0 ~ 2047
0x5111	LENC BLU X0	0x0C	RW	Bit[7:0]: blue_x0[7:0] X coordinate of the lens optical center for blue channel relative to the left-top corner of the ISP input image. Range is 0 ~ 2047
0x5112	LENC BLU Y0	0x03	RW	Bit[3:0]: blue_y0[11:8] Y coordinate of the lens optical center for blue channel relative to the left-top corner of the ISP input image. Range is 0 ~ 1535
0x5113	LENC BLU Y0	0x06	RW	Bit[7:0]: blue_y0[7:0] Y coordinate of the lens optical center for blue channel relative to the left-top corner of the ISP input image. Range is 0 ~ 1535
0x5114	LENC BLU A1	0x22	RW	LENC Control 20 Bit[6:0]: blue_a1[6:0] Composed of the first group of factors used in the LENC correction of the blue color channels
0x5115	LENC BLU A2	0x07	RW	LENC Control 21 Bit[3:0]: blue_a2[3:0] Composed of the first group of factors used in the LENC correction of the blue color channels
0x5116	LENC BLU B1	0xC2	RW	LENC Control 22 Bit[7:0]: blue_b1[7:0] Composed of the second group of factors used in the LENC correction of the blue color channels

table 5-3 LENC registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x5117	LENC BLU B2	0x08	RW	LENC Control 23 Bit[3:0]: blue_b2[3:0] Composed of the second group of factors used in the LENC correction of the blue color channels
0x5118	LENC XSTART	0x00	RW	Bit[1:0]: X coordinate of the lens starting point[9:8]
0x5119	LENC XSTART	0x00	RW	Bit[7:0]: X coordinate of the lens starting point[7:0]
0x511A	LENC YSTART	0x00	RW	Bit[1:0]: Y coordinate of the lens starting point[9:8]
0x511B	LENC YSTART	0x00	RW	Bit[7:0]: Y coordinate of the lens starting point[7:0]
0x511C	LENC CTRL24	0x80	RW	LENC Control 24 Bit[7]: round_en Determines whether or not to round off the last two bits of the LENC input data 0: Do not round off the last two bits 1: Round off the last two bits Changing this value is not allowed Bit[5]: skip_man_en 0: Use skip signals from system 1: Manually set skip signals by register 0x511C[3:0] Bit[4]: start_man_en 0: Start signal from system 1: Manually start set in register 0x5118~0x5116 Bit[3:2]: h_skip_man Bit[1:0]: v_skip_man

5.4 raw gamma (RGMA)

The main purpose of the raw gamma (RGMA) function is to compensate for the non-linear characteristics of the sensor. GMA converts the pixel values according to the Gamma curve to compensate the sensor output under different light strengths. The non-linear gamma curve is approximately constructed with different linear functions. RAWGAMMA compensates the image in the RAW domain and shares the curve parameters with YUVGAM to save registers. RAWGAMMA should be turned OFF when YUVGAM is ON.

table 5-4 RGMA registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	1'b0	RW	Bit[5]: RAW gamma enable 0: Disable 1: Enable
0x5005	ISP CTRL05	1'b1 1'b1	RW	Bit[7]: Raw gamma option 1 0: Does not add back BLC bias after raw gamma correction 1: Adds back BLC bias after raw gamma correction Bit[6]: Raw gamma option 2 0: Raw gamma applied on input data directly regardless of the black level 1: Subtract black level before applying raw gamma
0x5024	ISP CONTROL 36	0x80	RW	ISP Control 36 Bit[6]: Rgma manual mode 0: Use internal divider result for SLPH 1: Use register for SLPH
0x5043	ISP CTRL67	1'b0	RW	Bit[2]: gma_off_man_en
0x5480	GAMMA CTRL00	0x12	RW	Bit[7:0]: y_list_00 Output at 0x10 (10-bit scale) when register 0x5000[5] = 1
0x5481	GAMMA CTRL01	0x1D	RW	Bit[7:0]: y_list_01 Output at 0x20 (10-bit scale) when register 0x5000[5] = 1
0x5482	GAMMA CTRL02	0x2B	RW	Bit[7:0]: y_list_02 Output at 0x40 (10-bit scale) when register 0x5000[5] = 1

table 5-4 RGMA registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5483	GAMMA CTRL03	0x40	RW	Bit[7:0]: y_list_03 Output at 0x80 (10-bit scale) when register 0x5000[5] = 1
0x5484	GAMMA CTRL04	0x49	RW	Bit[7:0]: y_list_04 Output at 0xA0 (10-bit scale) when register 0x5000[5] = 1
0x5485	GAMMA CTRL05	0x51	RW	Bit[7:0]: y_list_05 Output at 0xC0 (10-bit scale) when register 0x5000[5] = 1
0x5486	GAMMA CTRL06	0x59	RW	Bit[7:0]: y_list_06 Output at 0xE0 (10-bit scale) when register 0x5000[5] = 1
0x5487	GAMMA CTRL07	0x62	RW	Bit[7:0]: y_list_07 Output at 0x100 (10-bit scale) when register 0x5000[5] = 1
0x5488	GAMMA CTRL08	0x6A	RW	Bit[7:0]: y_list_08 Output at 0x120 (10-bit scale) when register 0x5000[5] = 1
0x5489	GAMMA CTRL09	0x73	RW	Bit[7:0]: y_list_09 Output at 0x140 (10-bit scale) when register 0x5000[5] = 1
0x548A	GAMMA CTRL0A	0x88	RW	Bit[7:0]: y_list_10 Output at 0x180 (10-bit scale) when register 0x5000[5] = 1
0x548B	GAMMA CTRL0B	0xA0	RW	Bit[7:0]: y_list_11 Output at 0x1C0 (10-bit scale) when register 0x5000[5] = 1
0x548C	GAMMA CTRL0C	0xCA	RW	Bit[7:0]: y_list_12 Output at 0x240 (10-bit scale) when register 0x5000[5] = 1
0x548D	GAMMA CTRL0D	0xE0	RW	Bit[7:0]: y_list_13 Output at 0x2C0 (10-bit scale) when register 0x5000[5] = 1
0x548E	GAMMA CTRL0E	0xEA	RW	Bit[7:0]: y_list_14 Output at 0x340 (10-bit scale) when register 0x5000[5] = 1
0x548F	GAMMA CTRL0F	0x0F	RW	Bit[7:0]: y_list_15 Slope in range of (0x341, 0x3FF) which should be 2 x (255 - register 0x548E) / 3

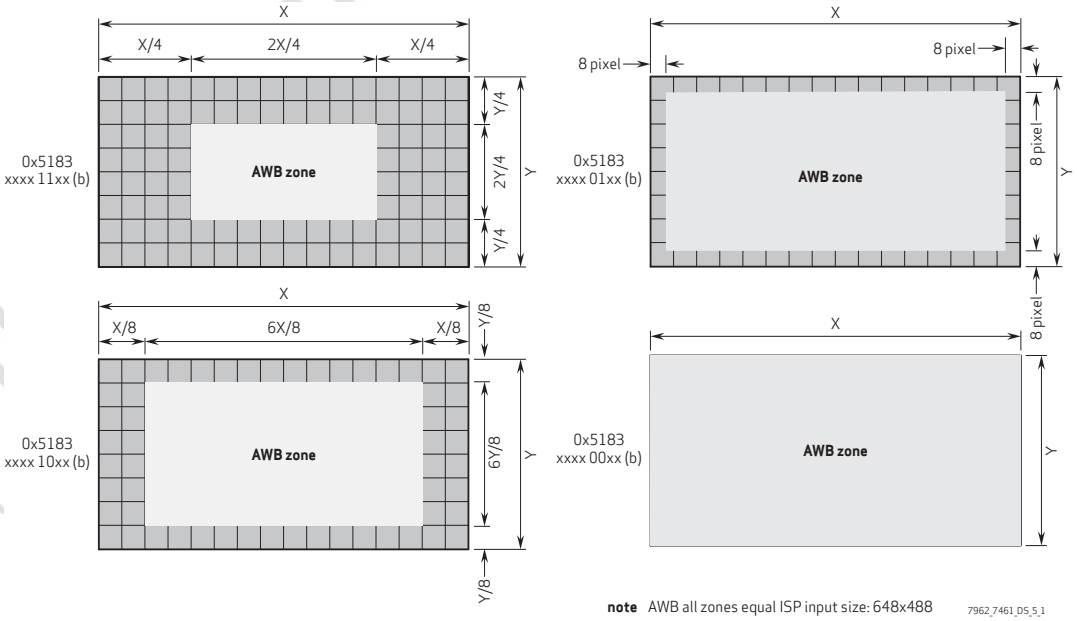
5.5 auto white balance (AWB)

The purpose of the auto white balance (AWB) block is to avoid unrealistic colors so that objects that appear white to the human eye are rendered white in the final image or video. Thus, the AWB makes sure that white is consistent with different color temperatures. This image sensor supports both manual white balance and auto white balance. There are both simple and advanced AWB methods available. Advanced AWB takes into account the color temperature of the light source, which relates to the relative warmth or coolness of white light.

5.5.1 AWB region of interest

Both simple and advanced AWB calculations are based on data from the color pixels. By default, all imaging pixels in the array are used for this calculation. However, there may be applications where it is advantageous to ignore pixels around the periphery of the imager. Those applications include those with large FOV lenses (180 degrees, for example) or with a known object in the FOV, like a car bumper, that should be ignored. In those cases, a smaller region of interest (ROI) can be selected within the imager for the AWB calculations.

figure 5-1 AWB region of interest diagram



note AWB all zones equal ISP input size: 648x488

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table 5-5 AWB registers

address	register name	default value	R/W	description
0x5001	ISP CTRL01	1'b1	RW	Bit[0]: Auto white balance (AWB) enable 0: Disable 1: Enable
0x5005	ISP CTRL05	1'b1	RW	Bit[4]: Advanced AWB option 1 0: Do not subtract black level 1: Subtract black level before statistics and apply gain
0x5043	ISP CTRL67	1'b0	RW	Bit[1]: awb_off_man_en
0x5180	AWB BBLOCK	0xFF	RW	Bit[7:0]: awb_b_block
0x5181	AWB CTRL00	0x58	RW	Bit[7:6]: step_local Bit[5:4]: step_fast Bit[3]: slop_8x Bit[2]: slop_4x Bit[1]: one_zone Bit[0]: avg_all
0x5182	AWB CTRL01	0x11	RW	Bit[7:4]: max_local_cnt Bit[3:0]: max_fast_cnt
0x5183	AWB CTRL02	0x90	RW	Bit[7:4]: Reserved Bit[3:2]: awb_win AWB ROI registers Bit[1:0]: Reserved

5.6 defective pixel cancellation (DPC)

Primarily due to process anomalies, pixel defects in the sensor array will occur, generating incorrect pixel levels and color values. The purpose of the DPC is to remove the effects caused by these defective pixels. Also, some special functions are available for those pixels located at the image boundary. To remove the white/black pixels effectively, the proper threshold levels should first be determined.

table 5-6 DPC registers

address	register name	default value	R/W	description
0x5000	ISP CTRL00	1'b1 1'b1	RW	Bit[2]: Black pixel cancellation enable 0: Disable 1: Enable Bit[1]: White pixel cancellation enable 0: Disable 1: Enable
0x5045	ISP CTRL69	1'b0 1'b0	RW	Bit[1]: bw_man Bit[0]: bw_man_en
0x5046	ISP CTRL70	1'b0	RW	Bit[7]: dpc_h_swap
0x5280	DPC CTRL00	0x7B	RW	Bit[6]: detail_en 0: Disable detail detection method 1: Enable detail detection method Bit[5:4]: bd_sel[1:0] Boundary select options Bit[3]: man_en 0: Disable manual mode 1: Enable manual mode Bit[2]: smooth_en Enable using average G values when doing recovery Bit[1]: dc_en 0: Disable different channel detection 1: Enable different channel detection Bit[0]: sc_en 0: Disable same channel detection 1: Enable same channel detection

5.7 de-noise (DNS)

Noise in digital images is most visible in uniform surfaces, and increases with temperature, sensitivity and decreasing pixel size.The main purpose of the DNS function is to decrease this noise.

table 5-7 DNS registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	1'b1	RW	Bit[3]: De-noise enable 0: Disable 1: Enable
0x5046	ISP CTRL70	0x30	RW	Bit[5:0]: color_noise_alpha
0x5290	DNS CTRL 00	0x04	RW	Bit[3:0]: Coefficient of Y de-noise threshold with respect to Y
0x5291	DNS CTRL 01	0x06	RW	Bit[4:0]: Coefficient of UV de-noise threshold with respect to Y
0x5292	DNS CTRL 02	0x00	RW	Bit[0]: De-noise and sharpness manual mode enable 0: Auto 1: Manual
0x5293	NOISE Y	0x02	RW	Bit[7:0]: noise_y De-noise weight for Y
0x5294	NOISE U	0x00	RW	Bit[0]: Noise U[8] De-noise weight for UV
0x5295	NOISE U	0x02	RW	Bit[7:0]: Noise U[7:0] De-noise weight for UV
0x5296	NOISE V	0x00	RW	Bit[0]: Noise V[8] De-noise weight for UV
0x5297	NOISE V	0x02	RW	Bit[7:0]: Noise V[7:0] De-noise weight for UV
0x5298	DNS EDGETHRE MAN	0x06	RW	Bit[7:0]: DNS edgethre Edge threshold for UV smoothing
0x5299	DNS GBGR EXTRA	0x0C	RW	Bit[2:0]: dns_gbgr_extra De-noise threshold adjustment for Gb and Gr
0x529A	NOISE YLIST0	0x01	RW	Bit[7:0]: Noise Y list0[7:0] Noise Y threshold at 1x sensor gain
0x529B	NOISE YLIST1	0x01	RW	Bit[7:0]: Noise Y list1[7:0] Noise Y threshold at 2x sensor gain

table 5-7 DNS registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x529C	NOISE YLIST2	0x01	RW	Bit[7:0]: Noise Y list2[7:0] Noise Y threshold at 4x sensor gain
0x529D	NOISE YLIST3	0x01	RW	Bit[7:0]: Noise Y list03[7:0] Noise Y threshold at 8x sensor gain
0x529E	NOISE YLIST4	0x01	RW	Bit[7:0]: Noise Y list4[7:0] Noise Y threshold at 16x sensor gain
0x529F	NOISE YLIST5	0x01	RW	Bit[7:0]: Noise Y list5[7:0] Noise Y threshold at 32x sensor gain
0x52A0	NOISE YLIST6	0x02	RW	Bit[7:0]: Noise Y list6[7:0] Noise Y threshold at 64x sensor gain
0x52A1	NOISE YLIST7	0x02	RW	Bit[7:0]: Noise Y list7[7:0] Noise Y threshold at 64x sensor gain
0x52A2	NOISE UVLIST0	0x00	RW	Bit[0]: Noise UV list0[8] Noise UV threshold at 1x sensor gain
0x52A3	NOISE UVLIST0	0x02	RW	Bit[7:0]: Noise UV list0[7:0] Noise UV threshold at 1x sensor gain
0x52A4	NOISE UVLIST1	0x00	RW	Bit[0]: Noise UV list1[8] Noise UV threshold at 2x sensor gain
0x52A5	NOISE UVLIST1	0x02	RW	Bit[7:0]: Noise UV list1[7:0] Noise UV threshold at 2x sensor gain
0x52A6	NOISE UVLIST2	0x00	RW	Bit[0]: Noise UV list2[8] Noise UV threshold at 4x sensor gain
0x52A7	NOISE UVLIST2	0x02	RW	Bit[7:0]: Noise UV list2[7:0] Noise UV threshold at 4x sensor gain
0x52A8	NOISE UVLIST3	0x00	RW	Bit[0]: Noise UV list3[8] Noise UV threshold at 8x sensor gain

table 5-7 DNS registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x52A9	NOISE UVLIST3	0x02	RW	Bit[7:0]: Noise UV list3[7:0] Noise UV threshold at 8x sensor gain
0x52AA	NOISE UVLIST4	0x00	RW	Bit[0]: Noise UV list4[8] Noise UV threshold at 16x sensor gain
0x52AB	NOISE UVLIST4	0x02	RW	Bit[7:0]: Noise UV list4[7:0] Noise UV threshold at 16x sensor gain
0x52AC	NOISE UVLIST5	0x00	RW	Bit[0]: Noise UV list5[8] Noise UV threshold at 32x sensor gain
0x52AD	NOISE UVLIST5	0x02	RW	Bit[7:0]: Noise UV list5[7:0] Noise UV threshold at 32x sensor gain
0x52AE	NOISE UVLIST6	0x00	RW	Bit[0]: Noise UV list6[8] Noise UV threshold at 64x sensor gain
0x52AF	NOISE UVLIST6	0x03	RW	Bit[7:0]: Noise UV list6[7:0] Noise UV threshold at 64x sensor gain
0x52B0	NOISE UVLIST7	0x00	RW	Bit[0]: Noise UV list7[8] Noise UV threshold at 64x sensor gain
0x52B1	NOISE UVLIST7	0x03	RW	Bit[7:0]: Noise UV list7[7:0] Noise UV threshold at 64x sensor gain

5.8 color interpolation (CIP)

The main function of the color interpolation (CIP) is interpolation from raw data to YUV data. For edge enhancement, both manual and auto modes are provided. RAW format is used for the sensor source image data, which means only one of R, G and B can be used for each pixel. CIP is needed to get the other two color values. CIP calculates those two color values using the neighboring same pixel (such as a real B pixel) to get the full RGB information for each pixel. YUV information can also be supported. The CIP functions include de-noising of raw images, RAW to RGB interpolation, and edge enhancement. CIP functions work in both manual and auto modes.

table 5-8 CIP registers

address	register name	default value	RW	description
0x5000	ISP CTRL00	1'b1	RW	Bit[0]: Color interpolation (CIP) enable 0: Disable 1: Enable
0x5045	ISP CTRL69	0x00	RW	Bit[3]: interlace_man Bit[2]: interlace_man_en Bit[1]: bw_man Bit[0]: bw_man_en

5.9 color matrix (CMX)

The main purpose of color matrix (CMX) is converting the image from RGB domain to YUV domain. For different color temperature, the parameters in the transmitting function will be changed. Given the color correction matrix, CCM, and RGB to YUV conversion matrix, RGB2YUV, the combined matrix is:

$$CMX = \begin{bmatrix} cmx00 & cmx01 & cmx02 \\ cmx10 & cmx11 & cmx12 \\ cmx20 & cmx21 & cmx22 \end{bmatrix} = BGR2YUV \times CCM \times \begin{bmatrix} 1 & 0.75 & -0.25 \\ 1 & -0.25 & -0.25 \\ 1 & -0.25 & 0.75 \end{bmatrix}$$

$$\text{where} \begin{bmatrix} B \\ G \\ R \end{bmatrix} = CCM \begin{bmatrix} B_0 \\ G_0 \\ R_0 \end{bmatrix}$$

The CMX is then normalized by $2^{0x5394[3:0]}$.

table 5-9 CMX registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5001	ISP CTRL01	1'b1	RW	Bit[1]: Color matrix enable 0: Disable 1: Enable
0x5380	CMX00	0x01	RW	Bit[1:0]: cmx00[9:8]
0x5381	CMX00	0x00	RW	Bit[7:0]: cmx00[7:0]
0x5382	CMX01	0x00	RW	Bit[1:0]: cmx01[9:8]
0x5383	CMX01	0x44	RW	Bit[7:0]: cmx01[7:0]
0x5384	CMX02	0x00	RW	Bit[1:0]: cmx02[9:8]
0x5385	CMX02	0x0B	RW	Bit[7:0]: cmx02[7:0]
0x5386	CMX10	0x00	RW	Bit[1:0]: cmx10[9:8]
0x5387	CMX10	0x00	RW	Bit[7:0]: cmx10[7:0]
0x5388	CMX11	0x01	RW	Bit[1:0]: cmx11[9:8]
0x5389	CMX11	0x06	RW	Bit[7:0]: cmx11[7:0]
0x538A	CMX12	0x00	RW	Bit[1:0]: cmx12[9:8]
0x538B	CMX12	0x25	RW	Bit[7:0]: cmx12[7:0]
0x538C	CMX20	0x00	RW	Bit[1:0]: cmx20[9:8]
0x538D	CMX20	0x00	RW	Bit[7:0]: cmx20[7:0]
0x538E	CMX21	0x00	RW	Bit[1:0]: cmx21[9:8]
0x538F	CMX21	0x02	RW	Bit[7:0]: cmx21[7:0]
0x5390	CMX22	0x00	RW	Bit[1:0]: cmx22[9:8]

table 5-9 CMX registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5391	CMX22	0xD2	RW	Bit[7:0]: cmx22[7:0]
0x5392	CMX SIGN	0x00	RW	Bit[0]: cmx_sign[8]
0x5393	CMX SIGN	0x26	RW	Bit[7:0]: cmx_sign[7:0]
0x5394	CMX SHIFT	0x08	RW	Bit[3:0]: cmx_shift

5.10 contrast

The auto contrast module is designed to stretch the image linearly to adjust the contrast according to the statistics results. According to the chosen parameters, the function can automatically calculate the maximum and minimum levels. Thus, the image will be adjusted to the correct brightness in different scenes which are implemented using the statistic information of each frame.

table 5-10 contrast registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5001	ISP CTRL01	1'b1	RW	Bit[3]: Auto contrast enable 0: Disable 1: Enable
0x5400	CONTRAST MAX HIGH LEVEL	0x3F	RW	Bit[6:0]: Maximum high level[14:8] Maximum high level threshold Changing this value is not recommended
0x5401	CONTRAST MAX HIGH LEVEL	0xFF	RW	Bit[7:0]: Maximum high level[7:0] Maximum high level threshold Changing this value is not recommended
0x5402	CONTRAST MIN HIGH LEVEL	0x34	RW	Bit[6:0]: Minimum high level[14:8] Minimum high level threshold in 15-bit scale
0x5403	CONTRAST MIN HIGH LEVEL	0x00	RW	Bit[7:0]: min_high_level[7:0]
0x5404	CONTRAST MAX LOW LEVEL	0x02	RW	Bit[6:0]: Maximum low level[14:8] Maximum low level threshold in 15-bit scale
0x5405	CONTRAST MAX LOW LEVEL	0x40	RW	Bit[7:0]: Maximum low level[7:0] Maximum low level threshold in 15-bit scale

table 5-10 contrast registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5406	CONTRAST MIN LOW LEVEL	0x00	RW	Bit[6:0]: Minimum low level[14:8] Minimum low level threshold in 15-bit data range
0x5407	CONTRAST MIN LOW LEVEL	0x00	RW	Bit[7:0]: Minimum low level[7:0] Minimum low level threshold in 15-bit data range

5.11 YUV gamma (YGMA)

For the YUVGAMMA function, UV gamma is separated from Y gamma. The UV gamma curve has a special relationship with Y gamma. Also, some special functions related to UV and Y processing in dark and bright conditions are available.

When RGMA is enabled, all parameters of YGMA will be fixed.

table 5-11 YGMA registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	1'b1	RW	Bit[6]: Gamma (in YUV domain) enable 0: Disable 1: Enable
0x5480	GAMMA CTRL00	0x12	RW	Bit[7:0]: y_list_00 Output at 0x10 (10-bit scale) when register 0x5000[5] = 1
0x5481	GAMMA CTRL01	0x1D	RW	Bit[7:0]: y_list_01 Output at 0x20 (10-bit scale) when register 0x5000[5] = 1
0x5482	GAMMA CTRL02	0x2B	RW	Bit[7:0]: y_list_02 Output at 0x40 (10-bit scale) when register 0x5000[5] = 1
0x5483	GAMMA CTRL03	0x40	RW	Bit[7:0]: y_list_03 Output at 0x80 (10-bit scale) when register 0x5000[5] = 1
0x5484	GAMMA CTRL04	0x49	RW	Bit[7:0]: y_list_04 Output at 0xA0 (10-bit scale) when register 0x5000[5] = 1
0x5485	GAMMA CTRL05	0x51	RW	Bit[7:0]: y_list_05 Output at 0xC0 (10-bit scale) when register 0x5000[5] = 1

table 5-11 YGMA registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5486	GAMMA CTRL06	0x59	RW	Bit[7:0]: y_list_06 Output at 0xE0 (10-bit scale) when register 0x5000[5] = 1
0x5487	GAMMA CTRL07	0x62	RW	Bit[7:0]: y_list_07 Output at 0x100 (10-bit scale) when register 0x5000[5] = 1
0x5488	GAMMA CTRL08	0x6A	RW	Bit[7:0]: y_list_08 Output at 0x120 (10-bit scale) when register 0x5000[5] = 1
0x5489	GAMMA CTRL09	0x73	RW	Bit[7:0]: y_list_09 Output at 0x140 (10-bit scale) when register 0x5000[5] = 1
0x548A	GAMMA CTRL0A	0x88	RW	Bit[7:0]: y_list_10 Output at 0x180 (10-bit scale) when register 0x5000[5] = 1
0x548B	GAMMA CTRL0B	0xA0	RW	Bit[7:0]: y_list_11 Output at 0x1C0 (10-bit scale) when register 0x5000[5] = 1
0x548C	GAMMA CTRL0C	0xCA	RW	Bit[7:0]: y_list_12 Output at 0x240 (10-bit scale) when register 0x5000[5] = 1
0x548D	GAMMA CTRL0D	0xE0	RW	Bit[7:0]: y_list_13 Output at 0x2C0 (10-bit scale) when register 0x5000[5] = 1
0x548E	GAMMA CTRL0E	0xEA	RW	Bit[7:0]: y_list_14 Output at 0x340 (10-bit scale) when register 0x5000[5] = 1
0x548F	GAMMA CTRL0F	0x0F	RW	Bit[7:0]: y_list_15 Slope in range of (0x341, 0x3FF) which should be 2 x (255 - register 0x548E) / 3

5.12 UV average (UVAVG)

The main purpose of the UVAVG module is to smooth UV by averaging.

table 5-12 UVAVG registers

address	register name	default value	R/W	description
0x5001	ISP CTRL01	1'b1	RW	Bit[2]: UV average enable 0: Disable 1: Enable
0x5005	ISP CTRL05	1'b0	RW	Bit[5]: UV average old style enable 0: Disable 1: Enable

5.13 UV adjust (UVADJ)

The main purpose of the UVADJ module is to adjust UV according to the sensor gain and register parameters.

table 5-13 UV adjust registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5001	ISP CTRL01	1'b1	RW	Bit[6]: Auto color saturation adjust enable 0: Disable 1: Enable
0x5500	UV UVADJUST CONTROL 0	0x08	RW	Bit[4:0]: Auto color saturation offset UV ADJUST IN value minimum threshold
0x5501	UV UVADJUST CONTROL 3	0x1F	RW	Bit[5]: Color saturation manual adjustment enable 0: Automatically adjust color saturation according to sensor gain 1: Manually set color saturation by register 0x5501[4:0] Bit[4:0]: UV ADJUST IN manual setting Manual color saturation setting

table 5-13 UV adjust registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5502	UV ADJ TH1	0x00	RW	Bit[0]: uv_adj_th1[8] Real gain threshold 1 for UV ADJUST IN. When real gain is smaller than UV ADJ TH1, UV ADJUST IN will be limited to 31
0x5503	UV ADJ TH1	0x1F	RW	Bit[7:0]: UV ADJ TH1[7:0] Real gain threshold 1 for UV ADJUST IN. When real gain is smaller than UV ADJ TH1, UV ADJUST IN will be limited to 31.
0x5504	UV ADJ TH2	0x00	RW	Bit[0]: uv_adj_th2[8] Real gain threshold 2 for UV ADJUST IN. When real gain is larger than UV ADJ TH1, UV ADJUST IN will be limited to UV offset (0x5500[4:0]).
0x5505	UV ADJ TH2	0x7F	RW	Bit[7:0]: UV adj th2[7:0] Real gain threshold 2 for UV ADJUST IN. When real gain is larger than UV ADJ TH1, UV ADJUST IN will be limited to UV offset (0x5500[4:0]).

5.14 special digital effect (SDE)

The main purpose of special digital effect (SDE) is making special digital effects such as hue/saturation etc.

Use SDE_Ctrl to perform the following effects:

- calculate the new U and V based on Hue Cos, Hue Sin and sign of the parameters; if the hue angle is enabled, calculation will be based on hue angle
- fix U and V values
- saturate U and V according to Sat_u and Sat_v
- calculate Y from Y offset, Y gain, and Y bright
- set Y to be a fixed value
- invert Y, U, and V values to get a negative image
- fix U and V to 128 (8-bit data) resulting in a gray image

table 5-14 SDE registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5001	ISP CTRL01	1'b0	RW	Bit[7]: Special digital effects (SDE) enable 0: Disable 1: Enable
0x5580	SDE CONTROL0	0x00	RW	Bit[7]: Fixed Y enable - works with register 0x5587[7:0] 0: Fixed Y disable 1: Fixed Y enable Bit[6]: Negative Y enable 0: Negative Y disable 1: Negative Y enable Bit[5]: Gray image enable 0: Gray image disable 1: Gray image enable Bit[4]: Fixed V enable - works with register 0x5586[7:0] 0: Fixed V disable 1: Fixed V enable Bit[3]: Fixed U enable - works with register 0x5585[7:0] 0: Fixed U disable 1: Fixed U enable Bit[2]: Contrast enable - works with registers 0x5587[7:0], 0x5588[7:0], and 0x5589[7:0] 0: Contrast disable 1: Contrast enable Bit[1]: Saturation enable - works with registers 0x5583[7:0] and 0x5584[7:0] 0: Saturation disable 1: Saturation enable Bit[0]: Hue enable 0: Hue disable 1: Hue enable

table 5-14 SDE registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5581	SDE CONTROL1	0x80	RW	Bit[7:0]: hue_cos When register 0x558A[6] = 0, this register is hue_cos. When register 0x558A[6] = 1, this register is angle[7:0].
0x5582	SDE CONTROL2	0x00	RW	Bit[7:0]: hue_sin When register 0x558A[6] = 0, this register is hue_sin. When register 0x558A[6] = 1, this register is angle[8]
0x5583	SDE CONTROL3	0x40	RW	Bit[7:0]: Saturation U
0x5584	SDE CONTROL4	0x40	RW	Bit[7:0]: Saturation V
0x5585	SDE CONTROL5	0x80	RW	Bit[7:0]: Ureg for fixed U
0x5586	SDE CONTROL6	0x80	RW	Bit[7:0]: Vreg for fixed V
0x5587	SDE CONTROL7	0x00	RW	Bit[7:0]: Yoffset for contrast or Y value for fixed Y
0x5588	SDE CONTROL8	0x20	RW	Bit[7:0]: Ygain for contrast
0x5589	SDE CONTROL9	0x00	RW	Bit[7:0]: Ybright for contrast
0x558A	SDE CONTROL10	0x01	RW	Bit[7]: Yoffset manual mode enable 0: Auto mode for Yoffset in contrast 1: Manual mode for Yoffset in contrast Bit[6]: Hue angle enable Bit[5]: COS sign for Cr Bit[4]: COS sign for Cb Bit[3]: Offset sign for contrast Bit[2]: Bright sign for contrast Bit[1]: SIN sign for Cb Bit[0]: SIN sign for Cr

5.15 clip

The main purpose of the clip module is to clip the Y and UV data with Y threshold and C threshold

table 5-15 clip registers

address	register name	default value	R/W	description
0x5041	ISP CTRL65	1'b1	RW	Bit[1]: yclp_en
0x5053	CLIP YTHREH	0xFF	RW	Bit[7:0]: y_thre_h
0x5054	CLIP YTHREL	0x00	RW	Bit[7:0]: y_thre_l
0x5055	CLIP CTHREH	0xFF	RW	Bit[7:0]: c_thre_h
0x5056	CLIP CTHREL	0x00	RW	Bit[7:0]: c_thre_l

5.16 16-zone luminance average (YAVG)

The main purposes of the YAVG module are:

- calculate Y average based on selected window
- output one average of window each time
- output Y data

table 5-16 YAVG registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5041	ISP CTRL65	1'b1	RW	Bit[4]: yavg_en
0x5042	ISP CTRL66	1'b0 2'b11	RW	Bit[3]: out_size_mode Bit[1:0]: yavg_source
0x5680	AVG XSTART	0x00	RW	Bit[3:0]: Avg x start[11:8] Horizontal start position for average window
0x5681	AVG XSTART	0x00	RW	Bit[7:0]: Avg x start[7:0] Horizontal start position for average window
0x5682	AVG XEND	0x08	RW	Bit[3:0]: Avg x end[11:8] Horizontal end position for average window
0x5683	AVG XEND	0x00	RW	Bit[7:0]: Avg x end[7:0] Horizontal end position for average window

table 5-16 YAVG registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5684	AVG YSTART	0x00	RW	Bit[2:0]: Avg y start[10:8] Vertical start position for average window
0x5685	AVG YSTART	0x00	RW	Bit[7:0]: Avg y start[7:0] Vertical start position for average window
0x5686	AVG YEND	0x06	RW	Bit[2:0]: Avg y end[10:8] Vertical end position for average window
0x5687	AVG YEND	0x00	RW	Bit[7:0]: Avg y end[7:0] Vertical end position for average window
0x5688	AVG R8	0xFF	RW	Bit[5:4]: window1_weight Bit[1:0]: window0_weight
0x5689	AVG R9	0xFF	RW	Bit[5:4]: window3_weight Bit[1:0]: window2_weight
0x568A	AVG RA	0xFF	RW	Bit[5:4]: window5_weight Bit[1:0]: window4_weight
0x568B	AVG RB	0xFF	RW	Bit[5:4]: window7_weight Bit[1:0]: window6_weight
0x568C	AVG RC	0xFF	RW	Bit[5:4]: window9_weight Bit[1:0]: window8_weight
0x568D	AVG RD	0xFF	RW	Bit[5:4]: window11_weight Bit[1:0]: window10_weight
0x568E	AVG RE	0xFF	RW	Bit[5:4]: window13_weight Bit[1:0]: window12_weight
0x568F	AVG RF	0xFF	RW	Bit[5:4]: window15_weight Bit[1:0]: window14_weight
0x5690	AVG CTRL08	0x00	RW	Bit[7]: win_man Bit[3:0]: yavg_mnr
0x5691	AVG BLK THRESH	0x00	RW	Bit[7:0]: blk_thresh
0x5692	AVG WHT THRESH	0xFF	RW	Bit[7:0]: wht_thresh

5.17 TV encoder

table 5-17 TV encoder registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x6400	WHITE LEVEL	0xFF	RW	Bit[7:0]: White level
0x6401	NORMAL LEVEL	0x56 (NTSC) 0x4E (PAL)	RW	Bit[7:0]: Normal level
0x6402	BLANK LEVEL	0x48 (NTSC) 0x4E (PAL)	RW	Bit[7:0]: Blank level
0x6403	SYNC LEVEL	0x02	RW	Bit[7:0]: Sync level
0x6404	BURST LEVEL	0x2A	RW	Bit[7:0]: Burst level
0x6405	MAX LEVEL	0xFF	RW	Bit[7:0]: Maximum level
0x6406	CHROMA SAT	0x7F	RW	Bit[6:0]: Chroma saturation
0x6407	MOD SHIFT	0x25 (NTSC) 0x26 (PAL)	RW	Bit[7:0]: Mode shift[23:16] For burst frequency adjust
0x6408	MOD SHIFT	0x55 (NTSC) 0x79 (PAL)	RW	Bit[7:0]: Mode shift[15:8] For burst frequency adjust
0x6409	MOD SHIFT	0x5A (NTSC) 0x8C (PAL)	RW	Bit[7:0]: Mode shift[7:0] For burst frequency adjust
0x640A	SCUSER	0x80	RW	Bit[7:0]: Sub-carrier clock option Manually set by user
0x640B	SCACT NTSC	0x00	RW	Bit[7:0]: Sub-carrier clock option NTSC default
0x640C	SCACT PAL	0x20	RW	Bit[7:0]: Sub-carrier clock option PAL default
0x640D	TEST MOD	0x88	RW	Bit[0]: Test mode
0x640E	SIN INS	0xFF (NTSC) 0xFF (PAL)	RW	Bit[7:0]: Sine parameter for burst
0x640F	COS INS	0xE3 (NTSC) 0x97 (PAL)	RW	Bit[7:0]: Cosine parameter for burst
0x6410	MIN LEVEL	0x90 (NTSC) 0x7F (PAL)	RW	Bit[7:0]: Minimum level
0x6411	COEF Y HIGH	0x52 (NTSC) 0x57 (PAL)	RW	Bit[7:0]: Coefficient Y high
0x6412	COEF U HIGH	0x54 (NTSC) 0x59 (PAL)	RW	Bit[7:0]: Coefficient U high

table 5-17 TV encoder registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x6413	COEF V HIGH	0x54 (NTSC) 0x59 (PAL)	RW	Bit[7:0]: Coefficient V high
0x6414	COEF YUV LOW	0x02	RW	Bit[7:0]: Coefficient Y low
0x6415	Y OFFSET	0x00	RW	Bit[0]: Y offset
0x6416	CBAR EN	0x10	RW	Bit[0]: Encoder color bar enable
0x6417	FILTER CTRL	0x05 (NTSC) 0x85 (PAL)	RW	Bit[7:0]: Encoder low pass filter control
0x6418	HSYNC LENGTH	0x73 (NTSC) 0x8B (PAL)	RW	Bit[7:0]: HSYNC length
0x6419	BURST LENG	0xBE (NTSC) 0xC3 (PAL)	RW	Bit[6:0]: Burst length
0x641A	FPORCH LENG	0x23	RW	Bit[5:0]: Fporch length
0x641B	BPORCH LENG	0xCE (NTSC) 0xD6 (PAL)	RW	Bit[5:0]: Bporch length

6 image sensor output interface digital functions

6.1 TV mode

6.1.1 timing diagrams

figure 6-1 NTSC timing diagram

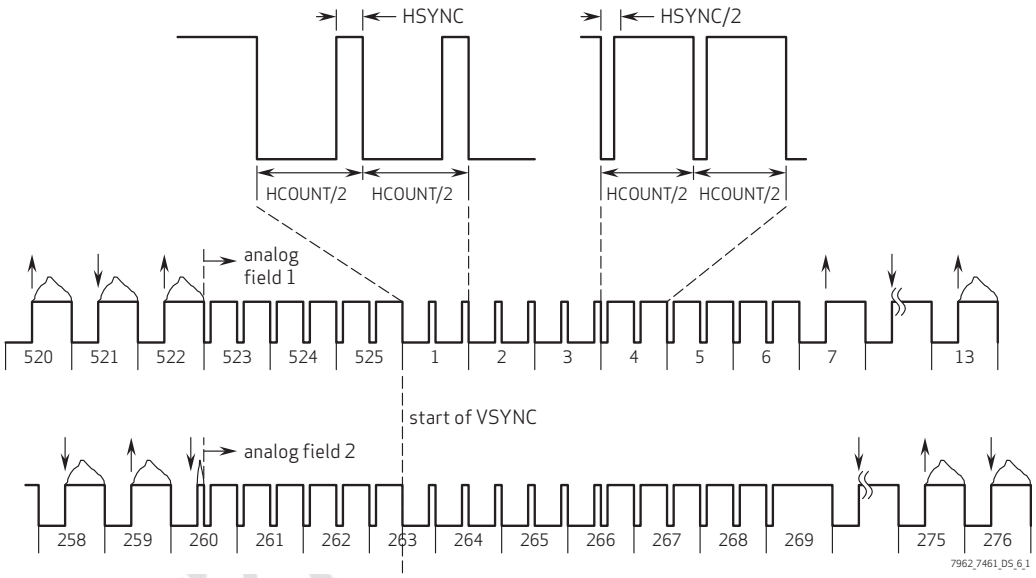
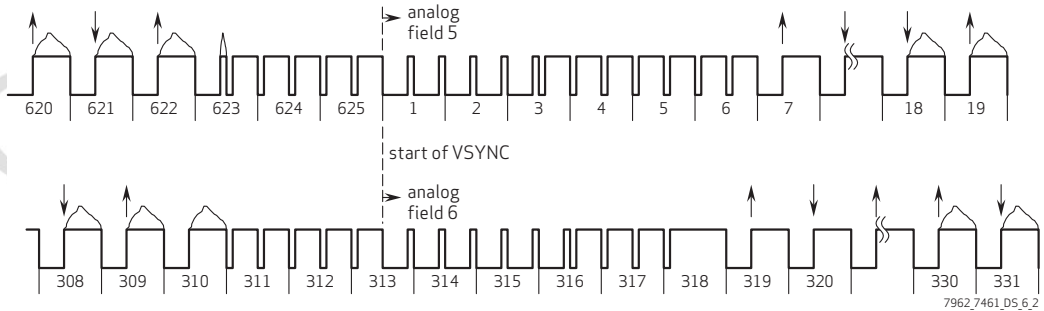


figure 6-2 PAL timing diagram



6.1.2 composite video signals

figure 6-3 NTSC composite video signal

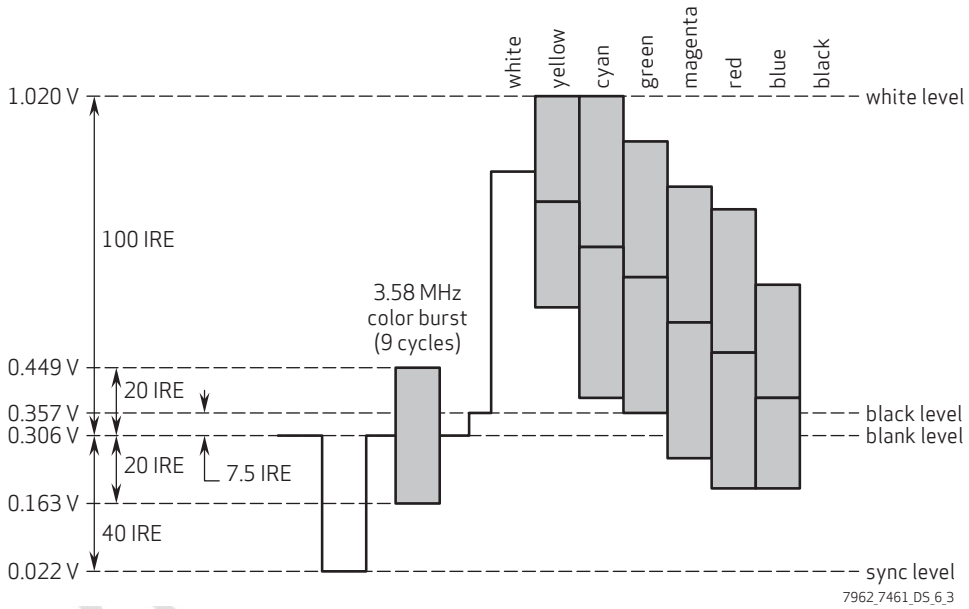
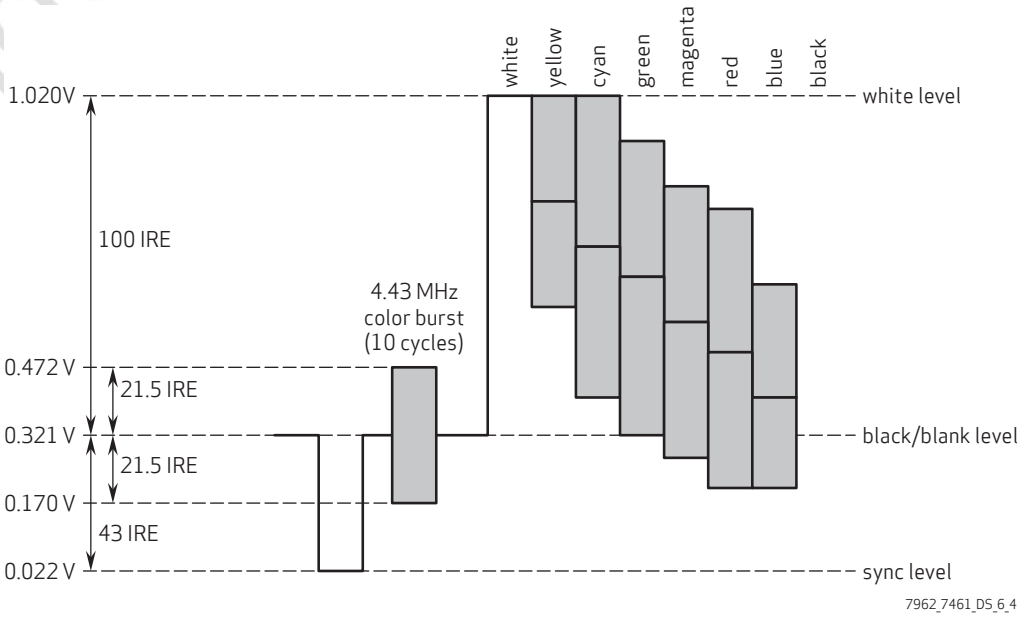


figure 6-4 PAL composite video signal



6.2 digital video port (DVP)

DVP supports RAW, RGB565, RGB666 and YUV422 data formats. It also supports HREF mode, HSYNC mode and ITU656 timing.

The VSYNC, HREF and PCLK have programmable polarity. The DVP data can be clipped by a programmable low boundary and high boundary. Also, the DVP data bits can be switched from 9:0 to 0:9 and from 9:2 to 2:9. The DVP data has options to right shift 1 and 2 bits while high bits will be set to low. For blackout video, the DVP data has an option to output all 0.

HSYNC mode supports maximum 8 dummy pixels in front of each line and 8 dummy pixels at the end of each line.

HSYNC and ITU656 timing is only available at full resolution and sub-sample mode. As long as scaling is enabled, HSYNC and ITU656 mode should be disabled.

The period of the horizontal blank prior to the first valid line may be different from other horizontal blank periods in HSYNC timing.

The horizontal blanking time may be different from line to line during the whole frame when scaling function is enabled. In full or sub-sample mode, all the horizontal and vertical blanking times are the same for every frame.

ITU656 timing needs to support external TV encoder chip for both NTSC and PAL.

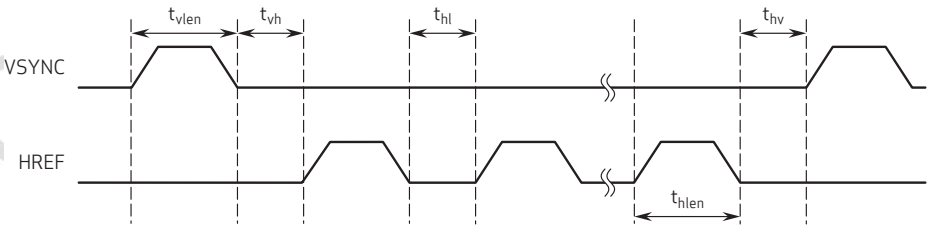
The DVP pins will be tri-state after power on. Users need to set registers to enable normal DVP function. Power down direction and output value are register programmable. VSYNC and HREF can be programmed to GPIO.

DVP supports master and slave mode.

6.2.1 HREF mode

HREF mode is the default mode of DVP. Every VSYNC indicates a frame start and data is valid when HREF is high.

figure 6-5 HREF mode

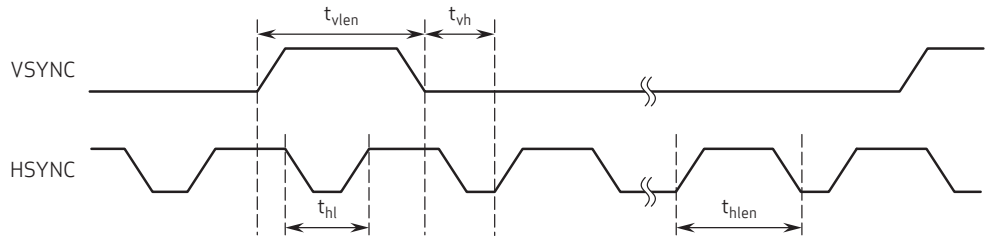


note t_{vh}, t_{hv}, t_{hlen}, t_{vlen}, and t_{hl} are fixed every frame at full resolution or sensor sub-sample mode, with arbitrary windowing.
t_{vh} may differ depending on ISP setting.
t_{hl} may be different in the same frame if scaling function is enabled.

7962_7461_DS_6_5

6.2.2 HSYNC mode

figure 6-6 HSYNC mode



note t_{vh}, t_{heln}, t_{vlen}, and t_{hl} are fixed every frame at full resolution or sensor sub-sample mode, with arbitrary windowing.

7962_7461_DS_6_6

6.2.3 CCIR656 mode

The OV7962/OV7461 supports standard CCIR656. Write to register 0x4720[0] to enable CCIR656 mode.

figure 6-7 CCIR656 timing

note XP: {1, F, V, H, P[3:0]}

F: 0 is field1, 1 is field 2	1	0	0	0	0	0	0	0	1	1	0	0	0	1	1	1
V: 1 for field blanking, 0 for else	1	0	0	1	1	1	0	1	1	1	0	1	1	0	1	0
H: 0 in SAV, 1 in EAV	1	0	1	0	1	0	1	1	1	1	1	0	1	1	0	0
P[3:0]: protect bits	1	0	1	1	0	1	1	0	1	1	1	1	0	0	0	1

7962_7461_DS_6_7

figure 6-8 DVP timing diagram

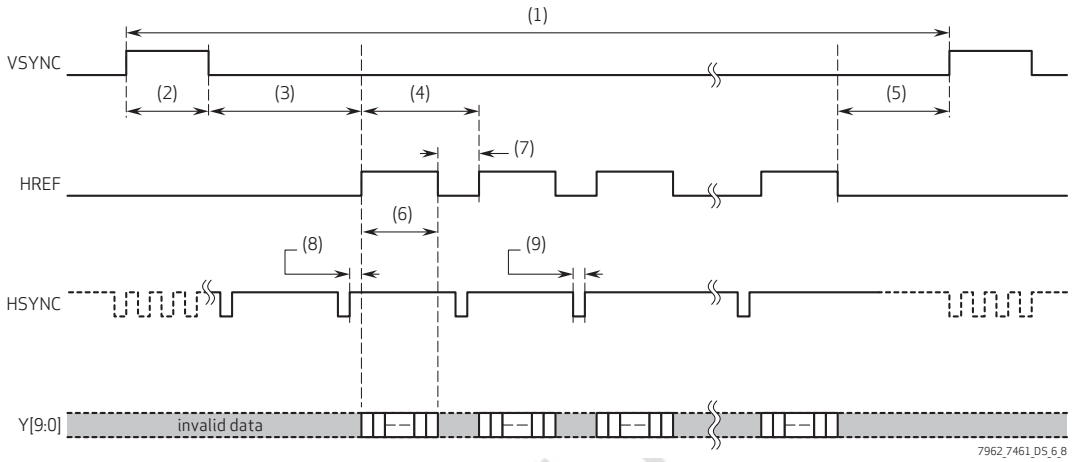


table 6-1 DVP timing specifications

mode	timing
WVGA 752x480	(1) 449072 tp (508 lines) (2) 1768 tp (2 lines) (3) 18704 tp (4) 884 tp (5) 4412 tp (6) 752 tp (7) 132 tp (8) 25 tp (9) 64 tp
VGA 640x480	(1) 400336 tp (524 lines) (2) 1528 tp (2 lines) (3) 20004 tp (4) 764 tp (5) 12208 tp (6) 640 tp (7) 124 tp (8) 25 tp (9) 64 tp
QVGA 320x240	(1) 100084 tp (262 lines) (2) 764 tp (2 lines) (3) 4654 tp (4) 382 tp (5) 3048 tp (6) 320 tp (7) 62 tp (8) 77 tp (9) 16 tp

note
The timing values shown in **table 6-1** may vary depending upon register settings.

table 6-2 DVP registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4700	SHP MAN	0x00	RW	Bit[3:0]: sh_p_man[11:8]
0x4701	SHP MAN	0x00	RW	Bit[7:0]: sh_p_man[7:0]
0x4702	SHL MAN	0x00	RW	Bit[6:0]: sh_l_man[14:8]
0x4703	SVL MAN	0x02	RW	Bit[7:0]: sv_l_man[7:0]
0x4704	SVP MAN	0x00	RW	Bit[3:0]: sv_p_man[11:8]
0x4705	SVP MAN	0x00	RW	Bit[7:0]: sv_p_man[7:0]
0x4706	HVP MAN	0x02	RW	Bit[3:0]: hv_p_man[11:8]
0x4707	HVP MAN	0x88	RW	Bit[7:0]: hv_p_man[7:0]
0x4708	HVL MAN	0x0F	RW	Bit[7:0]: hv_l_man
0x4709	VSL MAN	0x04	RW	Bit[7:0]: vs_l_man
0x470A	LL VSP MAN	0x00	RW	Bit[4]: ll_man[16] Bit[3:0]: vs_p_man[11:8]
0x470B	VSP MAN	0x01	RW	Bit[7:0]: vs_p_man[7:0]
0x470C	LL MAN	0x03	RW	Bit[7:0]: ll_man[15:8]
0x470D	LL MAN	0x0C	RW	Bit[7:0]: ll_man[7:0]
0x470E	CCIR CTRL	0x04	RW	Bit[7]: ccir_f_sel Bit[6]: ccir_v_sel Bit[5:0]: ccir_f_num
0x470F	VREF OFFSET	0x01	RW	Bit[7:4]: vref_end_offset Bit[3:0]: vref_offset
0x4710	VREF ADJ	0x00	RW	Bit[7:4]: vref_end_adj Bit[3:0]: vref_st_adj
0x4711	PADL CNT	0x00	RW	Bit[7:0]: padl_cnt
0x4712	PADR CNT	0x00	RW	Bit[7:0]: padr_cnt
0x4713	VREF ST	0x0A	RW	Bit[7:0]: vref_st[7:0]
0x4714	VREF END	0x00	RW	Bit[7:0]: vref_end[7:0]
0x4715	VREF ENDST	0x10	RW	Bit[7:4]: vref_end[11:8] Bit[3:0]: vref_st[11:8]
0x4716	FREF ST	0x00	RW	Bit[7:0]: fref_st[7:0]
0x4717	FIELDVST FREFST	0x11	RW	Bit[7:4]: field_vst[11:8] Bit[3:0]: fref_st[11:8]

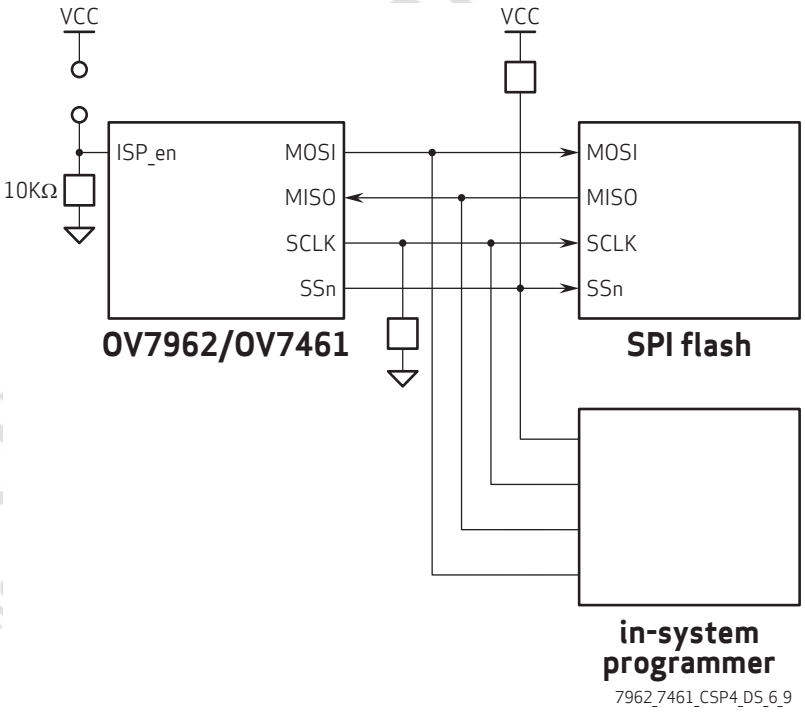
table 6-2 DVP registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4718	FIELD VST	0x00 (NTSC) 0x2C (PAL)	RW	Bit[7:0]: field_vst[7:0]
0x4719	FIELD HST	0x21 (NTSC) 0x3F (PAL)	RW	Bit[7:0]: field_hst[7:0]
0x471A	FIELD HST	0x02	RW	Bit[7:0]: field_hst[15:8]

6.3 overlay

6.3.1 hardware connection

figure 6-9 in-system programmer



On the hardware level, the connection from OV7962/OV7461 to serial flash is simply standard SPI. The OV7962/OV7461 supports in-system programming of SPI flash. Pull down pin C9 (OVLEN) and all four pins on the SPI port will be tri-stated, thus enabling an external downloader to program the flash.

6.3.2 internal overlay structure

The overlay image is read-in from SPI flash on a line-by-line, on-demand basis. Once inside, it is decompressed and mixed with pixel data. Up to four overlay images can be mixed in succession to produce the final output.

figure 6-10 overlay channels

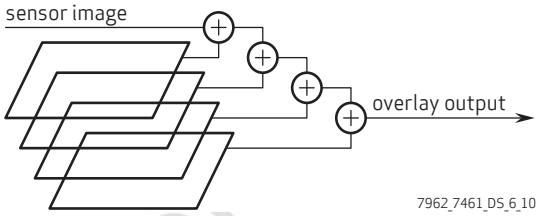
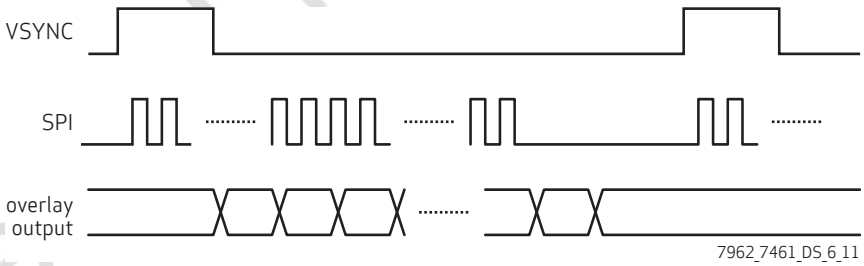


figure 6-11 relative timing



6.3.3 flash memory structure

The memory structure supports compressed overlay images in a proprietary 7-bit RLE format. It also supports the storage of boot ROM, application firmware, and register settings. The total number of images + boot ROM + register settings cannot exceed 1024.

table 6-3 overlay registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x6200	OSD_CTRL00	0x84	RW	Bit[7:6]: r_addr_byte 00: 1 byte address space of SPI EEPROM 01: 2 byte address space of SPI EEPROM 10: 3 byte address space of SPI EEPROM 11: 4 byte address space of SPI EEPROM Bit[5]: sclk_pol 0: Do not reverse spi_sclk_o 1: Reverse spi_sclk_o Bit[4:0]: spi_spd Max SPI speed is 49.09MHz 0: Set SCK as system clock speed 1: Two clock is one spi_sck.... SPI_clock frequency = Input system clock frequency/(2×SPI_SPD) (SPI_clock frequency = input system clock frequency, when X=0) Note: For OV7962 TV mode, SPI_clock frequency= {input system clock frequency/(2×SPI_SPD)}×2
0x6201	OSD_CTRL01	0x02	RW	Bit[7]: eof_clr 0: Use EOF to reset the whole module 1: Use SOF to reset the whole module Bit[6]: grp_hld 0: Registers will take effect 1: Registers will hold Bit[4:0]: spi_dly SPI delay for every command, unit is system clock cycle

table 6-3 overlay registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x6202	OSD_CTRL02	0x3F	RW	Bit[7]: sccb_acc 0: SCCB does not access SPI bus 1: SCCB access SPI bus Bit[6]: r_wr_en 0: sccb_wdata is not output 1: sccb_wdata is output Bit[5]: r_fast_rd Bit[4:0]: r_seq_nu OSD_SEQ number
0x6203	OSD_CTRL03	0x0B	RW	Bit[7:0]: Fast read instruction
0x6204	OSD_CTRL04	0x03	RW	Bit[7:0]: Normal read instruction
0x6205	OSD_CTRL05	0x03	RW	Bit[7:0]: index_l for layer 0
0x6206	OSD_CTRL06	0x04	RW	Bit[7:0]: index_l for layer 1
0x6207	OSD_CTRL07	0x04	RW	Bit[7:0]: index_l for layer 2
0x6208	OSD_CTRL08	0x04	RW	Bit[7:0]: index_l for layer 3
0x6209	OSD_CTRL09	0x00	RW	Bit[7:6]: index_h for layer 3 Bit[5:4]: index_h for layer 2 Bit[3:2]: index_h for layer 1 Bit[1:0]: index_h for layer 0
0x620A	OSD_CTRL0A	0x01	RW	Bit[7:6]: Resolution for layer 3 00: No overlay 01: 1x1 overlay 10: 2x2 overlay 11: 4x4 overlay Bit[5:4]: Resolution for layer 2 00: No overlay 01: 1x1 overlay 10: 2x2 overlay 11: 4x4 overlay Bit[3:2]: Resolution for layer 1 00: No overlay 01: 1x1 overlay 10: 2x2 overlay 11: 4x4 overlay Bit[1:0]: Resolution for layer 0 00: No overlay 01: 1x1 overlay 10: 2x2 overlay 11: 4x4 overlay
0x620B	OSD_CTRL0B	0x00	RW	Bit[7:0]: x_start_add_l for layer 0
0x620C	OSD_CTRL0C	0x00	RW	Bit[7:0]: y_start_add_l for layer 0

table 6-3 overlay registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x620D	OSD_CTRL0D	0x00	RW	Bit[7]: Sign bit of x_start_addr for layer 0 0: Positive 1: Negative Bit[6:4]: High bits of x_start_addr for layer 0 Bit[3]: Sign bit of y_start_addr for layer 0 0: Positive 1: Negative Bit[2:0]: High bits of y_start_addr for layer 0
0x620E	OSD_CTRL0E	0x00	RW	Bit[7:0]: x_start_add_l for layer 1
0x620F	OSD_CTRL0F	0x00	RW	Bit[7:0]: y_start_add_l for layer 1
0x6210	OSD_CTRL10	0x00	RW	Bit[7]: Sign bit of x_start_addr for layer 1 0: Positive 1: Negative Bit[6:4]: High bits of x_start_addr for layer 1 Bit[3]: Sign bit of y_start_addr for layer 1 0: Positive 1: Negative Bit[2:0]: High bits of y_start_addr for layer 1
0x6211	OSD_CTRL11	00x0	RW	Bit[7:0]: x_start_add_l for layer 2
0x6212	OSD_CTRL12	0x00	RW	Bit[7:0]: y_start_add_l for layer 2
0x6213	OSD_CTRL13	0x00	RW	Bit[7]: Sign bit of x_start_addr for layer 2 0: Positive 1: Negative Bit[6:4]: High bits of x_start_addr for layer 2 Bit[3]: Sign bit of y_start_addr for layer 2 0: Positive 1: Negative Bit[2:0]: High bits of y_start_addr for layer 2
0x6214	OSD_CTRL14	0x00	RW	Bit[7:0]: x_start_add_L for layer 3
0x6215	OSD_CTRL15	0x00	RW	Bit[7:0]: y_start_add_L for layer 3
0x6216	OSD_CTRL16	0x00	RW	Bit[7]: Sign bit of x_start_addr for layer 3 0: Positive 1: Negative Bit[6:4]: High bits of x_start_addr for layer 3 Bit[3]: Sign bit of y_start_addr for layer 3 0: Positive 1: Negative Bit[2:0]: High bits of y_start_addr for layer 3
0x6217	OSD_CTRL17	0x00	RW	Bit[7:0]: sccb_wdata

table 6-3 overlay registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x6218	OSD_CTRL18	0xE4	RW	Bit[7:6]: lay3_sel Bit[5:4]: lay2_sel Bit[3:2]: lay1_sel Bit[1:0]: lay0_sel
0x6219	OSD_CTRL19	0x00	RW	Bit[7:0]: r_ld_index
0x621A	OSD_CTRL1A	0x00	RW	Bit[7]: r_automovy_en3 Bit[6]: r_automovy_en2 Bit[5]: r_automovy_en1 Bit[4]: r_automovy_en0 Bit[3]: r_automovx_en3 Bit[2]: r_automovx_en2 Bit[1]: r_automovx_en1 Bit[0]: r_automovx_en0
0x621B	OSD_CTRL1B	0x00	RW	Bit[7]: r_automovy_wrap_en3 Bit[6]: r_automovy_wrap_en2 Bit[5]: r_automovy_wrap_en1 Bit[4]: r_automovy_wrap_en0 Bit[3]: r_automovx_wrap_en3 Bit[2]: r_automovx_wrap_en2 Bit[1]: r_automovx_wrap_en1 Bit[0]: r_automovx_wrap_en0
0x621C	OSD_CTRL1C	0x02	RW	Bit[7]: r_automv_step_sel Bit[6]: r_field_pol Bit[5]: r_spi_seln Bit[4]: r_ld_pad_dis Bit[3]: r_pon_ld_dis Bit[2]: r_fo_empty_clr Bit[1:0]: r_retry
0x621D	OSD_CTRL1D	0xFF	RW	Bit[7:0]: r_tog_cnt
0x621E	OSD_CTRL1E	0x20	RW	Bit[7:0]: r_seq_nu
0x621F	OSD_CTRL1F	0x04	RW	Bit[7]: r_read_once0 Bit[6]: r_read_once1 Bit[5]: r_read_once2 Bit[4]: r_read_once3 Bit[2]: r_retry_pon Bit[1]: r_interlace_dis Bit[0]: r_ld_blank

table 6-3 overlay registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x6220	OSD_CTRL20	0x00	RW	Bit[7]: r_autochg_wrap_en3 Bit[6]: r_autochg_wrap_en2 Bit[5]: r_autochg_wrap_en1 Bit[4]: r_autochg_wrap_en0 Bit[3]: r_autochg_en3 Bit[2]: r_autochg_en2 Bit[1]: r_autochg_en1 Bit[0]: r_autochg_en0
0x6221	OSD_CTRL21	0x00	RW	Bit[7:0]: r_autochg_stidx0[7:0]
0x6222	OSD_CTRL22	0x00	RW	Bit[7:0]: r_autochg_edidx0[7:0]
0x6223	OSD_CTRL23	0x00	RW	Bit[7:0]: r_autochg_stidx1[7:0]
0x6224	OSD_CTRL24	0x00	RW	Bit[7:0]: r_autochg_edidx1[7:0]
0x6225	OSD_CTRL25	0x00	RW	Bit[7:0]: r_autochg_stidx2[7:0]
0x6226	OSD_CTRL26	0x00	RW	Bit[7:0]: r_autochg_edidx2[7:0]
0x6227	OSD_CTRL27	0x00	RW	Bit[7:0]: r_autochg_stidx3[7:0]
0x6228	OSD_CTRL28	0x00	RW	Bit[7:0]: r_autochg_edidx3[7:0]
0x6229	OSD_CTRL29	0x00	RW	Bit[7:6]: r_autochg_edidx1[9:8] Bit[5:4]: r_autochg_stidx1[9:8] Bit[3:2]: r_autochg_edidx0[9:8] Bit[1:0]: r_autochg_stidx0[9:8]
0x622A	OSD_CTRL2A	0x00	RW	Bit[7:6]: r_autochg_edidx3[9:8] Bit[5:4]: r_autochg_stidx3[9:8] Bit[3:2]: r_autochg_edidx2[9:8] Bit[1:0]: r_autochg_stidx2[9:8]
0x622B	OSD_CTRL2B	0x00	RW	Bit[7:0]: r_autochg_step[7:0]
0x622C	OSD_CTRL2C	0x00	RW	Bit[7:0]: r_autochg_step[15:8]

6.3.4 SPI specifications

table 6-4 interface descriptions[a]

signal name	pin type	description
CS	output	chip select signal, active low
SCK	output	clock output
ESO	output	data output
ESI	input	data input

a. SPI bus are changed to inputs when OVLEN low

figure 6-12 basic timing diagram

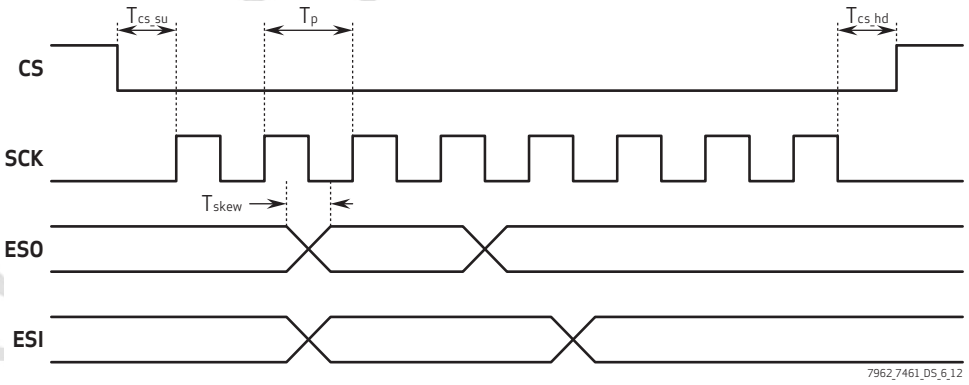


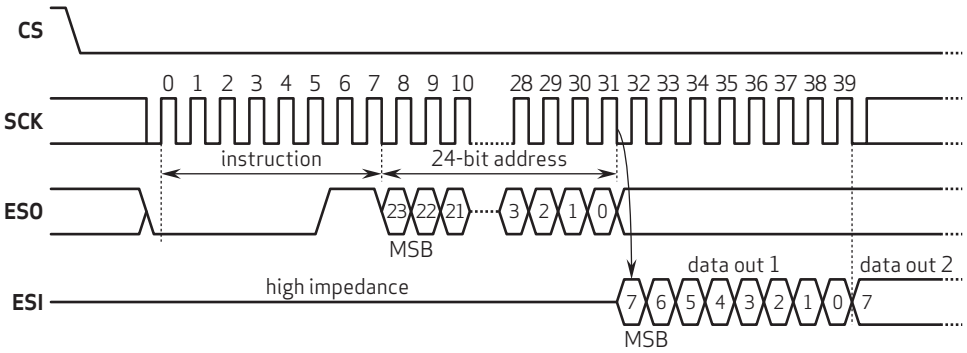
table 6-5 SPI timing[ab]

name	description	related register	min	max	unit
Tcs_su	CS setup time, 6201[4:0] + 1	0x6201[4:0]			system clock cycle
Tcs_hd	CS hold time, 6201[4:0] - 1	0x6201[4:0]			system clock cycle
Tp	SCK clock period it is divided by 2 × 0x6200[4:0] from 2 × system clock if 0x6200[4:0] is not 0, or it is 2 × system clock	0x6200[4:0]		49	MHz
Tskew	ESO skew from SCK		± 0.3	± 1.3	ns

a. ESO is launched at falling edge of SCK, user can use rising edge or SCK to latch data

b. user should launch ESI at falling edge of SCK, ESI at rising edge of SCK will latch by default

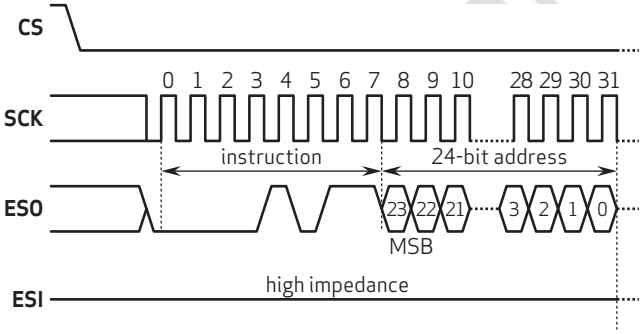
figure 6-13 normal read timing diagram

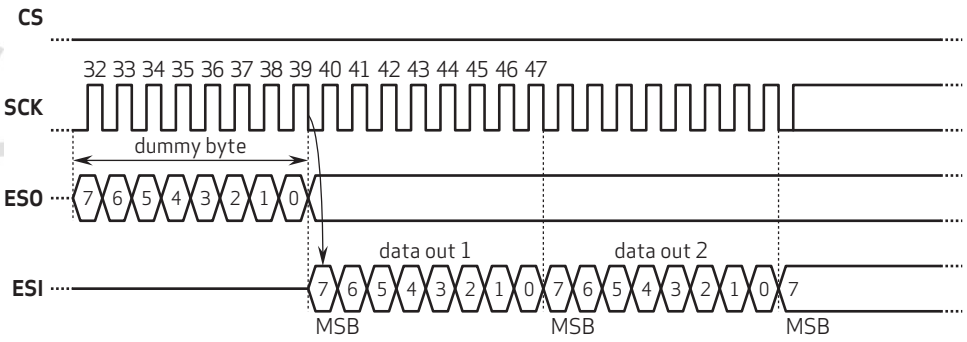


note as soon as the last bit been sent, device should return the first bit data at cycle #23

7962_7461_DS_6_13

figure 6-14 fast read timing diagram





note in fast read mode, there is one dummy byte following address bytes
ESI should be sent as soon as the last bit of dummy byte(cycle #40)

7962_7461_DS_6_14

7 register tables

The following tables provide a preliminary description of the device control registers contained in the OV7962/OV7461. Descriptions of additional registers will be released at a later date.The device slave address are 0x80 for write and 0x81 for read.

table 7-1 system control registers (sheet 1 of 26)

address	register name	default value	R/W	description
0x3000	GAIN	0x00	RW	Gain AGC[7:0] Refer to SCTRL09[1:0] (0x3015) for AGC[9:8] Gain = (AGC[9] + 1) × (AGC[8] + 1) × (AGC[7] + 1) × (AGC[6] + 1) × (AGC[5] + 1) × (AGC[4] + 1) × (AGC[3:0]/16 + 1) AGC[7:0] is analog gain, AGC[9:8] is digital gain
0x3001	BGAIN	0x00	RW	Bit[7:0]: BLUE[7:0] Blue channel gain Refer to BRGAINH[7:4] (0x3006) for BLUE[11:8] Blue gain = BLUE[11:0] / 0x400
0x3002	RGAIN	0x00	RW	Bit[7:0]: RED[7:0] Red channel gain Refer to BRGAINH[3:0] (0x3006) for RED[11:8] Red gain = RED[11:0] / 0x400
0x3003	GGAIN	0x00	RW	Bit[7:0]: GREEN[7:0] Green channel gain Refer to GGAINH[7:4] (0x3007) for GREEN[11:8] Green gain = GREEN[11:0] / 0x400
0x3004	SCTRL00	0x60	RW	Analog Control Bit[7]: Not used Bit[6:5]: Analog timing control Changing these values is not recommended Bit[4:2]: Analog control Changing these values is not recommended Bit[1:0]: Analog timing control Changing these values is not recommended

table 7-1 system control registers (sheet 2 of 26)

address	register name	default value	R/W	description
0x3005	SCTRL01	0x00	RW	Bit[7]: PAL/NTSC, COLOR/BW selection control 0: PAL/NTSC selected by PAL/NTSC pin, COLOR/BW selected by COLOR/BW pin 1: PAL/NTSC selected by register SCTRL06[6] (0x0x3012), COLOR/BW selected by register SCTRL06[5] (0x3012) Bit[6]: Banding control for NTSC 0: For 60Hz light 1: For 50Hz light Bit[5]: Banding filter control 0: Banding filter value is pre-defined, used for analog output 1: Banding filter is set by register BD50ST (0x3054) or BD60ST (0x3055), used for digital output Bit[4]: Manual sub-row exposure enable 0: Disable 1: Enable, exposure time is set by register LAECH (0x3030) and AECL(0x301F) Bit[3]: PAL window adjustment enable 0: Disable 1: Enable Bit[2]: Mirror control select 0: Mirror controlled by pin and also toggled by 0x300C[6] 1: Mirror controlled by 0x300C[6] Bit[1:0]: Analog control Changing these values is not recommended
0x3006	BRGAINH	0x44	RW	Blue and Red Channel Gain Most Significant Bits Bit[7:4]: BLUE[11:8] Refer to BGAIN (0x3001) for BLUE[7:0] Bit[3:0]: RED[11:8] Refer to RGAIN (0x3002) fore RED[7:0]
0x3007	GGAINH	0x40	RW	Green Channel Gain Most Significant Bits Bit[7:4]: GREEN[11:8] Refer to GGAIN (0x3003) for GREEN[7:0] Bit[3:2]: Not used Bit[1]: Debug timing option Changing this value is not recommended Bit[0]: Not used

table 7-1 system control registers (sheet 3 of 26)

address	register name	default value	R/W	description
0x3008	BLC	0x03	RW	Bit[7]: BLC trigger option 0: BLC will be triggered upon any change of the gain 1: BLC will be triggered when gain changes by 2x Bit[6]: BLC debug option Changing this value is not recommended Bit[5:4]: Digital timing control Changing these values is not recommended Bit[3]: BLC manual trigger Changing from 0 to 1 initiates the black level calibration for the next frame Bit[2]: BLC always on 0: BLC is triggered by gain change, format change or by register BLC[3] manually 1: Sensor calibrates black level for every frame Bit[1]: Initiate BLC upon power up or reset 0: Does not initiate BLC upon reset 1: Initiate BLC upon power up or reset Bit[0]: Initiate BLC upon format change 0: Does not initiate BLC when format changes 1: Initiate BLC when format changes
0x3009	SCTRL03	0x05	RW	TV Encoder Option on SCH Angle Bit[7:4]: SC for PAL mode Bit[3:0]: SC for NTSC mode
0x300A	PIDH	0x79	R	Product ID MSB
0x300B	PIDL	0x66	R	Product ID LSB
0x300C	SCTRL04	0x02	RW	Bit[7]: Vertical flip 0: Normal image 1: Vertically flipped image Bit[6]: Mirror 0: Normal image 1: Mirrored image Bit[5:3]: Not used Bit[2:1]: Maximum exposure time Maximum exposure time = (REND[15:0] – 1 – 2×SCTRL04[2:1])×t_{Row} Bit[0]: Not used
0x300D	VSOPT	0x34	RW	Not Used

table 7-1 system control registers (sheet 4 of 26)

address	register name	default value	R/W	description
0x300E	SCTRL05	0xE4	RW	Bit[7]: BLC debug control Changing this value is not allowed Bit[6:5]: Optical black row selection 00: Calibrate black level of blue/red row using blue/red optical black row, respectively 01: Calibrate black level of blue and red row using red optical black row 10: Calibrate black level of blue and red row using blue optical black row 11: Calibrate black level of blue/red row using blue/red optical black row, respectively Bit[4]: Analog circuit power down 0: Normal operating 1: Power down whole analog circuit Bit[3]: Sleep mode enable 0: Normal operating 1: Sleep Bit[2]: Double exposure in color and B/W mode Bit[1:0]: Drive capability select for the output pads 00: 1x 01: 2x 10: 3x 11: 4x
0x300F	AECH	0x00	RW	Bit[7:0]: AEC[15:8], refer to AECL (0x3010) for AEC[7:0] AEC[15:0] is the exposure time in unit of row period
0x3010	AECL	0x80	RW	Bit[7:0]: AEC[7:0], refer to AECL (0x300F) for AEC[15:8] AEC[15:0] is the Exposure Time in Unit of Row Period
0x3011	CLK	0x00	RW	Bit[7]: Debug control Changing this value is not recommended Bit[6]: Using input clock as pixel clock directly Changing this value is not recommended Bit[5:1]: System clock divider System clock is the PLL output clock divided by 2 × (CLK[5:0] + 1) Bit[0]: Special clock option

table 7-1 system control registers (sheet 5 of 26)

address	register name	default value	R/W	description
0x3012	SCTRL06	0x10	RW	Bit[7]: SRST 1: Initiates soft reset. All registers are set to factory default values after which the chip resumes normal operation. Bit[6:0]: Format options Changing these values is not recommended

table 7-1 system control registers (sheet 6 of 26)

address	register name	default value	R/W	description
0x3013	SCTRL07	0xBF	RW	Bit[7]: AEC speed selection 0: Normal mode 1: Fast mode Bit[6]: AGC/AEC control option Changing this value is not recommended Bit[5]: Banding filter enable 0: Disable, no restriction on exposure time 1: Enable, exposure time is restricted by n/100 or n/120 second, where n is integral Bit[4]: Banding filter option 0: Minimum exposure time is limited 1/100 or 1/120 second 1: Allow exposure time below 1/100 or 1/120 second in very bright condition to avoid over expose, in which case banding may appear Bit[3]: Sub-row exposure enable Refer to register LAECH (0x3030) and AECL(0x301F) for sub-row exposure time 0: Minimum exposure time is limited to one row period in AEC mode 1: Allow exposure time below one row period in AEC mode Bit[2]: Auto gain control (AGC) enable 0: Disable, gain is manually set by register GAIN (0x3000) 1: Enable, gain register GAIN (0x3000) is controlled by sensor AEC/AGC algorithm Bit[1]: AWB enable 0: Disable, AWB gain is manually set by register BGAIN (0x3001), RGAIN (0x3002), GGAIN (0x3003), BRGAINH (0x3006) and GGAINH (0x3007) 1: Enable, AWB gain register BGAIN (0x3001), RGAIN (0x3002), GGAIN (0x3003), BRGAINH (0x3006) and GGAINH (0x3007) are controlled by sensor AWB algorithm Bit[0]: Auto exposure control (AEC) enable 0: Disable, exposure is manually set by register AECH (0x300F) and AECL (0x3010) 1: Enable, exposure register AECH (0x300F) and AECL (0x3010) are controlled by sensor AEC/AGC algorithm

table 7-1 system control registers (sheet 7 of 26)

address	register name	default value	R/W	description
0x3014	SCTRL08	0x48	RW	Bit[7]: Debug mode Changing this registers is not recommended Bit[6:4]: Maximum gain 000: 2x 001: 4x 010: 8x 011: 16x 100: 32x 101: 64x 110: 128x 111: Not used Bit[3]: Analog control Changing this value is not recommended Bit[2:1]: Debug timing control Changing these values is not recommended Bit[0]: Debug mode Changing this value is not recommended
0x3015	SCTRL09	0x00	RW	Bit[7]: Night mode enable For digital output only 0: Disable 1: Enable, the sensor will insert dummy line to increase exposure time in low light condition automatically Bit[6:4]: Maximum number of frames can be inserted in night mode 000: No frame inserted 001: Insert maximum one frame 010: Insert maximum two frames 011: Insert maximum three frames 100: Insert maximum seven frames Others: Not allowed Bit[3:2]: Gain threshold to enter night mode 00: 2x 01: 4x 10: 8x 11: 16x Bit[1:0]: AGC[9:8] Refer to GAIN (0x3000) for AGC[7:0] Gain = (AGC[9] + 1) × (AGC[8] + 1) × (AGC[7] + 1) × (AGC[6] + 1) × (AGC[5] + 1) × (AGC[4] + 1) × (AGC[3:0]/16 + 1) AGC[7:0] is analog gain, AGC[9:8] is digital gain

table 7-1 system control registers (sheet 8 of 26)

address	register name	default value	R/W	description
0x3016	SCTRL10	0x06	RW	Bit[7:6]: AVSIZE[1:0] Array vertical output size Refer to register VSIZEINH (0x301A) for AVSIZE[9:2] Each digit count of AVSIZE[9:0] means one pixel Sensor vertical output size[1:0] Bit[5:4]: AHSIZE[1:0] Array horizontal output size Refer to register HSIZEINH (0x3018) for AHSIZE[9:2] Each digit count of AHSIZE[9:0] means one pixel Bit[3:2]: VSTART[1:0] Array vertical output start point Refer to register VSTARTH (0x3019) for VSTART[9:2] Each digit count of VSTART[9:0] means one row VREF start point[1:0] Bit[1:0]: HSTART[1:0] Array horizontal output start point Refer to register HSTARTH (0x3017) for HSTART[9:2] Each digit count of HSTART[9:0] means one pixel
0x3017	HSTARTH	0x23 (NTSC) 0x2E (PAL)	RW	Array Horizontal Output Start Point HSTART[9:2] Refer to SCTRL10[1:0] (0x3016) for HSTART[1:0] Each digit count of HSTART[9:0] means one pixel The maximum recommended value is 0x24 for NTSC
0x3018	HSIZEINH	0xA4 (NTSC) 0xC0 (PAL)	RW	Array Horizontal Output Size AHSIZE[9:2] Refer to SCTRL10[5:4] (0x3016) for AHSIZE[1:0] Each digit count of AHSIZE[9:0] means one pixel
0x3019	VSTARTH	0x01	RW	Array Vertical Output Start Point VSTART[9:2] Refer to SCTRL10[3:2] (0x3016) for VSTART[1:0] Each digit count of VSTART[9:0] means one row
0x301A	VSIZEINH	0x7B (NTSC) 0x90 (PAL)	RW	Array Vertical Output Size AVSIZE[9:2] Refer to SCTRL10[7:6] (0x3016) for AVSIZE[1:0] Each digit count of AVSIZE[9:0] means one pixel
0x301B	PSHFT	0x76	RW	Array Horizontal Output Delay One digit count means one pixel It is not recommended to change this register
0x301C	MIDH	0x7F	R	Manufacturer ID MSB
0x301D	MIDL	0xA2	R	Manufacturer ID LSB

table 7-1 system control registers (sheet 9 of 26)

address	register name	default value	R/W	description
0x301E	SCTRL11	0x11	RW	Bit[7]: Night mode timing option Should set to 1 when night mode is enabled 0: Do not latch dummy line number 1: Latch dummy line number by VSYNC Bit[6]: Debug mode Changing this value is not recommended Bit[5]: Analog debug mode Changing this value is not recommended Bit[4]: Initiate AEC/AGC algorithm when the sensor detects the change of light frequency 0: Does not adjust exposure when the light frequency change 1: Adjust exposure to right value when the light frequency changes Bit[3]: AEC/AGC algorithm selection 0: Average based algorithm 1: Histogram based algorithm Bit[2]: Debug mode Changing this value is not recommended Bit[1]: Night mode option when banding is enabled 0: Insert complete frame(s) 1: Insert incomplete frame(s) to double exposure time Bit[0]: Timing control Changing this value is not recommended
0x301F	LAECL	0x00	RW	Sub-row Exposure Time LAEC[7:0] Refer to LAECH (0x3030) for LAEC[15:8] Exposure time = Row length – LAEC[15:0] and the unit is pixel period
0x3020	SCTRL12	0x00	RW	Bit[7]: BDNUM50[4] Refer to BDNUM[7:4] (0x3021) for BDNUM50[3:0] BDNUM50[4:0] is equal to the integral part of frame period divided by 1/100 second Bit[6]: BDNUM60[4] Refer to BDNUM[3:0] (0x3021) for BDNUM60[3:0] BDNUM60[4:0] is equal to the integral part of frame period divided by 1/120 second Bit[5:0]: Banding options Changing these values is not recommended

table 7-1 system control registers (sheet 10 of 26)

address	register name	default value	R/W	description
0x3021	BDNUM	0x44	RW	Bit[7:4]: BDNUM50[3:0] Refer to SCTRL12[7] (0x3020) for BDNUM50[4] BDNUM50[4:0] is equal to the integral part of frame period divided by 1/100 second Bit[3:0]: BDNUM60[3:0] Refer to SCTRL12[6] (0x3020) for BDNUM60[4] BDNUM60[4:0] is equal to the integral part of frame period divided by 1/120 second
0x3022	SCTRL14	0x0D	RW	Analog Timing Control Changing this register is not recommended
0x3023	SCTRL15	0x00	RW	Analog Control Changing this register is not recommended
0x3024	WPT	0x4C	RW	Upper Limit of the Stable Luminance Range for Average-based AEC/AGC Algorithm
0x3025	BPT	0x40	RW	Lower Limit of the Stable Luminance Range for Average-based AEC/AGC Algorithm
0x3026	VPT	0x92	RW	Bit[7:4]: High nibble of the upper limit of fast AEC/AGC zone Bit[3:0]: High nibble of the lower limit of fast AEC/AGC zone
0x3027	SCTRL16	0xC1	RW	Bit[7]: Black sun cancellation enable 0: Disable 1: Enable Bit[6]: Debug mode Changing this value is not recommended Bit[5:4]: BLC debug mode Changing these values is not recommended Bit[3:0]: Internal field signal control Changing these values is not recommended
0x3028	SCTRL17	0x00	RW	Bit[7]: Not used Bit[6:1]: Debug control Changing these values is not recommended Bit[0]: Analog debug mode Changing this value is not recommended
0x3029	CSENDL	0x0C	RW	Bit[7:0]: CSEND[7:0] Line length Refer to CSENDH (0x302A) for CSEND[15:8] One digit count of CSEND[15:0] means one pixel

table 7-1 system control registers (sheet 11 of 26)

address	register name	default value	R/W	description
0x302A	CSENDH	0x03	RW	Bit[7:0]: CSEND[15:8] Line length Refer to CSENDH (0x3029) for CSEND[7:0] One digit count of CSEND[15:0] means one pixel
0x302B	RENDL	0x0C	RW	Bit[7:0]: REND[7:0] Frame length Refer to RENDH (0x302C) for REND[15:8] One digit count of REND[15:0] means one row
0x302C	RENDH	0x02	RW	Bit[7:0]: REND[15:8] Frame length Refer to RENDL (0x302B) for REND[7:0] One digit count of REND[15:0] means one row
0x302D	ADDVSL	0x00	RW	Bit[7:0]: ADDVS[7:0] Refer to ADDVSH (0x302E) for ADDVS[15:8] ADDVS[15:0] is the number of dummy rows inserted in night mode
0x302E	ADDVSH	0x00	RW	Bit[7:0]: ADDVS[15:8] Refer to ADDVSH(0x302D) for ADDVS[7:0] ADDVS[15:0] is the number of dummy rows inserted in night mode
0x302F	YAVG	0x00	RW	Luminance Average Value
0x3030	LAECH	0x00	RW	Bit[7:0]: LAEC[15:8] Sub-row exposure time Refer to LAECL (0x301F) for LAEC[7:0] Exposure time = Row length – LAEC[15:0], and the unit is pixel period
0x3031	HSIZEOH	0xA2 (NTSC) 0xC0 (PAL)	RW	Bit[7:0]: HSIZEO[9:2] Refer to SCTRL18[3:2] (0x3034) for HSIZEO[1:0] HSIZEO[9:0] is the horizontal size of the output image
0x3032	VSIZEOH	0x7B (NTSC) 0x90 (PAL)	RW	Bit[7:0]: VSIZEO[9:2] Refer to SCTRL18[1:0] (0x3034) for VSIZEO[1:0] VSIZEO[9:0] is the vertical size of the output image

table 7-1 system control registers (sheet 12 of 26)

address	register name	default value	R/W	description
0x3033	HVOFFS	0x40	RW	Bit[7:4]: Additional pixels on the left of the image that the array sends to the ISP, one digit count means one pixel. The maximum suggested setting for these register bits is 0x8 for NTSC. Bit[3:0]: Additional rows on top of the image that the array sends to the ISP, one digit count means one row.
0x3034	SCTRL18	0x00	RW	Bit[7:4]: Not used Bit[3:2]: HSIZEO[1:0] Refer to HSIZEOH (0x3031) for HSIZEO[9:2] HSIZEO[9:0] is the horizontal size of the output image Bit[1:0]: VSIZEO[1:0] Refer to VSIZEOH (0x3032) for VSIZEO[9:2] VSIZEO[9:0] is the vertical size of the output image
0x3035	SCTRL19	0x00	RW	Bit[7:0]: Array timing control Changing these values is not recommended
0x3036	SCTRL20	0x2F	RW	Bit[7:6]: Debug mode Changing these values is not recommended Bit[5:4]: Debug mode Changing these values is not recommended Bit[3:0]: Analog control Changing these values is not recommended
0x3037	SCTRL21	0x43	RW	Bit[7:0]: Timing control Changing these values is not recommended
0x3038	ACTRL1	0x00	RW	Bit[7]: Array horizontal readout start point selection 0: Pre-defined 1: Manually adjusted, refer to ACTRL17[6:5] (0x3048) Bit[6:4]: Analog control Changing these values is not recommended Bit[3:0]: Monitoring option for analog control
0x3039	ACTRL2	0x10	RW	Bit[7:0]: Analog control Changing these values is not recommended

table 7-1 system control registers (sheet 13 of 26)

address	register name	default value	R/W	description
0x303A	ACTRL3	0x00	RW	Bit[7:0]: Analog timing control Changing these values is not recommended
0x303B	ACTRL4	0x00	RW	Bit[7:0]: Analog timing control Changing these registers is not recommended
0x303C	ACTRL5	0x00	RW	Bit[7:0]: Analog timing control Changing these values is not recommended
0x303D	ACTRL6	0x28	RW	Bit[7:6]: Fixed analog gain for red and blue channel 00: 1.0x 01: 1.2x 10: 1.5x 11: 2.0x Bit[5:0]: Analog control Changing these values is not recommended
0x303E	ACTRL7	0x80	RW	Bit[7:2]: Analog control Changing these values is not recommended Bit[1:0]: Always G pre-gain 00: 1x 01: 1.125x 10: 1.25x 11: 1.5x
0x303F	ACTRL8	0x80	RW	Bit[7:0]: Analog control Changing these values is not recommended
0x3040	ACTRL9	0xCC	RW	Bit[7:0]: Analog control Changing these values is not recommended
0x3041	ACTRL10	0x04	RW	Bit[7:0]: Analog control Changing these values is not recommended
0x3042	ACTRL11	0x00	RW	Bit[7:6]: Analog timing control Changing these values is not recommended Bit[5:2]: Not used Bit[1]: Analog timing control Changing this value is not recommended Bit[0]: Not used

table 7-1 system control registers (sheet 14 of 26)

address	register name	default value	R/W	description
0x3043	ACTRL12	0x80	RW	Bit[7:5]: Analog control Changing these values is not recommended Bit[4]: Analog control Changing this value is not recommended Bit[3:1]: Not used Bit[1:0]: Analog timing control Changing this value is not recommended
0x3044	ACTRL13	0x74	RW	Bit[7:0]: Analog control Changing these values is not recommended
0x3045	ACTRL14	0x41	RW	Bit[7:0]: Analog control Changing these values is not recommended
0x3046	ACTRL15	0x0C	RW	Bit[7:0]: Analog timing control Changing these values is not recommended
0x3047	ACTRL16	0x0E	RW	Bit[7:0]: Analog control Changing these values is not recommended
0x3048	ACTRL17	0x80	RW	Bit[7]: Analog control Changing this value is not recommended Bit[6:5]: Analog control Array horizontal readout start point selection
0x3049	ACTRL18	0x64	RW	Bit[7:0]: Analog control Changing these values is not recommended
0x304A	SCTRL22	0xA0	RW	Bit[7:4]: Analog circuit control Bit[3]: Bypass internal regulator for DVDD 0: Enable internal regulator 1: Bypass internal regulator Bit[2:0]: Analog control Changing these values is not recommended
0x304B	ACTRL19	0x58	RW	Array Analog Circuit, Timing Control and Debug Mode Changing this register is not recommended
0x304C	ACTRL20	0x1A	RW	Bit[7:1]: Analog control Changing these values is not recommended Bit[0]: Not used

table 7-1 system control registers (sheet 15 of 26)

address	register name	default value	R/W	description
0x304D	ACTRL21	0x20	RW	Bit[7:0]: Analog control Changing these values is not recommended
0x304E	ACTRL22	0x95	RW	Bit[7:0]: Analog control Changing these values is not recommended
0x304F	ACTRL23	0x02	RW	Bit[7:0]: Analog control Changing these values is not recommended
0x3050	ACTRL24	0x1C	RW	Bit[7:0]: Analog control Changing these values is not recommended
0x3051	ACTRL25	0x03	RW	Bit[7:4]: Not used Bit[3:0]: Analog control Changing these values is not recommended
0x3052	SCTRL24	0x00	RW	Bit[7:6]: BD60[9:8] Refer to BD60ST (0x3055) for BD60[7:0] BD60[9:0] equals the 1/120 second divided by row period Bit[5:4]: BD50[9:8] Refer to BD50ST (0x3054) for BD50[7:0] BD50[9:0] equals the 1/100 second divided by row period Bit[3]: Analog control Changing this value is not recommended Bit[2]: DAC power down 0: Normal operating 1: Power down the DAC Bit[1]: Debug control Changing this value is not recommended Bit[0]: Analog control Changing this value is not recommended

table 7-1 system control registers (sheet 16 of 26)

address	register name	default value	R/W	description
0x3053	SCTRL25	0x03	RW	Bit[7]: Debug mode Changing this value is not recommended Bit[6]: Debug mode Bit[5]: DSP reset Bit[4:3]: Debug mode Changing this value is not recommended Bit[2]: VSYNC/HREF output selection 0: Normal VSYNC and HREF output 1: VSYNC and HREF are GPIOs, refer to register SCTRL40[1:0] (0x3065) Bit[1]: YAVG (0x302F) selection 0: YAVG from DSP 1: YAVG from array Bit[0]: Internal field signal control Changing this value is not recommended
0x3054	BD50ST	0x9C	RW	BD50[7:0] Refer to SCTRL24[5:4] (0x3052) for BD50[9:8] BD50[9:0] equals the 1/100 second divided by row period
0x3055	BD60ST	0x83	RW	BD60[7:0] Refer to SCTRL24[7:6] (0x3052) for BD60[9:8] BD60[9:0] equals the 1/120 second divided by row period
0x3056~ 0x3059	NOT USED	–	–	Not Used
0x305A	BLCCTRL0	0x00	RW	Bit[7:6]: Analog timing control Changing these values is not recommended Bit[5:3]: Analog control Changing these values is not recommended Bit[2]: YAVG (0x202F) selection for analog output 0: Frame average 1: Field average Bit[1:0]: BLC debug control Changing these values is not recommended
0x305B	ERNG	0x84	RW	Bit[7:4]: TV field reset option Bit[3:0]: AEC/AGC stable range adjustment at high temperature When BLC can not cancel all dark current at high temperature, the AEC/AGC stable range will change to (BPT[7:0] – ERNG[3:0], WPT[7:0] + ERNG[3:0])

table 7-1 system control registers (sheet 17 of 26)

address	register name	default value	R/W	description
0x305C	SCTRL32	0x55	RW	Bit[7:0]: Lent_rst[7:0] Frame sync line reset point
0x305D	BLCCTRL1	0x02	RW	Bit[7:4]: BLC debug control Changing these values is not recommended Bit[3]: Manual BLC bias for AWB 0: AWB subtracts black level before applying gain 1: AWB subtracts AWBBIAS (0x3066) before applying gain Bit[2]: DSP timing control Changing this value is not recommended Bit[1]: BLC update option 0: If I2C is occupied by an external device when BLC is updating window, BLC does not update 1: BLC always updates Bit[0]: Debug control Changing this value is not recommended
0x305E	BLCCTRL2	0x00	RW	Bit[7:6]: Analog control Changing these values is not recommended Bit[5:4]: Not used Bit[3:2]: Analog timing control Changing these values is not recommended Bit[1:0]: Not used
0x305F	MLEN	0x04	RW	Bit[7]: Line length manual adjustment enable CSENDH (0x302A) and CSENDL (0x3029) Using pre-defined line length for analog output is recommended 0: Line length is pre-defined 1: Line length is manually set by register Bit[6]: Frame length manual adjustment enable RENDH (0x302C) and RENDL (0x302B) Using pre-defined line length for analog output is recommended 0: Frame length is pre-defined 1: Frame length is manually set by register Bit[5:4]: Data path control for analog output Changing these values is not recommended Bit[3:0]: Gain compensation when entering sub-row exposure

table 7-1 system control registers (sheet 18 of 26)

address	register name	default value	R/W	description
0x3060~ 0x3061	NOT USED	–	–	Not Used
0x3062	SCTRL38	0x01	RW	Bit[7:4]: Analog control Changing these values is not recommended Bit[3]: Video feedback enable 0: Normal operating mode 1: Video feedback mode Bit[2]: IO direction control of FSIN pin 0: Input 1: Output Bit[1]: IO direction control of VICK, VI_[5:2] 0: Input 1: Output Bit[0]: Analog option Changing this value is not recommended
0x3063	AVGZN	–	R	Average Value of the Zone Specified by ACTRL1[3:0] (0x3038)
0x3064	SCTRL39	0x20	RW	Bit[7:5]: Analog control Changing these values is not recommended Bit[4]: Analog control option Changing this value is not recommended Bit[3]: Horizontal sub-sample enable 0: Full resolution 1: Sub-sample for QVGA Bit[2]: Vertical sub-sample enable 0: Full resolution 1: Sub-sample for QVGA Bit[1:0]: Debug mode Changing these values is not recommended
0x3065	SCTRL40	0x04	RW	Bit[7:6]: TV encoder field signal Changing these values is not recommended Bit[5:4]: Special DVP timing for ClockGen 00: Normal operating 01: Master device in the ClockGen system 10: Slave device in the ClockGen system 11: Not used Bit[3]: Test mode Changing this value is not recommended Bit[2]: Average option Changing this value is not recommended Bit[1]: GPIO register bit of pin HREF Bit[0]: GPIO register bit of pin VSYNC

table 7-1 system control registers (sheet 19 of 26)

address	register name	default value	R/W	description
0x3066	AWBBIAS	0x00	RW	Manual Black Level Bias for AWB
0x3067	BLC0	0xD4	RW	Bit[7]: BLC enable 0: Disable 1: Enable Bit[6]: BLC control Changing this value is not recommended Bit[5]: Clear black level compensation before update 0: Do not clear black level compensation before update 1: Clear black level compensation before update Bit[4]: BLC control Changing this value is not recommended Bit[3:0]: Target black level in 8-bit scale
0x3068	BLC1	0x92	RW	Bit[7]: BLC control option Changing this value is not recommended Bit[6]: BLC control in B/W mode Changing this value is not recommended Bit[5]: BLC control option Changing this value is not recommended Bit[4:0]: BLC control Changing these values is not recommended
0x3069	BLC2	0x60	RW	BLC Control Changing this register is not recommended
0x306A	HDLY1	0x18	RW	HSYNZDY Start Point Changing this register is not recommended
0x306B	HDLY2	0x20	RW	HSYNZDY End Point Changing this register is not recommended
0x306C	HFIELD	0x78	RW	HFLD[9:2] Refer to SCTRL41[5:4] (0x306E) for HFLD[1:0] HFLD[9:0] is the horizontal timing control for TV field Changing this register is not recommended
0x306D	VFIELD	0x80	RW	VFLD[9:2] Refer to SCTRL41[7:6] (0x306E) for VFLD[1:0] VFLD[9:0] is the vertical timing control for TV field Changing this register is not recommended

table 7-1 system control registers (sheet 20 of 26)

address	register name	default value	R/W	description
0x306E	SCTRL41	0xD0	RW	Bit[7:6]: VFLD[1:0], refer to VFIELD (0x306D) for VFLD[9:2] VFLD[9:0] is the vertical timing control for TV field Changing this register is not recommended Bit[5:4]: HFLD[1:0], refer to HFIELD (0x306C) for HFLD[9:2] HFLD[9:0] is the horizontal timing control for TV field Changing this values is not recommended Bit[3:0]: Not used
0x306F	SCTRL42	0x53	RW	Bit[7]: Reset internal timing upon mode change 0: Does not reset 1: Reset internal timing when sensor working mode changes Bit[6:4]: Analog timing control Changing these values is not recommended Bit[3]: Debug mode Changing this value is not recommended Bit[2]: BLC reset 0: Normal operation 1: Reset Bit[1:0]: Debug mode Changing these values is not recommended
0x3070~ 0x307E	5060DET	–	RW	Control Registers for 50/60 Hz Auto Detection Setting depends on input clock frequency, contact your local OmniVision FAE for the setting
0x307F	NOT USED	–	–	Not Used
0x3080	AVGRH	–	R	AVGR[9:2] Refer to AVGL[1:0] (0x3084) for AVGR[1:0] AVGL[9:0] is the black pixel average of red channel
0x3081	AVGBH	–	R	AVGB[9:2] Refer to AVGL[3:2] (0x3084) for AVGB[1:0] AVGB[9:0] is the black pixel average of blue channel
0x3082	AVGGRH	–	R	AVGGR[9:2] Refer to AVGL[5:4] (0x3084) for AVGGR[1:0] AVGGR[9:0] is the black pixel average of green-in-red channel
0x3083	AVGGBH	–	R	AVGGB[9:2] Refer to AVGL[7:6] (0x3084) for AVGGB[1:0] AVGGB[9:0] is the black pixel average of green-in-blue channel

table 7-1 system control registers (sheet 21 of 26)

address	register name	default value	R/W	description
0x3084	AVGL	–	R	Bit[7:6]: AVGGB[1:0], refer to AVGGBH (0x3083) for AVGGB[9:2] AVGGB[9:0] is the black pixel average of green-in-blue channel Bit[5:4]: AVGGR[1:0], refer to AVGGRH (0x3082) for AVGGR[9:2] AVGGR[9:0] is the black pixel average of green-in-red channel Bit[3:2]: AVGB[1:0], refer to AVGBH (0x3081) for AVGB[9:2] AVGB[9:0] is the black pixel average of blue channel Bit[1:0]: AVGR[1:0], refer to AVGRH (0x3080) for AVGR[9:2] AVGR[9:0] is the black pixel average of red channel
0x3085	BLC1	–	R	BLCHTMNT[10:3] Refer to BLC2[2:0] (0x3086) for BLCHTMNT[2:0] BLCHTMNT[10:0] is the black pixel average used for analog offset adjustment at high temperature
0x3086	BLC2	–	R	Bit[7:3]: Not used Bit[2:0]: BLCHTMNT[2:0], refer to BLC1 (0x3085) for BLCHTMNT[10:3] BLCHTMNT[10:0] is the black pixel average used for analog offset adjustment at high temperature
0x3087	HVPAD	0x40	RW	Bit[7:4]: Additional pixels on the right of the image that the array sends to the ISP, one digit count means one pixel. Bit[3:0]: Additional rows on the bottom of the image that the array sends to the ISP, one digit count means one row.
0x3088	HOFFOUT	0x00	RW	HOFFOUT[9:2] Refer to SCTRL45[3:2] (0x308A) for HOFFOUT[1:0] HOFFOUT[9:0] is the horizontal offset of the DSP input image relative to the array output image, one digital count means one pixel
0x3089	VOFFOUT	0x00	RW	VOFFOUT[9:2] Refer to SCTRL45[1:0] (0x308A) VOFFOUT[9:0] is the Vertical offset of the DSP input image relative to the array output image, one digital count means one row

table 7-1 system control registers (sheet 22 of 26)

address	register name	default value	R/W	description
0x308A	SCTRL45	0x00	RW	Bit[7:4]: Not used Bit[3:2]: HOFFOUT[1:0], refer to HOFFOUT (0x3088) for HOFFOUT[9:2] HOFFOUT[9:0] is the horizontal offset of the DSP input image relative to the array output image, one digital count means one pixel Bit[1:0]: VOFFOUT[1:0], refer to VOFFOUT (0x3089) for VOFFOUT[9:2] VOFFOUT[9:0] is the vertical offset of the DSP input image relative to the array output image, one digital count means one row
0x308B	BPLTH1	0x50	RW	Luminance Threshold for Dark Pixel Pixel with luminance smaller than BPLTH1 is counted as dark pixel, used in histogram based AEC/AGC control
0x308C	BPLTH2	0x20	RW	Luminance Threshold for Very Dark Pixel Pixel with luminance smaller than BPLTH2 is counted as very dark pixel, used in histogram based AEC/AGC control
0x308D	WPTH1	0x80	RW	Bright Pixel Luminance Threshold Pixel with luminance greater than WPTH1 is counted as bright pixel, used in histogram based AEC/AGC control
0x308E	WPTH2	0xD0	RW	Very Bright Pixel Luminance Threshold Pixel with luminance greater than WPTH2 is counted as very bright pixel, used in histogram based AEC/AGC control
0x308F	BPCNT1	0x90	RW	Dark Pixel Percentage Threshold When the percentage of dark pixel is greater than BPCNT1, AEC/AGC will increase the exposure/gain by normal step 0x7F is normalized as 100% for OV7962 TV mode
0x3090	BPCNT2	0x80	RW	Very Dark Pixel Percentage Threshold When the percentage of dark pixel is greater than BPCNT2, AEC/AGC will increase the exposure/gain by big step 0x7F is normalized as 100% for OV7962 TV mode
0x3091	WPCNT1	0x80	RW	Bright Pixel Percentage Threshold When the percentage of bright pixel is greater than WPCNT1, AEC/AGC will reduce the exposure/gain by normal step 0x7F is normalized as 100% for OV7962 TV mode

table 7-1 system control registers (sheet 23 of 26)

address	register name	default value	R/W	description
0x3092	WPCNT2	0xA0	RW	Very Bright Pixel Percentage Threshold when the percentage of bright pixel is greater than WPCNT2, AEC/AGC will reduce the exposure/gain by big step 0x7F is normalized as 100% for OV7962 TV mode
0x3093	YEN0	0x00	RW	Bit[7:0]: I/O direction control of Y[9:2] pin 0: Input 1: Output
0x3094	SCTRL46	0x00	RW	Bit[7]: Field signal option Changing this value is not recommended Bit[6]: HFIELD, VFIELD manual mode enable Bit[5]: Group register write enable 0: Normal register write mode 1: Group register write mode in which the sensor holds the write until the start of next frame after the group write command is initiated Bit[4]: I/O direction control of HREF/VI_7 pin 0: Input 1: Output Bit[3]: I/O direction control of PCLK pin 0: Input 1: Output Bit[2]: I/O direction control of VSYNC/VI_6 pin 0: Input 1: Output Bit[1:0]: I/O direction control of Y[1:0] / VI_[1:0] 0: Input 1: Output
0x3095	SCTRL47	0x1C	RW	Bit[7]: Analog control Changing this value is not recommended Bit[6:5]: PLL pre-divider 00: /1 01: /1.5 10: /2 11: /3 Bit[4:0]: PLL multiplier Multiplier = 32 – SCTRL47[4:0] Changing PLL configuration is not recommended for TV output application

table 7-1 system control registers (sheet 24 of 26)

address	register name	default value	R/W	description
0x3096	SCTRL48	0x00	RW	Bit[7]: Bypass PLL 0: Enable PLL 1: Bypass PLL including the PLL pre-divider and output divider Bit[6:5]: PLL output divider Divider = SCTRL48[6:5] + 1 Bit[4:3]: Analog control Changing these values is not recommended Bit[2]: PLL reset 0: Normal operating 1: Reset Bit[1]: Debug control Changing these values is not recommended Bit[0]: Reset PLL upon system reset
0x3097	VSFT	0x16	RW	Array Vertical Output Delay One digit count means one row
0x3098	H2SFT	0x00	RW	Debug Control Changing this register is not recommended
0x3099	BLCGBH	–	R	BLCGB[9:2] Refer to BLCL[7:6] (0x309D) for BLCGB[1:0] BLCGB[9:0] is the black level compensation of green-in-blue channel, automatically calculated by sensor when BLC is enabled
0x309A	BLCGRH	–	R	BLCGR[9:2] Refer to BLCL[5:4] (0x309D) for BLCGR[1:0] BLCGR[9:0] is the black level compensation of green-in-red channel, automatically calculated by sensor when BLC is enabled
0x309B	BLCBH	–	R	BLCB[9:2] Refer to BLCL[3:2] (0x309D) for BLCB[1:0] BLCB[9:0] is the black level compensation of blue channel, automatically calculated by sensor when BLC is enabled
0x309C	BLCRH	–	R	BLCR[9:2] Refer to BLCL[1:0] (0x309D) for BLCR[1:0] BLCL[9:0] is the black level compensation of red channel, automatically calculated by sensor when BLCL is enabled

table 7-1 system control registers (sheet 25 of 26)

address	register name	default value	R/W	description
0x309D	BLCL	–	R	Bit[7:6]: BLCR[1:0], refer to BLCRH (0x309C) for BLCR[9:2] BLCR[9:0] is the black level compensation of red channel, automatically calculated by sensor when BLC is enabled Bit[5:4]: BLCB[1:0], refer to BLCBH (0x309B) for BLCB[9:2] BLCB[9:0] is the black level compensation of blue channel, automatically calculated by sensor when BLC is enabled Bit[3:2]: BLCGR[1:0], refer to BLCGRH (0x309A) for BLCGR[9:2] BLCGR[9:0] is the black level compensation of green-in-red channel, automatically calculated by sensor when BLC is enabled Bit[1:0]: BLCGB[1:0], refer to BLCGBH (0x3099) for BLCGB[9:2] BLCGB[9:0] is the black level compensation of green-in-blue channel, automatically calculated by sensor when BLC is enabled
0x309E	BLCULMT	0xFF	RW	Upper Threshold of Black Pixel Average When the average is greater than this threshold, analog offset will increase for proper black level calibration
0x309F	BLCLLMT	0x10	RW	Lower Threshold of Black Pixel Average When the average is less than this threshold, analog offset will decrease for proper black level calibration
0x30A0~ 0x30EB	NOT USED	–	–	Not Used
0x30EC	SCTRL50	0x21	RW	Bit[7]: Light frequency auto detection enable 0: Light frequency is set by register SCTRL50[6] manually 1: Automatically detect the light frequency Bit[6]: Manual light frequency selection 0: 60Hz 1: 50Hz Bit[5]: Analog option Changing this value is not recommended Bit[4:3]: Not used Bit[2:0]: Analog timing control Changing values is not recommended
0x30EE	SCTRL51	0x00	RW	Command Register for Group Register Write Function

table 7-1 system control registers (sheet 26 of 26)

address	register name	default value	R/W	description
0x30EF	OTPCTRL	0x00	RW	Control Registers for OTP Writing 0x55 to this register will cause the sensor to load OTP content to register 0x30F0~0x30FF Writing 0xAA to this register will cause the sensor to program the value of register 0x30F0~0x30FF to OTP memory
0x30F0~ 0x30FF	OTPBUF	0x00	RW	Register Buffer to Access OTP Memory

table 7-2 format control (sheet 1 of 2)

address	register name	default value	R/W	description
0x4300	FMT CTRL	0x40	RW	Bit[7]: Reserved Bit[6:0]: fmt_ctrl RAW: fmt_ctrl00[6:0]=0x00: bgbg..../grgr... fmt_ctrl00[6:0]=0x01: gbgb..../rgrg... fmt_ctrl00[6:0]=0x02: grgr..../bgbg... fmt_ctrl00[6:0]=0x03: rgrg..../gbgb... RGB565: fmt_ctrl00[6:0]=0x10: {r[4:0],g[5:3],2'b00},{g[2:0],b[4:0], 2'b00},... fmt_ctrl00[6:0]=0x11: {b[4:0],g[5:3],2'b00},{g[2:0],r[4:0], 2'b00},... RGB666: fmt_ctrl00[6:0]=0x20: {r[5:0],g[5:3],1'b0},{g[2:0],b[5:0],1'b0}... fmt_ctrl00[6:0]=0x21: {b[5:0],g[5:3],1'b0},{g[2:0],r[5:0],1'b0}... YUV422: fmt_ctrl00[6:0]=0x30: yuyvyuyv... fmt_ctrl00[6:0]=0x31: yvyuyvyu... fmt_ctrl00[6:0]=0x32: uyvyuyvy... fmt_ctrl00[6:0]=0x33: vyuyvyuy... YUV444: fmt_ctrl00[6:0]=0x40: yuvyuv... fmt_ctrl00[6:0]=0x41: yvuyvu.... fmt_ctrl00[6:0]=0x42: uyvuyv... fmt_ctrl00[6:0]=0x43: uvyuvy... fmt_ctrl00[6:0]=0x44: vyuvyu... fmt_ctrl00[6:0]=0x45: vuyvuy...

table 7-2 format control (sheet 2 of 2)

address	register name	default value	R/W	description
0x4600	VFIFO CTRL0	0x7D (NTSC) 0x25 (PAL)	RW	Bit[7:0]: fifo_sh_p_cal_o[7:0]
0x4601	VFIFO CTRL1	0x03 (NTSC) 0x04 (PAL)	RW	Bit[7:5]: Reserved Bit[4]: fifo_start_size[8] Bit[3]: Reserved Bit[2:0]: fifo_sh_p_cal_o[10:8]
0x4602	VFIFO CTRL2	0x0D	RW	Bit[7]: vfifo_full_clear Bit[6:0]: fifo_sh_l_cal_o
0x4603	VFIFO CTRL3	0x02	RW	Bit[7:0]: fifo_start_size[7:0]
0x46C0	VSUB2 CTRL	0x01	RW	Bit[7:4]: Not used Bit[3]: even_pol Bit[2]: all_odd Bit[1]: all_even Bit[0]: field_sel

table 7-3 DVP control (sheet 1 of 4)

address	register name	default value	R/W	description
0x4700	SHP MAN	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: sh_p_man[12:8]
0x4701	SHP MAN	0x00	RW	Bit[7:0]: sh_p_man[7:0]
0x4702	SHL MAN	0x00	RW	Bit[7]: Reserved Bit[6:0]: sh_l_man
0x4703	SVL MAN	0x02	RW	Bit[7:0]: v_l_man
0x4704	SVP MAN	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: sv_p_man[12:8]
0x4705	SVP MAN	0x00	RW	Bit[7:0]: sv_p_man[7:0]
0x4706	HVP MAN	0x02	RW	Bit[7:5]: Reserved Bit[4:0]: hv_p_man[12:8]
0x4707	HVP MAN	0x88	RW	Bit[7:0]: hv_p_man[7:0]
0x4708	HVL MAN	0x0F	RW	Bit[7:0]: hv_l_man
0x4709	VSL MAN	0x04	RW	Bit[7:0]: vs_l_man
0x470A	LL VSP MAN	0x00	RW	Bit[7:6]: Reserved Bit[5]: ll_man[16] Bit[4:0]: vs_p_man[12:8]

table 7-3 DVP control (sheet 2 of 4)

address	register name	default value	R/W	description
0x470B	VSP MAN	0x01	RW	Bit[7:0]: vs_p_man[7:0]
0x470C	LL MAN	0x03	RW	Bit[7:0]: ll_man[15:8]
0x470D	LL MAN	0x0C	RW	Bit[7:0]: ll_man[7:0]
0x470E	CCIR CTRL	0x04	RW	Bit[7]: ccir_f_sel Bit[6]: ccir_v_sel Bit[5:0]: ccir_f_num
0x470F	VREF OFFSET	0x01	RW	Bit[7:4]: vref_end_offset Bit[3:0]: vref_offset
0x4710	VREF ADJ	0x00	RW	Bit[7:4]: vref_end_adj Bit[3:0]: vref_st_adj
0x4711	PADL CNT	0x00	RW	Bit[7:0]: padl_cnt
0x4712	PADR CNT	0x00	RW	Bit[7:0]: padr_cnt
0x4713	VREF ST	0x0A	RW	Bit[7:0]: vref_st[7:0]
0x4714	VREF END	0x00	RW	Bit[7:0]: vref_end[7:0]
0x4715	VREF ENDST	0x10	RW	Bit[7:4]: vref_end[11:8] Bit[3:0]: vref_st[11:8]
0x4716	FREF ST	0x00	RW	Bit[7:0]: fref_st[7:0]
0x4717	FIELDVST FREFST	0x11	RW	Bit[7:4]: field_vst[11:8] Bit[3:0]: fref_st[11:8]
0x4718	FIELD VST	0x00 (NTSC) 0x2C (PAL)	RW	Bit[7:0]: field_vst[7:0]
0x4719	FIELD HST	0x21 (NTSC) 0x3F (PAL)	RW	Bit[7:0]: field_hst[7:0]
0x471A	FIELD HST	0x02	RW	Bit[7:0]: field_hst[15:8]
0x471B	DVP CTRL00	0x00 (NTSC) 0xA0 (PAL)	RW	Bit[7:6]: Reserved Bit[5]: field_pol Bit[4]: fmt_chg_reg Bit[3]: tog_hs_en Bit[2]: tog_blk_en Bit[1]: retime_en Bit[0]: hsync_en_o
0x471C	DVP CTRL01	0x04	RW	Bit[7:3]: Reserved Bit[2]: frmae_1st_en Bit[1]: ll_man_en Bit[0]: sh_man_en

table 7-3 DVP control (sheet 3 of 4)

address	register name	default value	R/W	description
0x471D	DVP CTRL02	0x00	RW	Bit[7:6]: Reserved Bit[5]: vs_man_en Bit[4]: hv_man_en Bit[3]: sv_man_en Bit[2]: vsync_sel1_clr Bit[1]: vsync_sel2 Bit[0]: vsync_sel1
0x471E	DVP CTRL03	0x19	RW	Bit[7:5]: Reserved Bit[4]: sof_dcnt_dis Bit[3]: sof_lat_dis Bit[2]: low_long Bit[1]: pclk_div_man_en Bit[0]: pclk_div_en
0x471F	PCLK DIV MAN	0x01	RW	Bit[7:6]: Reserved Bit[5:0]: pclk_div_man
0x4720	DVP CTRL04	0x00	RW	Bit[7]: sync_code_sel Bit[6]: f_pol Bit[5]: f_value Bit[4]: fix_f Bit[3]: blk_sel1 Bit[2]: blk_sel0 Bit[1]: no_clip Bit[0]: ccir656_en
0x4721	FS	0xAB	RW	Bit[7:0]: FS
0x4722	FE	0xB6	RW	Bit[7:0]: FE
0x4723	LS	0x80	RW	Bit[7:0]: LS
0x4724	LE	0x9D	RW	Bit[7:0]: LE
0x4725	TOG01	0x09	RW	Bit[7:5]: Reserved Bit[4]: uv_first Bit[3:2]: tog0[9:8] Bit[1:0]: tog1[9:8]
0x4726	TOG0	0xAA	RW	Bit[7:0]: tog0[7:0]
0x4727	TOG1	0x55	RW	Bit[7:0]: tog1[7:0]
0x4728	DVP CTRL05	0x20	RW	Bit[7:6]: Reserved Bit[5]: pclk_pol Bit[4]: gate_l_clk_en Bit[3]: gate_vsync_en Bit[2]: gate_href_en Bit[1]: href_pol Bit[0]: vsync_pol

table 7-3 DVP control (sheet 4 of 4)

address	register name	default value	R/W	description
0x4729	DVP CTRL06	0x00	RW	Bit[7:5]: Reserved Bit[4]: toggle_en Bit[3]: href_lo_keep Bit[2]: tst_en Bit[1]: tst_md Bit[0]: tst_bit8
0x472A	TOGGLE DATA0	0xAA	RW	Bit[7:0]: toggle_data0[7:0]
0x472B	DVP CTRL07	0xC9	RW	Bit[7:6]: dvp_clip_max[9:8] Bit[5:4]: dvp_clip_min[9:8] Bit[3:2]: toggle_data1[9:8] Bit[1:0]: toggle_data0[9:8]
0x472C	TOGGLE DATA1	0x55	RW	Bit[7:0]: toggle_data1[7:0]
0x472D	DVP CTRL08	0x00	RW	Bit[7]: Reserved Bit[6]: dvp_clip_en Bit[5]: dvp_all_zero Bit[4]: dvp_rs_two Bit[3]: dvp_rs_one Bit[2]: dvp_h Bit[1]: dvp_l Bit[0]: data_order
0x472E	CLIP MAX	0xFF	RW	Bit[7:0]: dvp_clip_max[7:0]
0x472F	CLIP MIN	0x00	RW	Bit[7:0]: dvp_clip_min[7:0]

table 7-4 ISP control (sheet 1 of 3)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0x4F	RW	ISP Control 00 Bit[7]: LENC correction enable 0: Disable 1: Enable Bit[6]: Gamma (in YUV domain) enable 0: Disable 1: Enable Bit[5]: RAW gamma enable 0: Disable 1: Enable Bit[4]: Debug control Changing this value is not recommended Bit[3]: De-noise enable 0: Disable 1: Enable Bit[2]: Black pixel cancellation enable 0: Disable 1: Enable Bit[1]: White pixel cancellation enable 0: Disable 1: Enable Bit[0]: Color interpolation (CIP) enable 0: Disable 1: Enable

table 7-4 ISP control (sheet 2 of 3)

address	register name	default value	R/W	description
0x5001	ISP CTRL01	0x4F	RW	ISP Control 01 Bit[7]: Special digital effects (SDE) enable 0: Disable 1: Enable Bit[6]: Auto color saturation adjust enable 0: Disable 1: Enable Bit[5]: Vertical scaling enable 0: Disable 1: Enable Bit[4]: Horizontal scaling enable 0: Disable 1: Enable Bit[3]: Auto contrast enable 0: Disable 1: Enable Bit[2]: UV average enable 0: Disable 1: Enable Bit[1]: Color matrix enable 0: Disable 1: Enable Bit[0]: Auto white balance (AWB) enable 0: Disable 1: Enable
0x5002	RSVD	–	–	Reserved
0x5003	ISP CTRL03	0x08	RW	ISP Control 03 Bit[7]: Pad in buffer control enable 0: Buffer control boundary padded external 1: Buffer control pad boundary internal Bit[6:4]: Reserved Bit[3]: YUV to YCbCr enable 0: Disable 1: Enable Bit[2:1]: Reserved Bit[0]: Color bar test pattern enable 0: Disable 1: Enable
0x5004	ISP CTRL04	0x00	RW	ISP Control 04 Bit[7:3]: Reserved Bit[2]: Bar move enable 0: Disable 1: Enable Bit[1:0]: Color bar style

table 7-4 ISP control (sheet 3 of 3)

address	register name	default value	R/W	description
0x5005	ISP CTRL05	0xDC	RW	ISP Control 05 Bit[7]: Raw gamma option 1 0: Does not add back BLC bias after raw gamma correction 1: Adds back BLC bias after raw gamma correction Bit[6]: Raw gamma option 2 0: Raw gamma applied on input data directly regardless of the black level 1: Subtract black level before applying raw gamma Bit[5]: UV average old style enable 0: Disable 1: Enable Bit[4]: Advanced AWB option 1 0: Do not subtract black level 1: Subtract black level before statistics and apply gain Bit[3]: Lens correction option 1 0: Does not add back BLC bias after lens correction 1: Adds back BLC bias after lens correction Bit[2]: Lens correction option 2 0: Lens correction applied on input data directly regardless of the black level 1: Subtract black level before applying lens correction Bit[1:0]: Reserved
0x5040~ 0x5056	RSVD	–	–	Reserved

table 7-5 LENC control (sheet 1 of 4)

address	register name	default value	R/W	description
0x5100	LENC RED X0	0x04	RW	Bit[7:2]: Not used Bit[1:0]: red_x0[9:8] X coordinate of the lens optical center for red channel relative to the left-top corner of the ISP input image Range is 0 ~ 2047
0x5101	LENC RED X0	0x0C	RW	Bit[7:0]: red_x0[7:0] X coordinate of the lens optical center for red channel relative to the left-top corner of the ISP input image Range is 0 ~ 2047
0x5102	LENC RED Y0	0x03	RW	Bit[7:2]: Not used Bit[1:0]: red_y0[9:8] Y coordinate of the lens optical center for red channel relative to the left-top corner of the ISP input image Range is 0 ~ 1535
0x5103	LENC RED Y0	0x06	RW	Bit[7:0]: red_y0[7:0] Y coordinate of the lens optical center for red channel relative to the left-top corner of the ISP input image Range is 0 ~ 1535
0x5104	LENC RED A1	0x22	RW	LENC Control 04 Bit[7]: Not used Bit[6:0]: red_a1[6:0] Composed of the first group of factors used in the LENC correction of the red color channels
0x5105	LENC RED A2	0x07	RW	LENC Control 05 Bit[7:4]: Not used Bit[3:0]: red_a2[3:0] Composed of the first group of factors used in the LENC correction of the red color channels
0x5106	LENC RED B1	0xC2	RW	LENC Control 06 Bit[7:0]: red_b1[7:0] Composed of the second group of factors used in the LENC correction of the red color channels
0x5107	LENC RED B2	0x08	RW	LENC Control 07 Bit[7:4]: Not used Bit[3:0]: red_b2[3:0] Composed of the second group of factors used in the LENC correction of the red color channels

table 7-5 LENC control (sheet 2 of 4)

address	register name	default value	R/W	description
0x5108	LENC GREEN X0	0x04	RW	Bit[7:2]: Not used Bit[1:0]: green_x0[9:8] X coordinate of the lens optical center for green channel relative to the left-top corner of the ISP input image Range is 0 ~ 2047
0x5109	LENC GREEN X0	0x0C	RW	Bit[7:0]: green_x0[7:0] X coordinate of the lens optical center for green channel relative to the left-top corner of the ISP input image Range is 0 ~ 2047
0x510A	LENC GREEN Y0	0x03	RW	Bit[7:2]: Not used Bit[1:0]: green_y0[9:8] Y coordinate of the lens optical center for green channel relative to the left-top corner of the ISP input image Range is 0 ~ 1535
0x510B	LENC GREEN Y0	0x06	RW	Bit[7:0]: green_y0[7:0] Y coordinate of the lens optical center for green channel relative to the left-top corner of the ISP input image Range is 0 ~ 1535
0x510C	LENC GREEN A1	0x22	RW	LENC Control 12 Bit[7]: Not used Bit[6:0]: green_a1[6:0] Composed of the first group of factors used in the LENC correction of the green color channels
0x510D	LENC GREEN A2	0x07	RW	LENC Control 13 Bit[7:4]: Not used Bit[3:0]: green_a2[3:0] Composed of the first group of factors used in the LENC correction of the green color channels
0x510E	LENC GREEN B1	0xC2	RW	LENC Control 14 Bit[7:0]: green_b1[7:0] Composed of the second group of factors used in the LENC correction of the green color channels
0x510F	LENC GREEN B2	0x08	RW	LENC Control 15 Bit[7:4]: Not used Bit[3:0]: green_b2[3:0] Composed of the second group of factors used in the LENC correction of the green color channels

table 7-5 LENC control (sheet 3 of 4)

address	register name	default value	R/W	description
0x5110	LENC BLUE X0	0x04	RW	Bit[7:2]: Not used Bit[1:0]: blue_x0[9:8] X coordinate of the lens optical center for blue channel relative to the left-top corner of the ISP input image Range is 0 ~ 2047
0x5111	LENC BLUE X0	0x0C	RW	Bit[7:0]: blue_x0[7:0] X coordinate of the lens optical center for blue channel relative to the left-top corner of the ISP input image Range is 0 ~ 2047
0x5112	LENC BLUE Y0	0x03	RW	Bit[7:4]: Not used Bit[3:0]: blue_y0[11:8] Y coordinate of the lens optical center for blue channel relative to the left-top corner of the ISP input image Range is 0 ~ 1535
0x5113	LENC BLUE Y0	0x06	RW	Bit[7:0]: blue_y0[7:0] Y coordinate of the lens optical center for blue channel relative to the left-top corner of the ISP input image Range is 0 ~ 1535
0x5114	LENC BLUE A1	0x22	RW	LENC Control 20 Bit[7]: Not used Bit[6:0]: blue_a1[6:0] Composed of the first group of factors used in the LENC correction of the blue color channels
0x5115	LENC BLUE A2	0x07	RW	LENC Control 21 Bit[7:4]: Not used Bit[3:0]: blue_a2[3:0] Composed of the first group of factors used in the LENC correction of the blue color channels
0x5116	LENC BLUE B1	0xC2	RW	LENC Control 22 Bit[7:0]: blue_b1[7:0] Composed of the second group of factors used in the LENC correction of the blue color channels
0x5117	LENC BLUE B2	0x08	RW	LENC Control 23 Bit[7:4]: Not used Bit[3:0]: blue_b2[3:0] Composed of the second group of factors used in the LENC correction of the blue color channels

table 7-5 LENC control (sheet 4 of 4)

address	register name	default value	R/W	description
0x5118	LENC XSTARTH	0x00	RW	Bit[7:2]: Not used Bit[1:0]: X coordinate of the lens starting point[9:8]
0x5119	LENC XSTARTL	0x00	RW	Bit[7:0]: X coordinate of the lens starting point[7:0]
0x511A	LENC YSTARTH	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Y coordinate of the lens starting point[9:8]
0x511B	LENC YSTARTL	0x00	RW	Bit[7:0]: Y coordinate of the lens starting point[7:0]
0x511C	LENC CONTROL 24	0x80	RW	LENC Control 24 Bit[7]: round_en Determines whether or not to round off the last two bits of the LENC input data 0: Do not round off the last two bits 1: Round off the last two bits Bit[6]: Not used Changing this value is not allowed Bit[5]: skip_man_en 0: Use skip signals from system 1: Manually set skip signals by register 0x511C[3:0] Bit[4]: start_man_en 0: Start signal from system 1: Manually start set in register 0x5118~0x5116 Bit[3:2]: h_skip_man Bit[1:0]: v_skip_man
0x511D	RSVD	–	–	Reserved

table 7-6 WBC control (sheet 1 of 3)

address	register name	default value	R/W	description
0x5290	DNS CONTROL 00	0x04	RW	Bit[7:4]: Not used Bit[3:0]: Coefficient of Y de-noise threshold with respect to Y
0x5291	DNS CONTROL 01	0x06	RW	Bit[7:5]: Not used Bit[4:0]: Coefficient of UV de-noise threshold with respect to Y
0x5292	DNS CONTROL 02	0x00	RW	Bit[7:1]: Not used Bit[0]: De-noise and sharpness manual mode enable 0: Auto 1: Manual
0x5293	NOISE Y	0x02	RW	Bit[7:0]: noise_y De-noise weight for Y
0x5294	NOISE U	0x00	RW	Bit[7:1]: Not used Bit[0]: Noise U[8] De-noise weight for UV
0x5295	NOISE U	0x02	RW	Bit[7:0]: Noise U[7:0] De-noise weight for UV
0x5296	NOISE V	0x00	RW	Bit[7:1]: Not used Bit[0]: Noise V[8] De-noise weight for UV
0x5297	NOISE V	0x02	RW	Bit[7:0]: Noise V[7:0] De-noise weight for UV
0x5298	DNS EDGETHRE	0x06	RW	Bit[7:0]: DNS edgethre Edge threshold for UV smoothing
0x5299	DNS GBGR EXTRA	0x0C	RW	Bit[7:3]: Not used Bit[2:0]: dns_gbgr_extra De-noise threshold adjustment for Gb and Gr
0x529A	NOISE Y LIST 0	0x01	RW	Bit[7:0]: Noise Y list0[7:0] Noise Y threshold at 1x sensor gain
0x529B	NOISE Y LIST 1	0x01	RW	Bit[7:0]: Noise Y list1[7:0] Noise Y threshold at 2x sensor gain
0x529C	NOISE Y LIST 2	0x01	RW	Bit[7:0]: Noise Y list2[7:0] Noise Y threshold at 4x sensor gain
0x529D	NOISE Y LIST 3	0x01	RW	Bit[7:0]: Noise Y list03[7:0] Noise Y threshold at 8x sensor gain
0x529E	NOISE Y LIST 4	0x01	RW	Bit[7:0]: Noise Y list4[7:0] Noise Y threshold at 16x sensor gain

table 7-6 WBC control (sheet 2 of 3)

address	register name	default value	R/W	description
0x529F	NOISE Y LIST 5	0x01	RW	Bit[7:0]: Noise Y list5[7:0] Noise Y threshold at 32x sensor gain
0x52A0	NOISE Y LIST 6	0x02	RW	Bit[7:0]: Noise Y list6[7:0] Noise Y threshold at 64x sensor gain
0x52A1	NOISE Y LIST 7	0x02	RW	Bit[7:0]: Noise Y list7[7:0] Noise Y threshold at 64x sensor gain
0x52A2	NOISE UV LIST 0	0x00	RW	Bit[7:1]: Not used Bit[0]: Noise UV list0[8] Noise UV threshold at 1x sensor gain
0x52A3	NOISE UV LIST 0	0x02	RW	Bit[7:0]: Noise UV list0[7:0] Noise UV threshold at 1x sensor gain
0x52A4	NOISE UV LIST 1	0x00	RW	Bit[7:1]: Not used Bit[0]: Noise UV list1[8] Noise UV threshold at 2x sensor gain
0x52A5	NOISE UV LIST 1	0x02	RW	Bit[7:0]: Noise UV list1[7:0] Noise UV threshold at 2x sensor gain
0x52A6	NOISE UV LIST 2	0x00	RW	Bit[7:1]: Not used Bit[0]: Noise UV list2[8] Noise UV threshold at 4x sensor gain
0x52A7	NOISE UV LIST 2	0x02	RW	Bit[7:0]: Noise UV list2[7:0] Noise UV threshold at 4x sensor gain
0x52A8	NOISE UV LIST 3	0x00	RW	Bit[7:1]: Not used Bit[0]: Noise UV list3[8] Noise UV threshold at 8x sensor gain
0x52A9	NOISE UV LIST 3	0x0C	RW	Bit[7:0]: Noise UV list3[7:0] Noise UV threshold at 8x sensor gain
0x52AA	NOISE UV LIST 4	0x00	RW	Bit[7:1]: Not used Bit[0]: Noise UV list4[8] Noise UV threshold at 16x sensor gain
0x52AB	NOISE UV LIST 4	0x30	RW	Bit[7:0]: Noise UV list4[7:0] Noise UV threshold at 16x sensor gain
0x52AC	NOISE UV LIST 5	0x00	RW	Bit[7:1]: Not used Bit[0]: Noise UV list5[8] Noise UV threshold at 32x sensor gain
0x52AD	NOISE UV LIST 5	0x02	RW	Bit[7:0]: Noise UV list5[7:0] Noise UV threshold at 32x sensor gain
0x52AE	NOISE UV LIST 6	0x00	RW	Bit[7:1]: Not used Bit[0]: Noise UV list6[8] Noise UV threshold at 64x sensor gain

table 7-6 WBC control (sheet 3 of 3)

address	register name	default value	R/W	description
0x52AF	NOISE UV LIST 6	0x03	RW	Bit[7:0]: Noise UV list6[7:0] Noise UV threshold at 64x sensor gain
0x52B0	NOISE UV LIST 7	0x00	RW	Bit[7:1]: Not used Bit[0]: Noise UV list7[8] Noise UV threshold at 64x sensor gain
0x52B1	NOISE UV LIST 7	0x03	RW	Bit[7:0]: Noise UV list7[7:0] Noise UV threshold at 64x sensor gain

table 7-7 CIP control (sheet 1 of 3)

address	register name	default value	R/W	description
0x5300	CIP MIN GAIN	0x00	RW	Bit[7:3]: Not used Bit[2:0]: cip_mingain[10:8] Minimum real gain for calculation of CIP parameters normalized by 0x10
0x5301	CIP MIN GAIN	0x10	RW	Bit[7:0]: cip_mingain[7:0] Minimum real gain for calculation of CIP parameters normalized by 0x10
0x5302	CIP MAX GAIN	0x00	RW	Bit[7:3]: Not used Bit[2:0]: cip_maxgain[10:8] Maximum real gain for calculation of CIP parameters normalized by 0x10
0x5303	CIP MAX GAIN	0x80	RW	Bit[7:0]: cip_maxgain[7:0] Maximum real gain for calculation of CIP parameters normalized by 0x10
0x5304	CIP MIN INTNOISE	0x00	RW	Bit[7:1]: Reserved Bit[0]: cip_min_intnoise[8] CIP de-noise at CIP MIN GAIN. The larger the value, the blurrier the image.
0x5305	CIP MIN INTNOISE	0x20	RW	Bit[7:0]: cip_min_intnoise[7:0] CIP de-noise at CIP MIN GAIN. The larger the value, the blurrier the image.
0x5306	CIP MAX INTNOISE	0x00	RW	Bit[7:2]: Not used Bit[1:0]: cip_max_intnoise[9:8] CIP de-noise at CIP MAX GAIN. The larger the value, the blurrier the image.
0x5307	CIP MAX INTNOISE	0x20	RW	Bit[7:0]: cip_max_intnoise[7:0] CIP de-noise at CIP MAX GAIN. The larger the value, the blurrier the image.

table 7-7 CIP control (sheet 2 of 3)

address	register name	default value	R/W	description
0x5308	CIP SHARPEN MASK 0	0x00	RW	Bit[7:0]: CIP punsharpen mask0[7:0] (sign + abs) Weight for position 0 and 4 in the 5-point filter when evaluating edge effect
0x5309	CIP SHARPEN MASK 1	0x20	RW	Bit[7:0]: CIP punsharpen mask1[7:0] (sign + abs) Weight for position 1 and 3 in the 5-point filter when evaluating edge effect
0x530A	CIP CONTROL 10	0x81	RW	Bit[7:4]: Debug mode Bit[3]: Manual sharpen and de-noise enable 0: Auto 1: Manual Bit[2:1]: Debug mode Changing this value is not allowed Bit[0]: Anti-aliasing enable 0: Anti-aliasing mode disable 1: Anti-aliasing mode enable
0x530B	CIP CONTROL 11	0x02	RW	Bit[7:4]: Not used Bit[3:0]: Anti-aliasing parameter The larger the value, the stronger the color alias. Changing this value is not recommended.
0x530C	CIP CONTROL 12	0x04	RW	Bit[7:5]: Not used Bit[4:0]: Minimum sharpen[4:0] Sharpening at CIP MAX GAIN
0x530D	CIP CONTROL 13	0x0F	RW	Bit[7:6]: Not used Bit[5:0]: Maximum sharpen[5:0] Sharpening at CIP MIN GAIN
0x530E	CIP CONTROL 14	0x0C	RW	Bit[7:6]: Not used Bit[5:0]: Minimum positive edge threshold[5:0] Positive edge threshold for sharpening at CIP MIN GAIN
0x530F	CIP CONTROL 15	0x60	RW	Bit[7:0]: Maximum positive edge threshold[7:0] Positive edge threshold for sharpening at CIP MAX GAIN
0x5310	CIP CONTROL 16	0x18	RW	Bit[7:6]: Not used Bit[5:0]: Minimum negative edge threshold[5:0] Negative edge threshold for sharpening at CIP MIN GAIN
0x5311	CIP CONTROL 17	0x60	RW	Bit[7:0]: Maximum negative edge threshold[7:0] Negative edge threshold for sharpening at CIP MAX GAIN

table 7-7 CIP control (sheet 3 of 3)

address	register name	default value	R/W	description
0x5312	CIP CONTROL 18	0x40	RW	Bit[7:0]: Coefficient of edge threshold with respect to Y
0x5313	CIP CONTROL 19	0x18	RW	Bit[7:5]: Not used Bit[4:0]: Sharpening ratio of negative edge to positive edge normalized by 0x10
0x5314~ 0x5319	CIP CONTROL	–	RW	Color Interpolation Parameters Changing these values is not recommended
0x531A~ 0x5321	CIP CONTROL	–	RW	Manual Sharpness and De-noise Control

table 7-8 contrast control (sheet 1 of 3)

address	register name	default value	R/W	description
0x5400	CONTRAST MAX HIGH LEVEL	0x3F	RW	Bit[7]: Not used Bit[6:0]: Maximum high level[14:8] Maximum high level threshold Changing this value is not recommended
0x5401	CONTRAST MAX HIGH LEVEL	0xFF	RW	Bit[7:0]: Maximum high level[7:0] Maximum high level threshold Changing this value is not recommended
0x5402	CONTRAST MIN HIGH LEVEL	0x34	RW	Bit[7]: Not used Bit[6:0]: Minimum high level[14:8] Minimum high level threshold in 15-bit scale
0x5403	CONTRAST MIN HIGH LEVEL	0x00	RW	Bit[7:0]: Minimum high level[7:0] Minimum high level threshold in 15-bit scale
0x5404	CONTRAST MAX LOW LEVEL	0x02	RW	Bit[7]: Not used Bit[6:0]: Maximum low level[14:8] Maximum low level threshold in 15-bit scale
0x5405	CONTRAST MAX LOW LEVEL	0x40	RW	Bit[7:0]: Maximum low level[7:0] Maximum low level threshold in 15-bit scale
0x5406	CONTRAST MIN LOW LEVEL	0x00	RW	Bit[7]: Not used Bit[6:0]: Minimum low level[14:8] Minimum low level threshold in 15-bit data range

table 7-8 contrast control (sheet 2 of 3)

address	register name	default value	R/W	description
0x5407	CONTRAST MIN LOW LEVEL	0x00	RW	Bit[7:0]: Minimum low level[7:0] Minimum low level threshold in 15-bit data range
0x5408	CONTRAST CURLOWLEVEL	0x01	RW	Bit[7]: Not used Bit[6:0]: Current lowlevel[14:8] Current low level manual setting
0x5409	CONTRAST CURLOWLEVEL	0x00	RW	Bit[7:0]: Current lowlevel[7:0] Current low level manual setting
0x540A	CONTRAST CURHIGHLEVEL	0x3F	RW	Bit[7]: Not used Bit[6:0]: Current highlevel[14:8] Current high level manual setting
0x540B	CONTRAST CURHIGHLEVEL	0xFF	RW	Bit[7:0]: Current highlevel[7:0] Current high level manual setting
0x540C~ 0x540D	NOT USED	–	–	Not Used
0x540E	CONTRAST THRES1	0x00	RW	Bit[7]: Not used Bit[6:0]: Thres1[22:16] Dark pixel number threshold used to determine low level threshold
0x540F	CONTRAST THRES1	0x3A	RW	Bit[7:0]: Thres1[15:8] Dark pixel number threshold used to determine low level threshold
0x5410	CONTRAST THRES1	0x98	RW	Bit[7:0]: Thres1[7:0] Dark pixel number threshold used to determine low level threshold
0x5411	NOT USED	–	–	Not Used
0x5412	CONTRAST THRES2	0x00	RW	Bit[7]: Not used Bit[6:0]: Thres2[22:16] Bright pixel number threshold used to determine high level threshold
0x5413	CONTRAST THRES2	0x3A	RW	Bit[7:0]: Thres2[15:8] Bright pixel number threshold used to determine high level threshold
0x5414	CONTRAST THRES2	0x98	RW	Bit[7:0]: Thres2[7:0] Bright pixel number threshold used to determine high level threshold
0x5415~ 0x541C	DEBUG MODE	–	–	Debug Mode Changing these values is not allowed

table 7-8 contrast control (sheet 3 of 3)

address	register name	default value	R/W	description
0x541D	CONTRAST STEP	0x20	RW	Bit[7:0]: Step[7:0] Step for low and high level adjustment in 15-bit scale
0x541E~ 0x5426	DEBUG MODE	–	–	Debug Mode Changing these values is not allowed

table 7-9 gamma control (sheet 1 of 5)

address	register name	default value	R/W	description
0x5480	GAMMA CTRL00	0x12	RW	Bit[7:0]: y_list_00 Output at 0x10 (10-bit scale) when register 0x5000[5] = 1
0x5481	GAMMA CTRL01	0x1D	RW	Bit[7:0]: y_list_01 Output at 0x20 (10-bit scale) when register 0x5000[5] = 1
0x5482	GAMMA CTRL02	0x2B	RW	Bit[7:0]: y_list_02 Output at 0x40 (10-bit scale) when register 0x5000[5] = 1
0x5483	GAMMA CTRL03	0x40	RW	Bit[7:0]: y_list_03 Output at 0x80 (10-bit scale) when register 0x5000[5] = 1
0x5484	GAMMA CTRL04	0x49	RW	Bit[7:0]: y_list_04 Output at 0xA0 (10-bit scale) when register 0x5000[5] = 1
0x5485	GAMMA CTRL05	0x51	RW	Bit[7:0]: y_list_05 Output at 0xC0 (10-bit scale) when register 0x5000[5] = 1
0x5486	GAMMA CTRL06	0x6E	RW	Bit[7:0]: y_list_06 Output at 0xE0 (10-bit scale) when register 0x5000[5] = 1
0x5487	GAMMA CTRL07	0x62	RW	Bit[7:0]: y_list_07 Output at 0x100 (10-bit scale) when register 0x5000[5] = 1
0x5488	GAMMA CTRL08	0x6A	RW	Bit[7:0]: y_list_08 Output at 0x120 (10-bit scale) when register 0x5000[5] = 1

table 7-9 gamma control (sheet 2 of 5)

address	register name	default value	R/W	description
0x5489	GAMMA CTRL09	0x73	RW	Bit[7:0]: y_list_09 Output at 0x140 (10-bit scale) when register 0x5000[5] = 1
0x548A	GAMMA CTRL0A	0x88	RW	Bit[7:0]: y_list_10 Output at 0x180 (10-bit scale) when register 0x5000[5] = 1
0x548B	GAMMA CTRL0B	0xA0	RW	Bit[7:0]: y_list_11 Output at 0x1C0 (10-bit scale) when register 0x5000[5] = 1
0x548C	GAMMA CTRL0C	0xCA	RW	Bit[7:0]: y_list_12 Output at 0x240 (10-bit scale) when register 0x5000[5] = 1
0x548D	GAMMA CTRL0D	0xE0	RW	Bit[7:0]: y_list_13 Output at 0x2C0 (10-bit scale) when register 0x5000[5] = 1
0x548E	GAMMA CTRL0E	0xEA	RW	Bit[7:0]: y_list_14 Output at 0x340 (10-bit scale) when register 0x5000[5] = 1
0x548F	GAMMA CTRL0F	0x0F	RW	Bit[7:0]: y_list_15 Slope in range of (0x341, 0x3FF) which should be 2 x (255 - register 0x548E) / 3
0x5490	GAMMA GAIN LIST00	0x04	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 00[11:8] UV output at 0x10 (10-bit scale)
0x5491	GAMMA GAIN LIST00	0x80	RW	Bit[7:0]: Gain list 00[7:0] UV output at 0x10 (10-bit scale)
0x5492	GAMMA GAIN LIST01	0x03	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 01[11:8] UV output at 0x20 (10-bit scale)
0x5493	GAMMA GAIN LIST01	0xA0	RW	Bit[7:0]: Gain list 01[7:0] UV output at 0x20 (10-bit scale)
0x5494	GAMMA GAIN LIST02	0x02	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 02[11:8] UV output at 0x40 (10-bit scale)
0x5495	GAMMA GAIN LIST02	0xB0	RW	Bit[7:0]: Gain list 02[7:0] UV output at 0x40 (10-bit scale)
0x5496	GAMMA GAIN LIST03	0x02	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 03[11:8] UV output at 0x80 (10-bit scale)

table 7-9 gamma control (sheet 3 of 5)

address	register name	default value	R/W	description
0x5497	GAMMA GAIN LIST03	0x00	RW	Bit[7:0]: Gain list 03[7:0] UV output at 0x80 (10-bit scale)
0x5498	GAMMA GAIN LIST04	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 04[11:8] UV output at 0xA0 (10-bit scale)
0x5499	GAMMA GAIN LIST04	0xD3	RW	Bit[7:0]: Gain list 04[7:0] UV output at 0xA0 (10-bit scale)
0x549A	GAMMA GAIN LIST05	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 05[11:8] UV output at 0xC0 (10-bit scale)
0x549B	GAMMA GAIN LIST05	0xB0	RW	Bit[7:0]: Gain list 05[7:0] UV output at 0xC0 (10-bit scale)
0x549C	GAMMA GAIN LIST06	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 06[11:8] UV output at 0xE0 (10-bit scale)
0x549D	GAMMA GAIN LIST06	0x97	RW	Bit[7:0]: Gain list 06[7:0] UV output at 0xE0 (10-bit scale)
0x549E	GAMMA GAIN LIST07	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 07[11:8] UV output at 0x100 (10-bit scale)
0x549F	GAMMA GAIN LIST07	0x88	RW	Bit[7:0]: Gain list 07[7:0] UV output at 0x100 (10-bit scale)
0x54A0	GAMMA GAIN LIST08	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 08[11:8] UV output at 0x120 (10-bit scale)
0x54A1	GAMMA GAIN LIST08	0x79	RW	Bit[7:0]: Gain list 08[7:0] UV output at 0x120 (10-bit scale)
0x54A2	GAMMA GAIN LIST09	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 09[11:8] UV output at 0x140 (10-bit scale)
0x54A3	GAMMA GAIN LIST09	0x70	RW	Bit[7:0]: Gain list 09[7:0] UV output at 0x140 (10-bit scale)
0x54A4	GAMMA GAIN LIST10	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 10[11:8] UV output at 0x180 (10-bit scale)
0x54A5	GAMMA GAIN LIST10	0x6B	RW	Bit[7:0]: Gain list 10[7:0] UV output at 0x180 (10-bit scale)
0x54A6	GAMMA GAIN LIST11	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 11[11:8] UV output at 0x1C0 (10-bit scale)

table 7-9 gamma control (sheet 4 of 5)

address	register name	default value	R/W	description
0x54A7	GAMMA GAIN LIST11	0x6E	RW	Bit[7:0]: Gain list 11[7:0] UV output at 0x1C0 (10-bit scale)
0x54A8	GAMMA GAIN LIST12	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 12[11:8] UV output at 0x240 (10-bit scale)
0x54A9	GAMMA GAIN LIST12	0x67	RW	Bit[7:0]: Gain list 12[7:0] UV output at 0x240 (10-bit scale)
0x54AA	GAMMA GAIN LIST13	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 13[11:8] UV output at 0x2C0 (10-bit scale)
0x54AB	GAMMA GAIN LIST13	0x45	RW	Bit[7:0]: Gain list 13[7:0] UV output at 0x2C0 (10-bit scale)
0x54AC	GAMMA GAIN LIST14	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 14[11:8] UV output at 0x340 (10-bit scale)
0x54AD	GAMMA GAIN LIST14	0x20	RW	Bit[7:0]: Gain list 14[7:0] UV output at 0x340 (10-bit scale)
0x54AE	GAMMA GAIN LIST15	0xFF	RW	Bit[7:5]: Reserved Bit[4:0]: gain_list_15[12:8] Slope in range of (0x341, 0x3FF) which should be 2 x (255 - {0x54AC[3:0], 0x54AD[7:0]}) / 3
0x54AF	GAMMA GAIN LIST15	0xEB	RW	Bit[7:0]: Gain list 15[7:0] Slope in range of (0x341, 0x3FF) which should be 2 x (255 - {0x54AC[3:0], 0x54AD[7:0]}) / 3
0x54B0	GAMMA CTRL30	0x01	RW	Bit[7:2]: Not used Bit[1]: Debug mode Changing this value is not allowed Bit[0]: Dark area color saturation reduction enable 0: Do not reduce color saturation in dark area 1: Reduce color saturation in area where luminance level is less than 0x54B1[7:0]
0x54B1	GAMMA CTRL31	0x20	RW	Bit[7:0]: Dark threshold for color saturation reduction
0x54B2	GAMMA CTRL32	0x00	RW	Bit[7:1]: Not used Bit[0]: Dark area noise reduction enable 0: Do not reduce noise in dark area 1: Reduce noise in area where luminance level is less than 0x54B3[7:0]
0x54B3	GAMMA CTRL33	0x10	RW	Bit[7:0]: Dark threshold for noise reduction

table 7-9 gamma control (sheet 5 of 5)

address	register name	default value	R/W	description
0x54B4	GAMMA CTRL34	0x00	RW	Bit[7:1]: Not used Bit[0]: Bright area color saturation reduction enable 0: Do not reduce color saturation in bright area 1: Reduce color saturation in area where luminance level is greater than 0x54B5[7:0]
0x54B5	GAMMA CTRL35	0xF0	RW	Bit[7:0]: Bright threshold for color saturation reduction
0x54B6	GAMMA CTRL36	0x00	RW	Bit[7:1]: Not used Bit[0]: Bright area noise reduction enable 0: Do not reduce noise in bright area 1: Reduce noise in area where luminance level is greater than 0x54B7[7:0]
0x54B7	GAMMA CTRL37	0xDF	RW	Bit[7:0]: Bright threshold for noise reduction

table 7-10 auto color saturation (sheet 1 of 2)

address	register name	default value	R/W	description
0x5500	UV UVADJUST CONTROL 0	0x08	RW	Bit[7:5]: Not used Bit[4:0]: Auto color saturation offset UV ADJUST IN value minimum threshold
0x5501	UV UVADJUST CONTROL 3	0x1F	RW	Bit[7:6]: Not used Bit[5]: Color saturation manual adjustment enable 0: Automatically adjust color saturation according to sensor gain 1: Manual set color saturation by register 0x5501[4:0] Bit[4:0]: UV ADJUST IN manual setting Manual color saturation setting
0x5502	UV ADJ TH1	0x00	RW	Bit[7:1]: Not used Bit[0]: uv_adj_th1[8] Real gain threshold 1 for UV ADJUST IN. When real gain is smaller than UV ADJ TH1, UV ADJUST IN will be limited to 31.

table 7-10 auto color saturation (sheet 2 of 2)

address	register name	default value	R/W	description
0x5503	UV ADJ TH1	0x1F	RW	Bit[7:0]: UV ADJ TH1[7:0] Real gain threshold 1 for UV ADJUST IN. When real gain is smaller than UV ADJ TH1, UV ADJUST IN will be limited to 31.
0x5504	UV ADJ TH2	0x00	RW	Bit[7:1]: Reserved Bit[0]: uv_adj_th2[8] Real gain threshold 2 for UV ADJUST IN. When real gain is larger than UV ADJ TH1, UV ADJUST IN will be limited to UV offset (0x5500[4:0]).
0x5505	UV ADJ TH2	0x7F	RW	Bit[7:0]: UV adj th2[7:0] Real gain threshold 2 for UV ADJUST IN. When real gain is larger than UV ADJ TH1, UV ADJUST IN will be limited to UV offset (0x5500[4:0]).

table 7-11 SDE control (sheet 1 of 2)

address	register name	default value	R/W	description
0x5580	SDE CONTROL0	0x00	RW	Bit[7]: Fixed Y enable - works with register 0x5587[7:0] 0: Fixed Y disable 1: Fixed Y enable Bit[6]: Negative Y enable 0: Negative Y disable 1: Negative Y enable Bit[5]: Gray image enable 0: Gray image disable 1: Gray image enable Bit[4]: Fixed V enable - works with register 0x5586[7:0] 0: Fixed V disable 1: Fixed V enable Bit[3]: Fixed U enable - works with register 0x5585[7:0] 0: Fixed U disable 1: Fixed U enable Bit[2]: Contrast enable - works with registers 0x5587[7:0], 0x5588[7:0], and 0x5589[7:0] 0: Contrast disable 1: Contrast enable Bit[1]: Saturation enable - works with registers 0x5583[7:0] and 0x5584[7:0] 0: Saturation disable 1: Saturation enable Bit[0]: Hue enable 0: Hue disable 1: Hue enable
0x5581	SDE CONTROL1	0x80	RW	Bit[7:0]: hue_cos When register 0x558A[6] = 0, this register is hue_cos. When register 0x558A[6] = 1, this register is angle[7:0].
0x5582	SDE CONTROL2	0x00	RW	Bit[7:0]: hue_sin When register 0x558A[6] = 0, this register is hue_sin. When register 0x558A[6] = 1, this register is angle[8]
0x5583	SDE CONTROL3	0x40	RW	Bit[7:0]: Saturation U
0x5584	SDE CONTROL4	0x40	RW	Bit[7:0]: Saturation V
0x5585	SDE CONTROL5	0x80	RW	Bit[7:0]: Ureg for fixed U
0x5586	SDE CONTROL6	0x80	RW	Bit[7:0]: Vreg for fixed V

table 7-11 SDE control (sheet 2 of 2)

address	register name	default value	R/W	description
0x5587	SDE CONTROL7	0x00	RW	Bit[7:0]: Yoffset for contrast or Y value for fixed Y
0x5588	SDE CONTROL8	0x20	RW	Bit[7:0]: Ygain for contrast
0x5589	SDE CONTROL9	0x00	RW	Bit[7:0]: Ybright for contrast
0x558A	SDE CONTROL10	0x01	RW	Bit[7]: Yoffset manual mode enable 0: Auto mode for Yoffset in contrast 1: Manual mode for Yoffset in contrast Bit[6]: Hue angle enable Bit[5]: COS sign for Cr Bit[4]: COS sign for Cb Bit[3]: Offset sign for contrast Bit[2]: Bright sign for contrast Bit[1]: SIN sign for Cb Bit[0]: SIN sign for Cr

table 7-12 AVG control (sheet 1 of 2)

address	register name	default value	R/W	description
0x5680	AVG X START	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Avg x start[11:8] Horizontal start position for average window
0x5681	AVG X START	0x00	RW	Bit[7:0]: Avg x start[7:0] Horizontal start position for average window
0x5682	AVG X END	0x08	RW	Bit[7:4]: Not used Bit[3:0]: Avg x end[11:8] Horizontal end position for average window
0x5683	AVG X END	0x00	RW	Bit[7:0]: Avg x end[7:0] Horizontal end position for average window
0x5684	AVG Y START	0x00	RW	Bit[7:3]: Not used Bit[2:0]: Avg y start[10:8] Vertical start position for average window
0x5685	AVG Y START	0x00	RW	Bit[7:0]: Avg y start[7:0] Vertical start position for average window

table 7-12 AVG control (sheet 2 of 2)

address	register name	default value	R/W	description
0x5686	AVG Y END	0x06	RW	Bit[7:3]: Not used Bit[2:0]: Avg y end[10:8] Vertical end position for average window
0x5687	AVG Y END	0x00	RW	Bit[7:0]: Avg y end[7:0] Vertical end position for average window
0x5688	AVG R8	0xFF	RW	Bit[7:6]: Not used Bit[5:4]: window1_weight Bit[3:2]: Not used Bit[1:0]: window0_weight
0x5689	AVG R9	0xFF	RW	Bit[7:6]: Not used Bit[5:4]: window3_weight Bit[3:2]: Not used Bit[1:0]: window2_weight
0x568A	AVG RA	0xFF	RW	Bit[7:6]: Not used Bit[5:4]: window5_weight Bit[3:2]: Not used Bit[1:0]: window4_weight
0x568B	AVG RB	0xFF	RW	Bit[7:6]: Not used Bit[5:4]: window7_weight Bit[3:2]: Not used Bit[1:0]: window6_weight
0x568C	AVG RC	0xFF	RW	Bit[7:6]: Not used Bit[5:4]: window9_weight Bit[3:2]: Not used Bit[1:0]: window8_weight
0x568D	AVG RD	0xFF	RW	Bit[7:6]: Not used Bit[5:4]: window11_weight Bit[3:2]: Not used Bit[1:0]: window10_weight
0x568E	AVG RE	0xFF	RW	Bit[7:6]: Not used Bit[5:4]: window13_weight Bit[3:2]: Not used Bit[1:0]: window12_weight
0x568F	AVG RF	0xFF	RW	Bit[7:6]: Not used Bit[5:4]: window15_weight Bit[3:2]: Not used Bit[1:0]: window14_weight

8 operating specifications

8.1 absolute maximum ratings

table 8-1 absolute maximum ratings

parameter		absolute maximum rating[a]
supply voltage (with respect to ground)	V_{DD-A}	4.5V
	V_{DD-D}	3.0V
	V_{DD-IO}	4.5V
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
all input/output voltages (with respect to ground)		-0.3V to V_{DD-IO} + 1V
I/O current on any input or output pin		± 200 mA
peak solder temperature (10 second dwell time)		245°C

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

8.2 functional temperature

table 8-2 functional temperature

parameter	range
operating temperature[a]	-20°C to +70°Cjunction temperature
stable image temperature range[b]	0°C to +50°C junction temperature

a. sensor functions in the operating range; however, some image quality changes may be noticed at the temperature extremes.

b. image quality remains stable throughout this temperature range

8.3 DC characteristics

table 8-3 DC characteristics

symbol	parameter	min	typ	max	unit
supply					
V_{DD-A}	supply voltage (analog)	3.14	3.3	3.47	V
V_{DD-IO}	supply voltage (digital I/O)	1.7	1.8	3.47	V
I_{DD-A}	active (operating) current for NTSC	–	46	64	mA
I_{DD-IO}		–	52	73	mA
I_{DD-A}	active (operating) current for digital	–	46	69	mA
I_{DD-IO}		–	52	78	mA
$I_{DDS-SCCB}$	standby current	–	1.8	2.7	mA
$I_{DDS-PWDN}$		–	20	50	µA
digital inputs (typical conditions: AVDD = 3.3V, DOVDD = 1.8V~3.3V)					
V_{IL}	input voltage LOW	–	–	0.3 × DOVDD	V
V_{IH}	input voltage HIGH	0.7 × DOVDD	–	–	V
C_{IN}	input capacitor	–	–	10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	0.9 × DOVDD	–	–	V
V_{OL}	output voltage LOW	–	–	0.1 × DOVDD	V
serial interface inputs					
V_{IL}	SCL and SDA	-0.5	0.0	0.3 × DOVDD	V
V_{IH}	SCL and SDA	0.7 × DOVDD	DOVDD	DOVDD + 0.5	V

8.4 AC characteristics

table 8-4 AC characteristics (T_A = 25°C, V_{DD-A} = 3.3V, V_{DD-IO} = 1.8V)

symbol	parameter	min	typ	max	unit
ADC parameters					
B	analog bandwidth		12		MHz
DLE	DC differential linearity error		<0.5		LSB
ILE	DC integral linearity error		<0.5		LSB
	settling time for software reset			<1	ms
	settling time for resolution mode change			<1	ms
	settling time for register setting			<300	ms

table 8-5 timing characteristics

symbol	parameter	min	typ	max	unit
oscillator and clock input					
	frequency for NTSC		24.545452		MHz
f_{OSC}[a]	frequency for PAL		29.5		MHz
	frequency for digital	6	12.27	29.5	MHz
t_r, t_f	clock input rise/fall time			5 (10[b])	ns

a. less than ± 30 ppm for f_{osc} tolerance is recommended

b. if using the internal PLL

9 mechanical specifications

9.1 physical specifications

figure 9-1 package specifications

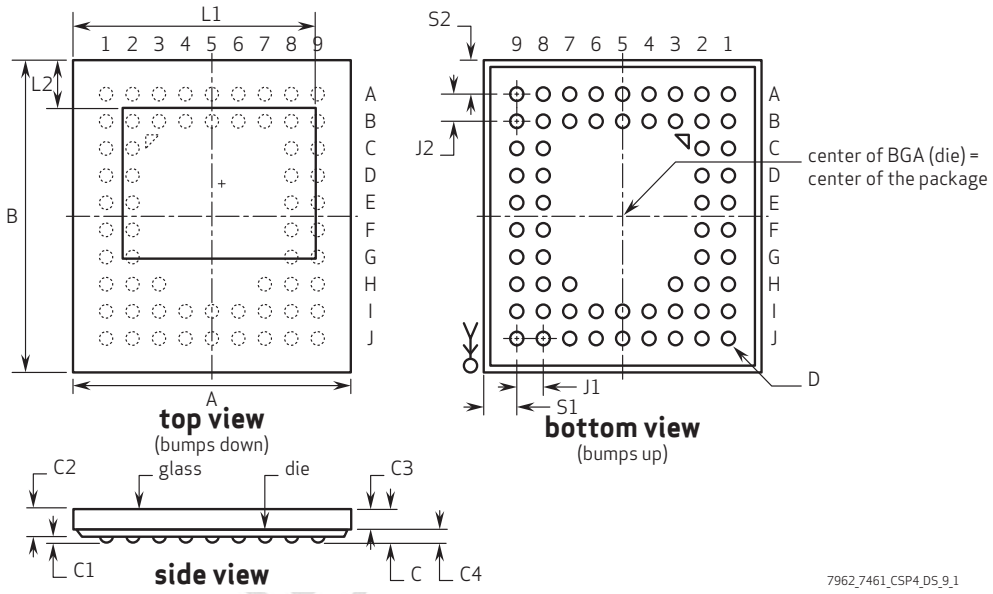


table 9-1 package dimensions (sheet 1 of 2)

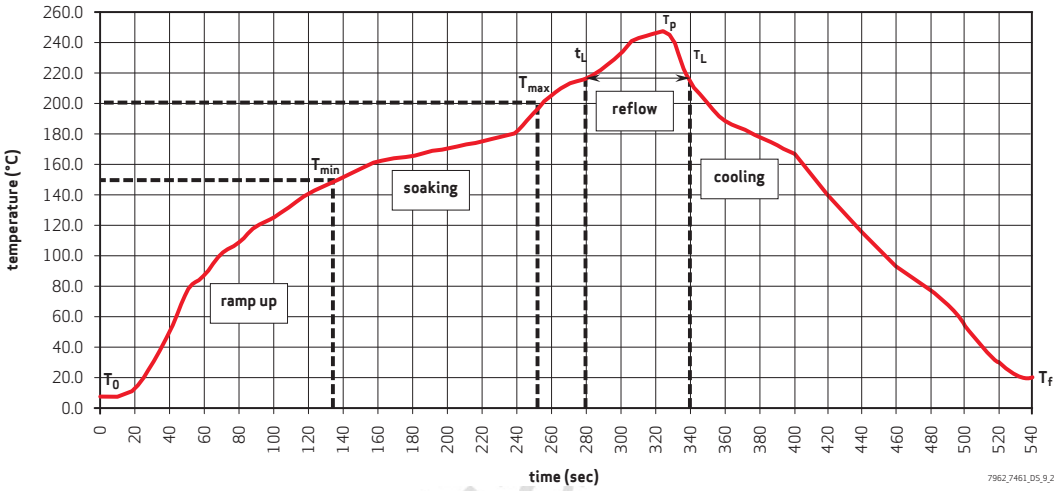
parameter	symbol	min	typ	max	unit
package body dimension x	A	6620	6645	6670	µm
package body dimension y	B	7070	7095	7120	µm
package height	C	610	670	730	µm
pixel to package edge dimension A	L1	5904.5	5939.5	5974.5	µm
pixel to package edge dimension B	L2	985.5	1020.5	1055.5	µm
ball height	C1	130	160	190	µm
package body thickness	C2	465	510	555	µm
thickness of glass surface to die	C3	385	405	425	µm
image plane height	C4	225	265	305	µm
ball diameter	D	270	300	330	µm

table 9-1 package dimensions (sheet 2 of 2)

parameter	symbol	min	typ	max	unit
total pin count	N		62 (10 NC)		
pin count x-axis	N1		9		
pin count y-axis	N2		10		
pins pitch x-axis	J1		670		µm
pins pitch y-axis	J2		660		µm
edge-to-pin center distance along x	S1	613	643	673	µm
edge-to-pin center distance along y	S2	548	578	608	µm
tilt between die and glass				0.12	degree
die rotation				0.2	degree

9.2 IR reflow specifications

figure 9-2 IR reflow ramp rate requirements



note
The OV7962/OV7461 uses a lead free package.

table 9-2 reflow conditions[ab]

zone	description	exposure
ramp up A (T_0 to T_{min})	heating from room temperature to 150°C	temperature slope ≤ 3°C per second
soaking	heating from 150°C to 200°C	90 ~ 150 seconds
ramp up B (t_L to T_p)	heating from 217°C to 245°C	temperature slope ≤ 3°C per second
peak temperature	maximum temperature in SMT	245°C +0/-5°C (duration max 30 sec)
reflow (t_L to T_L)	temperature higher than 217°C	30 ~ 120 seconds
ramp down A (T_p to T_L)	cooling from 245°C to 217°C	temperature slope ≤ 3°C per second
ramp down B (T_L to T_f)	cooling from 217°C to room temperature	temperature slope ≤ 2°C per second
T_0 to T_p	room temperature to peak temperature	≤ 8 minutes

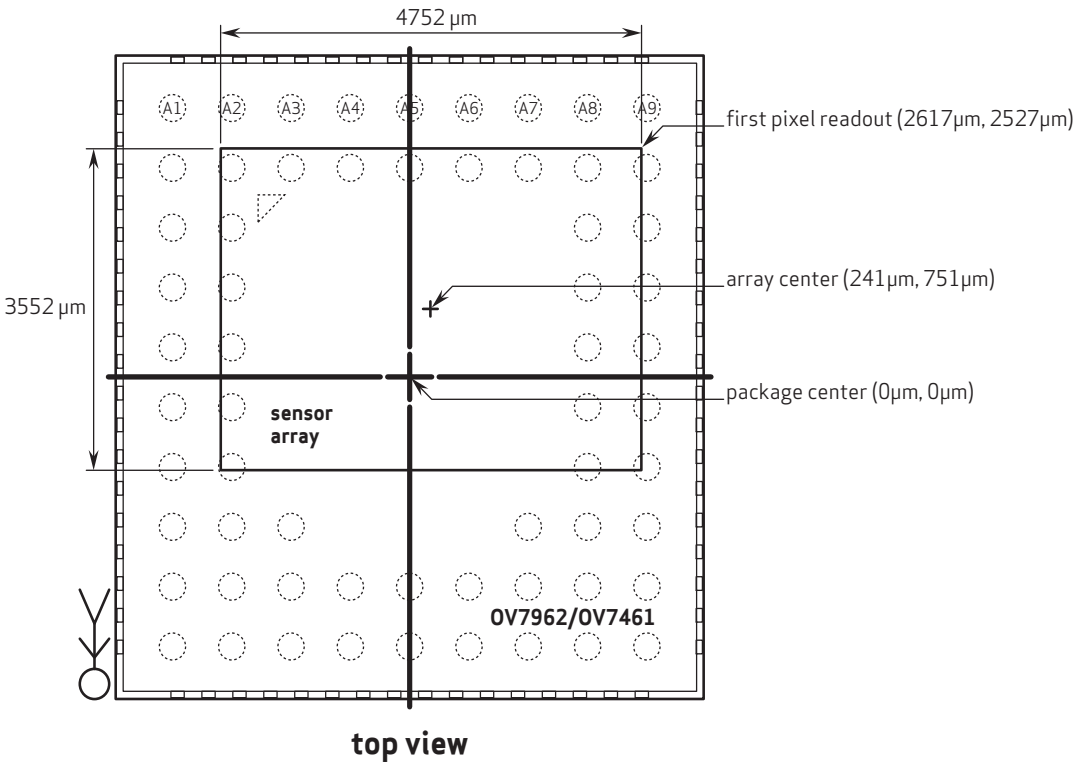
a. maximum number of reflow cycles = 3

b. N2 gas reflow or control O2 gas PPM<500 as recommendation

10 optical specifications

10.1 sensor array center

figure 10-1 sensor array center



top view

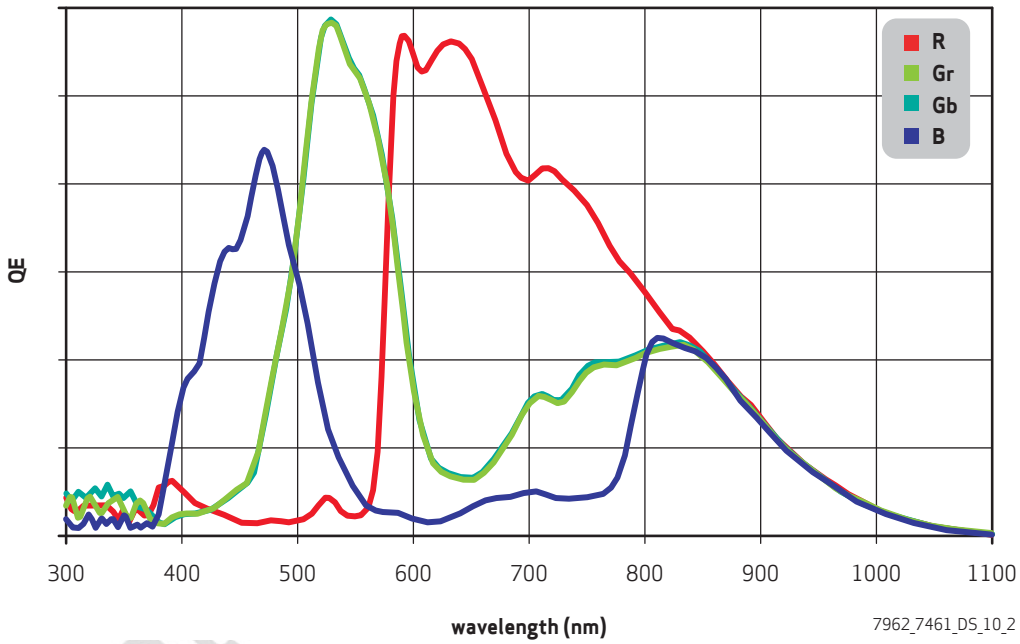
note 1 this drawing is not to scale and is for reference only.

note 2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pins A1 to A9 oriented down on the PCB.

7962_7461_CSP4_DS_10_1

note To reduce image artifacts from infrared light and provide the best image quality, OmniVision recommends an IR cut filter

figure 10-2 light response graph



revision history

version 1.0 07.02.2009

- initial release

version 1.2 02.05.2010

- in ordering information, in ordering information changed B&W part number from "OV07462" to "OV07461", removed TBDs from key specifications and changed analog power supply from "3.3V ± 5%" to "3.14V~3.47V"
- in key specifications, added "(no microlens shift)" to chief ray angle,
- in 2, updated figure 2-2
- in section 2.6, inserted diagrams 2-4, 2-5, 2-6 and table 2-3
- in section 2.3, changed divider register from "0x3095" to "0x3096" and values "10 – /2" to "10 – /3"
- in section 2.3, created cross references to registers, added System Divider information, and updated figure 2-3
- in section 5.9, replaced color matrix information with "to cancel out crosstalk and convert color space..." and added color matrix block
- in 6, added "Max SPI speed is 49.09MHz" to register 0x6200 Bit[4:0]
- in 6, added section 6.2.4
- in section 7, split table 7-1 to create ISP control table 7-4 and inserted registers 0x4300 through 0x472F into tables 7-2 and 7-3
- in chapter 7, added "The device slave address are 0x80 for write and 0x81 for read."
- in table 7-1, changed Bit[2] description for register 0x3005 from "Not used" to "Mirror control select", changed Bit[7] description from "Not used" to "SRST" and added information for SRST
- in section 8, changed section title from "electrical" to "operating"
- in table 8-2, changed note a from "sensor functions but image quality may be noticeably different at temperatures outside of stable range" to "Sensor functions in the operating range, however, some image quality changes may be noticed at the temperature extremes."

version 1.3 03.22.2010

- in section 2.7, added "including the register write, set 0x3094[5] to 0, to disable group write if necessary" for step 2
- in chapter 5, extensively updated default values for tables 5-1, 5-4, 5-7, 5-9, 5-10, 5-11, 5-13, 5-16, and 5-17
- in chapter 6, extensively updated default values for tables 6-2 and 6-3
- in section 6.2.2, updated figure 6-5
- in table 6-1, changed WVGA timing (3) "14424" to "18704", (5) "8692" to "12208", VGA timing (3) "14032" to "20004", (5) "18180" to "12208" and QVGA (3) "3578" to "4654", (5) "4124" to "3048"
- in chapter 7, extensively updated default values for tables 7-1, 7-2, 7-3, 7-4, 7-6, 7-7, 7-8, 7-9, 7-10, and 7-12

version 1.4 07.15.2010

- in key specifications, changed active power requirements to 245 mW
- in table 7-3, changed typ value for active (operating) current for NTSC (I_{DD-A}) to 46 mA and max value to 64 mA
- in table 7-3, added typ value for active (operating) current for digital (I_{DD-A}) to 46 mA and max value to 69 mA
- in table 7-3, changed typ value for active (operating) current for NTSC (I_{DD-IO}) to 52 mA and max value to 73 mA
- in table 7-3, added typ value for active (operating) current for digital (I_{DD-IO}) to 52 mA and max value to 78 mA
- in table 7-3, changed typ value for $I_{DDS-SCCB}$ to 1.8 mA and max value to 2.7mA
- in table 7-3, changed typ value for $I_{DDS-PWDN}$ to 20 µA and max value to 50 µA
- in table 7-4, changed typ value for analog bandwidth to 12 MHz

version 2.0 01.06.2011

- updated datasheet from Preliminary Specification to Product Specification
- in section 1, added description "(this pin cannot be floating)" to signal description for pins A8 and D2
- in section 2, added new section 2.7 and figure 2-7
- in table 6-3, for register 0x6200, changed "Max SPI speed is 24.5454MHz" to "SPI_Clock frequency = Input system clock frequency..."
- in table 6-4, added note "a"
- extensive changes to register tables' default values in section 7
- in section 7, for registers 0x308F~0x3092 added "FF is normalized as 100% for 7960" to register description
- in table 8-3, changed from "DOVDD = 1.8V" to "DOVDD =1.8V ~3.3V", V_{IL} max from "0.54" to "0.3 DOVDD, C_{IN} max from "0.18" to "0.1 DOVDD", serial interface inputs V_{IL} max from "0.54" to "0.3 DOVDD", VIH from "1.26, 1.8, 2.3" to "0.7 DOVDD, DOVDD, DOVDD + 0.5" and removed note a
- in table 8-5 added note a
- in table 9-1, changed package body dimension x min, typ, max from "6655, 6680, 6705" to "6620, 6645, 6670", package body dimension y min, typ, max from "7105, 7130, 7155" to "7070, 7095, 7120", package height min, typ, max from "630, 700, 770" to "610, 670, 730", package body thickness min, typ, max from "485, 540, 595" to "465, 510, 555", thickness of glass surface to die min, typ, max from "405, 435, 465" to "385, 405, 425", edge-to-pin center distance analog x min, typ, max from "630, 660, 690" to "613, 643, 673" and edge-to-pin center distance analog y min, typ, max from "565, 595, 625" to "548, 578, 608"
- in section 9, added note a to table 9-2
- in section 10, added figure 10-2

version 2.1 03.01.2012

- in table 1-1, added "digital..." to pin description for pins G8, H9 and removed sidebar note

- in section 2.2, changed "stream..." to "streaming..." and "circuitry ..." to "circuitry which..." in section description
- in section 2.3, changed "...frequency..." to "frequencies..." in section description
- in table 2-1, replaced table and removed table 2-2
- in section 4.2, changed "...setting signal..." to "...setting register..."
- in table 4-2, changed table title to "test pattern registers"
- in table 4-5, updated register descriptions for registers 0x5688, 0x5689, 0x568A, 0x568B, 0x568C, 0x568D, 0x568E, 0x568F, and 0x5690
- in section 4.4, updated last two sentences in section description
- in sub-section 4.4.1.2, changed "In 50 or 60Hz flicker light..." to "In a 50Hz or 60Hz light flicker..."
- in section 4.6, changed section description to "After black level subtraction an optional digital..."
- in section 5, updated section descriptions for sections 5.3, 5.5, and 5.6
- in table 5-3, updated register description for register 0x511C
- in table 5-6, updated register description for register 0x5280
- in table 5-7, updated register descriptions for registers 0x5291 and 0x5299
- in section 5.11, changed "...H processing..." to "..Y processing..."
- in table 5-13, updated register descriptions for registers 0x5502 and 0x5504
- in table 5-16, updated register descriptions for registers 0x5688, 0x5689, 0x568A, 0x568B, 0x568C, 0x568D, 0x568E, 0x568F, and 0x5690
- in table 6-4, changed ESO description from "data input" to "data output"
- in table 7-1, updated bit descriptions for registers 0x3005, 0x3009, 0x3011, 0x3012, 0x3020, 0x3038, 0x303E, 0x3041, 0x3043, 0x3053, 0x3053, 0x305A, 0x305B, 0x305C, 0x3062, 0x3064, 0x3068, 0x306A, 0x306B, 0x3094, and 0x30EC
- in table 7-5, updated register description for register 0x511C
- in table 7-6, updated register descriptions for registers 0x5291 and 0x5299
- in table 7-7, updated register descriptions for registers 0x5300, 0x5302, 0x5306, and 0x530A
- in table 7-9, updated register description for register 0x54AE
- in table 7-10, updated register descriptions for registers 0x5502 and 0x5504
- in table 7-12, updated register descriptions for registers 0x5688, 0x5689, 0x568A, 0x568B, 0x568C, 0x568D, 0x568E, 0x568F, and 0x5690
- in chapter 9, removed sidebar note
- in section 10.1, added sidebar note

version 2.2 08.01.2012

- in section 5.5, added sub-section 5.5.1 and figure 5-1
- in table 5-5, added row for register 0x5183
- in section 9.1, updated figure 9-1 and table 9-1 by adding rows for symbols L1 and L2
- in section 9.2, updated figure 9-2 and table 9-2

version 2.21 09.06.2012

- in section 4.1, added last to sentences to section description
- in table 7-1, added "The maximum recommended value is 0x24 for NTSC" to register 0x3017, "It is not recommended to change this register" to register 0x301B, and "The maximum suggested setting for these register bits is 0x8 for NTSC" to register 0x3033[7:4]

version 2.3 02.05.2013

- in section 9.1, updated figure 9-1 and added parameters to table 9-1 for image plane height, tilt between die and glass, and die rotation
- in section 9.2, updated figure 9-2 and replaced table 9-2 with new table

version 2.31 08.27.2013

- in chapter 2, updated figure 2-2
- in section 4.4, added figure 4-6

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