OXFORD SEMICONDUCTOR

Data Sheet

# OXE800DSE
## Network Attached Storage Device

## Features

- Flexible, extendable storage
  - Seamless interface to 2 internal SATA drives, expandable via PCI SATA bridge chips
- Accessible from multiple clients using Ethernet (integrated 10/100 Ethernet MAC) or 802.11 WiFi (via PCI WiFi chips)
- 200-MHz ARM926EJ-S processor with 32-Kbyte caches & MMU
- Network coprocessor
  - TCP / IP acceleration
- Supports multiple software architectures
  - Linux OS
  - TCP/IP & CIFS
  - EXT3
- Simple to install—no specialist user knowledge necessary; automatic installation with DHCP client & simple configuration
- RAID 1 hardware accelerator
- Integrated fan/tacho/PWM
- AES-based encryption supports multiple authentication methods & devices for secure storage of user data
- 5-channel DMA controller
- USB 2.0 & USB full-speed host controllers
- 32-Kbyte on-chip SRAM
- DDR SDRAM controller with selectable 8 & 16-bit interface supports combinations up to 64 Mbytes addressable storage
- 16-bit static memory interface (optional—device boots from HDD) supports up to 4 Mbytes addressable storage per chip-select
- 0.13-µm CMOS process with 1.2-V core
- 19 mm×19 mm 272-pin PBGA (1-mm ball pitch)

## Overview

The OXE800DSE delivers a powerful network storage product combined with software that prioritizes ease of use. These primary characteristics make it ideal for customers without specialized IT knowledge and especially useful in the small office or the home, where the RAID and encryption facilities of the OXE800DSE are particularly suitable for storing critical data such as sensitive information and digital photos.

The OXE800DSE combines a wealth of potential with low cost of ownership. It delivers a high level of integration and its minimal requirements for external components render it particularly suitable for the following application areas:

- Networked consumer PC cluster
- Small office/home office
- Consumer media storage or server device

## Functionality

The Oxford Semiconductor OXE800DSE is a network-attached storage (NAS) device with advanced encryption capabilities which allow it to store data securely. It offers diverse connectivity including 10/100 Ethernet plus CIFS over TCP/IP, and EXT3 with optional RAID capabilities.

This adaptable and highly-configurable device also supports connections to 802.11 and other standard wireless chips via mini PCI. It provides two integrated SATA cores (expandable via a PCI bus), a USB high-speed port and two USB full-speed host ports with print server function, and additional expansion capability via USB HDDs. The RAID controller provides a high-level control interface with a common data path from the enhanced DMA engine to either or both SATA blocks. It supports RAID1, disk spanning or two independent disk configurations, and also a port multiplier for expanded configurations on either port.

An integrated ARM926EJ-S processor, featuring an MMU and 32-Kbyte caches, runs Linux OS with a full network stack. For off-chip control, the integrated fan/tachometer/pulse width modulator provides counter functionality and a thermistor circuit. Used in conjunction, these facilities can optionally trigger and modulate a fan or initiate protective measures. Alternatively, the core can be used to provide low-resolution analogue output controls for any other function.

Figure 1 shows the OXE800DSE.

***Figure 1 OXE800DSE***

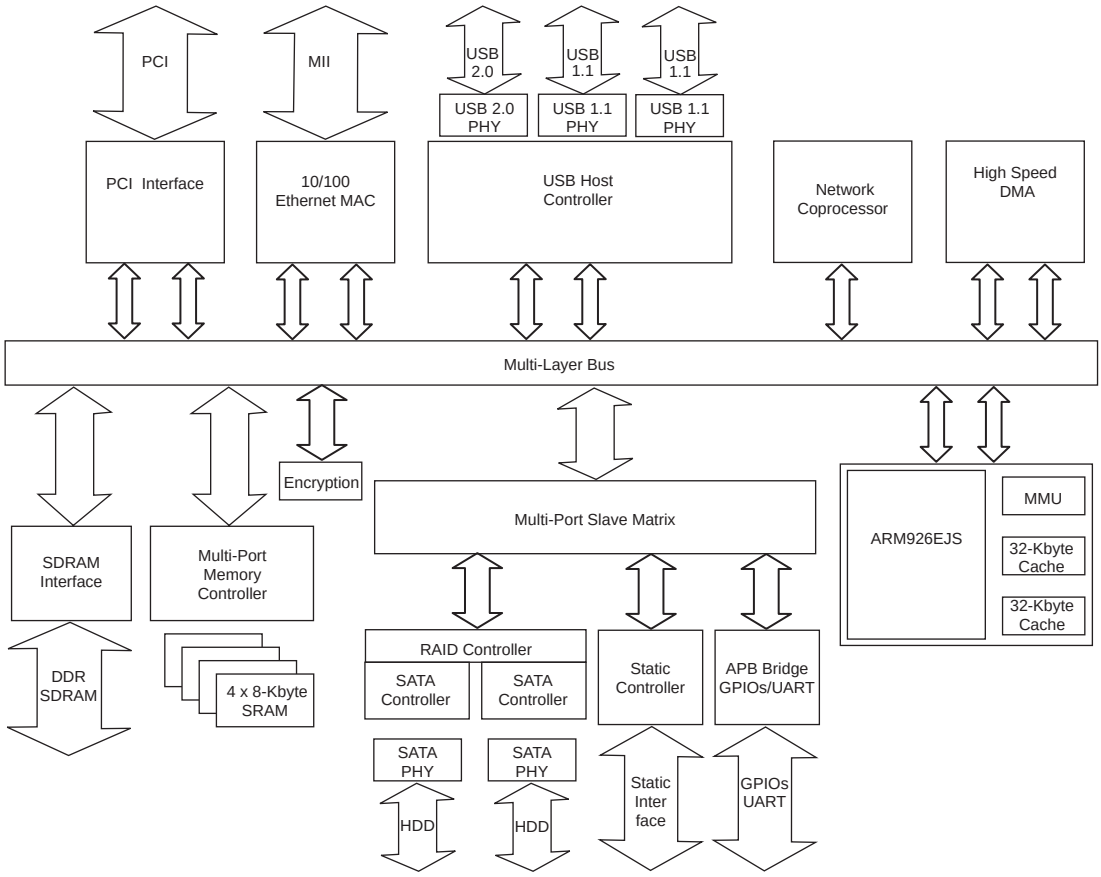



Figure 2 shows a sample low-cost application in which the OXE800DSE uses a single 25-MHz crystal and can boot directly from disk without the need for flash memory.

***Figure 2 Sample OXE800DSE Boot-From-HDD Application***

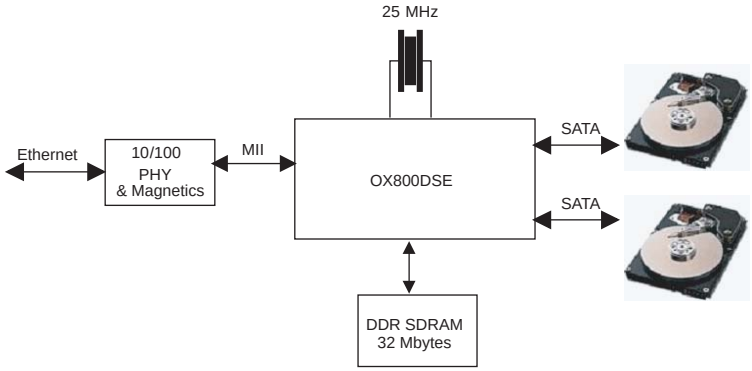
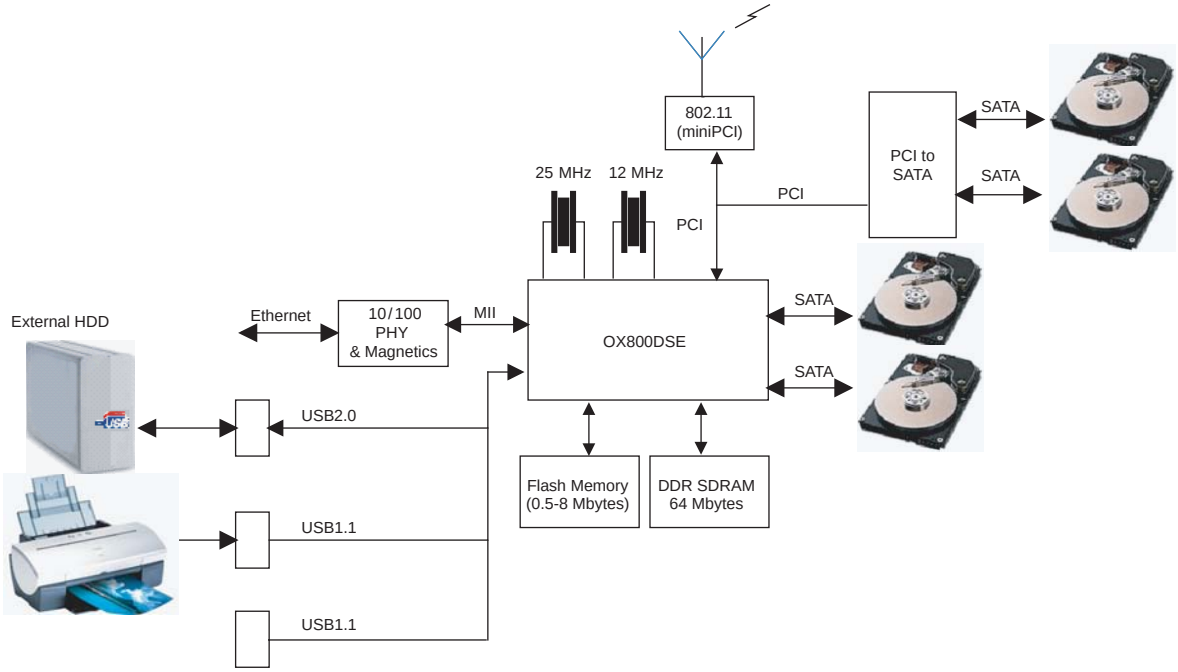


Figure 3 exemplifies a more-capable application in which the capacity of the OXE800DSE has been expanded to support four SATA drives in addition to an Ethernet connection, external HDD and printer.

***Figure 3 Sample Four-SATA OXE800DSE Application***



# Operating Conditions

Tables 1 and 2 detail the required operating conditions for the device.

*Table 1 Absolute Maximum Device Ratings*

| Symbol | Parameter | Rating | Max | Units |
|---|---|---|---|---|
| $V_{DD}$ | DC supply voltage | 1.2 V<br>3.3 V | 1.8<br>3.8 | V |
| $V_{IN}$ | DC input voltage | 2.5-V input buffer<br>3.3-V input buffer<br>3.3-V interface/5-V tolerant input buffer | 3.6<br>4.8<br>6.5 | V |
| $V_{OUT}$ | DC output voltage | 2.5-V output buffer<br>3.3-V output buffer<br>3.3-V interface/5-V tolerant output buffer | 3.6<br>4.8<br>6.5 | V |
| $T_{STG}$ | Storage temperature | Storage temperature | –40 to 85 | °C |

*Table 2 Recommended Operating Conditions*

| Symbol | Parameter | Rating | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{DD}$ | DC supply voltage for internal<br><br>DC supply voltage for I/O block | 1.2 V<br>3.3 V<br><br>2.5-V I/O | 1.14<br>3.0<br><br>2.3 | 1.26<br>3.6<br><br>2.7 | V |
| $V_{IN}$ | DC input voltage | 2.5-V input buffer<br>3.3-V input buffer<br>3.3-V interface/5-V tolerant input buffer | 2.3<br>3.0<br>3.0 | 2.7<br>3.6<br>5.25 | V |
| $V_{OUT}$ | DC output voltage | 2.5-V output buffer<br>3.3-V output buffer<br>3.3-V interface/5-V tolerant output buffer | 2.3<br>3.0<br>3.0 | 2.7<br>3.6<br>3.6 | |
| $T_A$ | Ambient temperature range | | 0 | 70 | °C |

# Electrical Characteristics

Table 3 details the required DC electrical characteristics for the device.

*Table 3 3.3-V I/O Buffer Electrical Characteristics*

| Symbol | Parameter | Condition | Min | Type | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | CMOS Interface | 2.0 | | | V |
| $V_{IL}$ | Input low voltage | CMOS Interface | | | 0.8 | V |
| VT | Switching threshold | | | 1.4 | | V |
| $VT^+$ | Schmitt trigger, positive-going threshold | CMOS | | | 2.0 | V |
| $VT^-$ | Schmitt trigger, negative-going threshold | CMOS | 0.8 | | | V |
| $I_{IH}$ | Input high current:<br>Input buffer<br>Input buffer with pull-down | $V_{IN} = V_{DD}$ | <br>–10<br>10 | <br><br>33 | <br>10<br>60 | µA |
| $I_{IL}$ | Input low current:<br>Input buffer<br>Input buffer with pull-up | $V_{IN} = V_{SS}$ | <br>–10<br>–60 | <br><br>–33 | <br>10<br>–10 | µA |
| $V_{OH}$ | Output high voltage | $I_{OH}$ = –1 µA<br>$I_{OH}$ = –1 mA to –24 mA | $V_{DD}$ – 0.05<br>2.4 | | | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = 1 µA<br>$I_{OL}$ = 1 mA to 24 mA | | | 0.05<br>0.4 | V |
| $I_{OZ}$ | Tri-state output leakage current | $V_{OUT} = V_{SS}$ or $V_{DD}$ | -10 | | 10 | µA |
| $I_{DD}$ | Quiescent supply current | | | | 100 | µA |
| $C_{IN}$ | Input capacitance | Any input & bidirectional buffers | | | 4 | pF |
| $C_{OUT}$ | Output capacitance | Any output buffer | | | 4 | pF |

# Power Consumption

Table 4 gives typical power consumption figures for the OXE800DSE on a quad test board with the following additional features:

- The VIA PCI SATA chip has been removed
- The 10/100 PHY has been removed
- A PCI Gb PHY is being used

*Table 4 OXE800DSE Power Consumption*

| | | System Idle After Login | | Max Reading/Writing Data to the Disk | |
|---|---|---|---|---|---|
| | | mA | W | mA | W |
| 1.2 V | Total | 377 | | 403 | |
| 3.3 V | Total | 167 | | 180 | |
| 2.5 V | Total | 184 | | 329 | |
| Package power | | | 1.4365 | | 1.8803 |

# Pinout & Package Information

The OXE800DSE is supplied as a 272-pin PBGA package.

Figure 4 shows the OXE800DSE pin layout.

***Figure 4 OXE800DSE Pin Layout***

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | VSS | GPIO_27 | GPIO_29 | GPIO_32 | MEM_DQ15 | MEM_DQ12 | MEM_DQS1 | MEM_DQ9 | MEM_VREF1 | MEM_A13 | MEM_A11 | MEM_A10 | MEM_FBCK | MEM_CK | MEM_A4 | MEM_A3 | MEM_A1 | MEM_VREF0 |
| B | GPIO_24 | GPIO_26 | GPIO_28 | GPIO_31 | GPIO_34 | MEM_DQ13 | MEM_DQ11 | MEM_DQ8 | MEM_CS_N1 | MEM_A12 | MEM_A9 | MEM_A7 | MEM_A5 | MEM_CK_N | MEM_A2 | MEM_A0 | MEM_RAS_N | MEM_DM0 |
| C | GPIO_21 | GPIO_23 | GPIO_25 | GPIO_30 | GPIO_33 | MEM_DQ14 | MEM_DQ10 | MEM_DM1 | MEM_CAS_N | MEM_A8 | MEM_A6 | VSS_MEM | MEM_BA1 | MEM_BA0 | MEM_WE_N | MEM_CS_N0 | MEM_DQ7 | MEM_DQ4 |
| D | GPIO_18 | GPIO_19 | GPIO_22 | VDD33 | VSS | VSS_MEM | VSS_MEM | VDD12_MEM | VSS_MEM | MEM_CKE | VDD25_MEM | VDD12_MEM | VSS_MEM | MEM_DQ5 | MEM_DQ6 | MEM_DQS0 | MEM_DQ3 | MEM_DQ2 |
| E | GPIO_13 | GPIO_14 | GPIO_20 | VDD12 | VSS_MEM | VDD25_MEM | | | | | | | VDD25_MEM | VSS_MEM | VDD12_MEM | MEM_DQ0 | MEM_DQ1 | SATA_CLKO |
| F | GPIO_6 | GPIO_12 | GPIO_15 | GPIO_17 | VDD25_MEM | | | | | | | | | SATA_VDDOSC | SATA_VSSOSC | SATA_VSS | SATA_VSS | SATA_CLKI |
| G | TEST_EN | HIGH_Z_N | GPIO_7 | GPIO_16 | | | VSS_MEM | VDD25_MEM | VSS_MEM | VSS_MEM | VSS_MEM | VDD25_MEM | | | SATA0_REXT | SATA0_VDDTX | SATA0_TXP | SATA0_TXN |
| H | USBC_DM | USBC_DP | RESET_N | GPIO_8 | | | VSS | VDD12 | VDD25_MEM | VDD25_MEM | SATA_VSSPLL | SATA_VSSPLL | | | SATA_VSS | SATA1_VDDRX | SATA0_RXN | SATA0_RXP |
| J | USBB_DM | USBB_DP | MII_MDIO | MII_MDC | | | USB_VDD12 | VSS | VDD33 | VSS | SATA_VDDPLL | SATA_VDDPLL | | | SATA_VSS | SATA0_VDDRX | SATA_VSS | SATA_VSS |
| K | USB_VSSA33C | USB_VSS12 | USB_VDDA33T1 | USB_VDD12 | | | USB_VSS12 | USB_VDDA33T1 | USB_VSSA33T1 | VSS | SATA_VDDPLL | SATA_VDDPLL | | | SATA_VSS | SATA1_VDDTX | SATA1_RXP | SATA1_RXN |
| L | USBA_DP | USBA_DM | USB_VSSA33T1 | USB_REXT | | | VDD12 | VSS | VSS | VDD33 | SATA_VSSPLL | SATA_VSSPLL | | | SATA1_REXT | VDD12A_PLLA | SATA1_TXN | SATA1_TXP |
| M | USB_VSSA33T1 | USB_VDDA33C | USB_X0 | MII_TXEN | | | VSS | VDD12 | VDD33 | VSS | VSS | VDD12 | | | PLLA_FILT | VSSD_PLLA | VBBD_PLLA | SATA_VSS |
| N | USB_X1 | USB_ANALOG_TEST | MII_CRS | MII_TXD0 | NC | | | | | | | | | PCI_AD30 | PCI_AD31 | VDD12-PCI | VDD12A_PLLA | VSSA_PLLA |
| P | CLKO | MII_COL | MII_TXD2 | NC | MII_TXER | VDD33 | | | | | | | PCI_AD24 | PCI_AD29 | PCI_AD28 | PCI_AD27 | PCI_AD26 | PCI_AD25 |
| R | MII_TXD1 | MII_TXD3 | NC | MII_RXDV | MII_RXD2 | NC | GPIO_11 | GPIO_4 | PCI_AD12 | PCI_AD14 | PCI_AD17 | PCI_PAR | PCI_AD21 | PCI_C_BE_N3 | VSS-PCI | VSS | PCI_AD23 | PCI_AD22 |
| T | NC | MII_RXER | MII_RXD1 | NC | NC | GPIO_5 | GPIO_3 | PCI_AD0 | VDD12-PCI | VSS-PCI | VDD33 | VDD33 | VDD33 | VDD33 | VSS | VSS | PCI_AD20 | PCI_AD19 |
| U | NC | MII_RXD0 | NC | GPIO_10 | GPIO_9 | GPIO_2 | GPIO_0 | PCI_AD2 | PCI_AD4 | PCI_AD7 | PCI_AD8 | PCI_AD11 | PCI_AD15 | PCI_DEVSEL_N | PCI_FRAME_N | PCI_IRDY_N | PCI_AD16 | PCI_AD18 |
| V | MII_TXCLK | MII_RXD3 | MII_RXCLK | VSS | PCI_CLK | GPIO_1 | PCI_AD1 | PCI_AD3 | PCI_AD5 | PCI_AD6 | PCI_C_BE_N0 | PCI_AD9 | PCI_AD10 | PCI_AD13 | PCI_C_BE_N1 | PCI_STOP_N | PCI_TRDY_N | PCI_C_BE_N2 |

Table 5 on page 9 details the pin allocations for the device.

*Table 5 OXE800DSE Pin Allocations (Sheet 1 of 4)*

| Ball | No. Bits | Type[(1)] | Name | Description |
|---|---|---|---|---|
| Clocks, Reset & Mode (6 pins) | | | | |
| P1 | 1 | O | CLKO | 25-MHz reference clock out |
| H4 | 1 | I | RESET_N | Reset input |
| G2 | 1 | I | HIGH_Z_N | Force all inputs to high impedance |
| G1 | 1 | I | TEST_EN | Enable test (JTAG) |
| F18 | 1 | I | SATA_CLKI | 25-MHz reference clock input; either crystal oscillator or external clock |
| E18 | 1 | O | SATA_CLKO | Reference clock output. Crystal oscillator output |
| Ethernet Interface (18 pins) | | | | |
| R2,P3,R1,N4 | 4 | O | MII_TXD[3:0] | Transmit data—100 Mbps<br>MII[3:0]—MII @ 25 MHz |
| V2,R5,T3,U2 | 4 | I | MII_RXD[3:0] | Receive data—100 Mbps<br>MII[3:0]—MII @ 25 MHz |
| J3 | 1 | B | MII_MDIO | MDIO serial data |
| J4 | 1 | O | MII_MDC | MDIO clock |
| N3 | 1 | I | MII_CRS | Carrier sense |
| P5 | 1 | O | MII_TXER | Transmit error |
| T2 | 1 | I | MII_RXER | Receive error |
| V1 | 1 | I | MII_TXCLK | MII transmit clock in—25 MHz |
| V3 | 1 | I | MII_RXCLK | MII receive clock—25 MHz |
| M4 | 1 | O | MII_TXEN | Transmit enable |
| R4 | 1 | I | MII_RXDV | Receive data valid |
| P2 | 1 | I | MII_COL | Collision detect |
| SDRAM (47 pins) | | | | |
| A14 | 1 | 2V5_O | MEM_CK | Differential clock (non-inverted) |
| B14 | 1 | 2V5_O | MEM_CK_N | Differential clock (inverted) |
| A13 | 1 | 2V5_I | MEM_FBCK | Feedback clock |
| D10 | 1 | 2V5_O | MEM_CKE | Clock enable |
| B9,C16 | 2 | 2V5_O | MEM_CS_N[1:0] | Chip selects |
| B17 | 1 | 2V5_O | MEM_RAS_N | Read address strobe |
| C9 | 1 | 2V5_O | MEM_CAS_N | Column address strobe |
| C15 | 1 | 2V5_O | MEM_WE_N | Write enable |
| C13,C14 | 2 | 2V5_O | MEM_BA[1:0] | Bank address |
| A10,B10,A11,A12,B11,C10,B12, C11,B13,A15,A16,B15, A17,B16 | 14 | 2V5_O | MEM_A[13:0] | Address |
| A7,B7,D8,B8,D9,B9,A9,A10, D17,C20,D19,E17,E19,E20, F17,F19 | 16 | 2V5_B | MEM_DQ[15:0] | Data input/output |
| A7,D16 | 2 | 2V5_B | MEM_DQS[1:0] | Data in/out strobes |
| C8,B18 | 2 | 2V5_O | MEM_DM[1:0] | Data mask |

*Table 5 OXE800DSE Pin Allocations (Sheet 2 of 4)*

| Ball | No. Bits | Type[(1)] | Name | Description |
|---|---|---|---|---|
| A9,A18 | 2 | A | MEM_VREF[1:0] | Voltage references (1.25 V) for SSTL-2 |
| PCI (43 pins) | | | | |
| N15,N14,P14,P15,P16,P17, P18,P13,R17,R18,R13,T17,T18, U18,R11,U17,U13,R10,V14,R9, U12,V13,V12,U11,U10,V10,V9, U9,V8,U8,V7,T8 | 32 | B | PCI_AD[31:0] | PCI address & data.<br>PCI_AD[15:0]—PCI address & data (lower 16 bits) also serves as STATIC_A[15:0] lower 16 bits of static memory address.<br>PCI_AD[31:16]—PCI address & data (upper 16 bits) also serves as STATIC_D[15:0] static memory controller bus |
| U14 | 1 | B | PCI_DEVSEL_N | PCI device selection |
| U16 | 1 | B | PCI_IRDY_N | PCI initiator ready |
| V17 | 1 | B | PCI_TRDY_N | PCI target ready |
| R14,V18,V15,V11 | 4 | B | PCI_C_BE_N[3:0] | PCI command/byte enable |
| V5 | 1 | I | PCI_CLK | PCI clock |
| V16 | 1 | B | PCI_STOP_N | PCI stop |
| U15 | 1 | B | PCI_FRAME_N | PCI frame |
| R12 | 1 | B | PCI_PAR | PCI parity |
| G3,F1,T6,R8 | 4 | I | PCI_REQ[3:0] | PCI host arbiter bus requests. Shared with GPIO |
| T7, U6,V6,U7 | 4 | O | PCI_GNT[3:0] | PCI host arbiter bus grants. Shared with GPIO |
| R7, U4,U5,H4 | 4 | O | PCI_CKO | Programmable PCI output clocks. Shared with GPIO |
| Static memory interface | | | | |
| N15,N14,P14,P15,P16,P17, P18,P13,R17,R18,R13,T17,T18, U18,R11,U17 | 16 | B | STATIC_D[15:0] | Static memory controller data bus. Shared with PCI |
| U13,R10,V14,R9,U12,V13,V12, U11,U10,V10,V9,U9,V8,U8,V7, T8 | 16 | O | STATIC_A[15:0] | Lower 16 bits of static memory controller address. Shared with PCI |
| D1,F4,C4,F3,E2,E1 | 6 | O | STATIC_A[21:16] | Upper 16 bits of static memory controller address. Shared with GPIO |
| E3,D2 | 2 | O | STATIC_CS_N[1:0] | Shared with GPIO |
| D3,C1 | 2 | O | STATIC_WE_N[1:0] | Shared with GPIO |
| F2 | 1 | O | STATIC_OE_N | Shared with GPIO |
| SATA 0 (5 pins) | | | | |
| H18 | 1 | I | SATA0_RXP | Receive differential data (+); differential inputs to the PHY. Terminals receive NRZ data at 1.5 or 3.0 Gbps |
| H17 | 1 | I | SATA0_RXN | Receive differential data (–); differential inputs to the PHY. Terminals receive NRZ data at 1.5 or 3.0 Gbps |
| G18 | 1 | O | SATA0_TXN | Transmit differential data (–); differential outputs to the PHY. Terminals transmit NRZ data at 1.5 or 3.0 Gbps |
| G17 | 1 | O | SATA0_TXP | Transmit differential data (+); differential outputs to the PHY. Terminals transmit NRZ data at 1.5 or 3.0 Gbps |

*Table 5 OXE800DSE Pin Allocations (Sheet 3 of 4)*

| Ball | No. Bits | Type[1] | Name | Description |
|---|---|---|---|---|
| G15 | 1 | A | SATA0_REXT | External 1-K ±1% Ω reference resistor |
| SATA 1 (5 pins) | | | | |
| K17 | 1 | I | SATA1_RXP | Receive differential data (+); differential inputs to the PHY. Terminals receive NRZ data at 1.5 or 3.0 Gbps |
| K18 | 1 | I | SATA1_RXN | Receive differential data (–); differential inputs to the PHY. Terminals receive NRZ data at 1.5 or 3.0 Gbps |
| L17 | 1 | O | SATA1_TXN | Transmit differential data (–); differential outputs to the PHY. Terminals transmit NRZ data at 1.5 or 3.0 Gbps |
| L18 | 1 | O | SATA1_TXP | Transmit differential data (+); differential outputs to the PHY. Terminals transmit NRZ data at 1.5 or 3.0 Gbps |
| L15 | 1 | A | SATA1_REXT | External 1-K ±1% Ω reference resistor |
| USB2.0 Port A (6 pins) | | | | |
| N2 | 1 | A | USB_ANALOG_ TEST | |
| N1 | 1 | I | USB_XI | 12-MHz crystal oscillator XI signal |
| M3 | 1 | O | USB_XO | Crystal oscillator XO signal |
| L2 | 1 | B | USBA_DM | Differential data minus—480 Mbps |
| L1 | 1 | B | USBA_DP | Differential data plus—480 Mbps |
| L4 | 1 | A | USB_REXT | External 3.6-K ±1% Ω reference resistor |
| USB1.1 Port B (2 pins) | | | | |
| J1 | 1 | B | USBB_DM | Differential data minus—12 Mbps |
| J2 | 1 | B | USBB_DP | Differential data plus—12 Mbps |
| USB1.1 Port C (2 pins) | | | | |
| H1 | 1 | B | USBC_DM | Differential data minus—12 Mbps |
| H2 | 1 | B | USBC_DP | Differential data plus—12 Mbps |
| MISC (1 pin) | | | | |
| M15 | 1 | A | PLLA_FILT | System PLL filter |
| GPIO (35 pins) | | | | |
| B5,C5,A4,B4,C4,A3,B3,A2,B2, C3,B1,C2,D3,C1,E3,D2,D1,F4, G4,F3,E2,E1,F2,R7,U4,U5,H4, G3,F1,T6,R8,T7, U6,V6,U7 | 35 | B | GPIO[34:0][2] | General purpose I/O pins. Uses depend on pin multiplexing, including PCI, UART, audio, PWM & static signals |
| Power & Ground (91 pins) | | | | |
| N17 | 1 | P | VDD12A_PLLA | System PLL analog 1.2-V supply |
| L16 | 1 | P | VDD12D_PLLA | System PLL digital 1.2-V supply |
| M16 | 1 | P | VSSD_PLLA | System PLL ground |
| N18 | 1 | P | VSSA_PLLA | System PLL ground |
| M17 | 1 | P | VBBD_PLLA | System PLL bulk bias (0 V) |
| K16 | 1 | P | SATA1_VDDTX0 | SATA Tx power (1.2 V) |

*Table 5 OXE800DSE Pin Allocations (Sheet 4 of 4)*

| Ball | No. Bits | Type[(1)] | Name | Description |
|---|---|---|---|---|
| G16 | 1 | P | SATA0_VDDTX0 | SATA Tx power (1.2 V) |
| H16 | 1 | P | SATA1_VDDRX0 | SATA Rx power (1.2 V) |
| J16 | 1 | P | SATA0_VDDRX1 | SATA Rx power (1.2 V) |
| L11,L12,H11,H12 | 4 | P | SATA_VSSPLL | SATA PLL ground |
| K12,K11,J11,J12 | 4 | P | SATA_VDDPLL | PLL supply (1.2 V) |
| F15 | 1 | P | SATA_VSSOSC | SATA ground for the crystal oscillator |
| F14 | 1 | P | SATA_VDDOSC | SATA 3.3-V power supply for the crystal oscillator |
| F16,F17,H15,J15,J17,J18,K15, M18 | 8 | P | SATA_VSS | Ground |
| M2 | 1 | P | USB_VDDA33C | Analog 3.3-V supply |
| K1 | 1 | P | USB_VSSA33C | Analog ground |
| K4,J7 | 2 | P | USB_VDD12 | Digital 1.2-V supply |
| K7,K2 | 2 | P | USB_VSS12 | Digital ground |
| M1,L3,K9 | 3 | P | USB_VSSA33T1 | Analog ground |
| R3,U3 | 2 | P | USB_VDDA33T1 | Analog 3.3-V supply |
| A1,R16,T15,T16,D5,J8,M7,M10, K10,H7,L8,L9,M11,J10,V4 | 15 | P | VSS | Ground |
| E4,L7,M8,M12,H8 | 5 | P | VDD12 | 1.2-V supply |
| D4,J9,P6,M9,L10,T11,T12,T13, T14 | 9 | P | VDD33 | 3.3-V supply |
| E13,G12,D11,H10,H9,G8,E6,F5 | 8 | P | VDD25_MEM | 2.5-V SDRAM interface supply |
| E14,C12,D7,D13,G11,D9,G10, G9,G7,D6,E5 | 11 | P | VSS_MEM | SDRAM interface ground |
| E15,D12,D8 | 3 | P | VDD12_MEM | 1.2-V SDRAM interface supply |
| N16,T9 | 2 | P | VDD12_PCI | 1.2-V PCI bus interface supply |
| R15,T10 | 2 | P | VSS_PCI | PCI ground |
| NC (9 pins) | | | | |
| N5,P4,R3,T1,T5,U3,T4,R6,U1 | 9 | | | Do not connect |

**Notes:**

1 Type key: format is [(W_)X)] where the following conventions apply:

| W—Supply | | X—Type | |
|---|---|---|---|
| 5V | 5-V tolerant 3.3 V | I | Input |
| 3V3 | 3.3 V | O | Output |
| 2V5 | 2.5 | B | Bidirectional |
| | | A | Analog |

2 Any of the 35 GPIO pins on the device can be assigned to a primary function, a secondary function or bit-programmable general-purpose I/O in response to peripheral control register tertiary settings.JTAG must not be enabled in conjunction with HIGH_Z_N asserted low.

Figures 5 and 6 show the OXE800DSE package.

***Figure 5 OXE800DSE Package—Top & Side View***

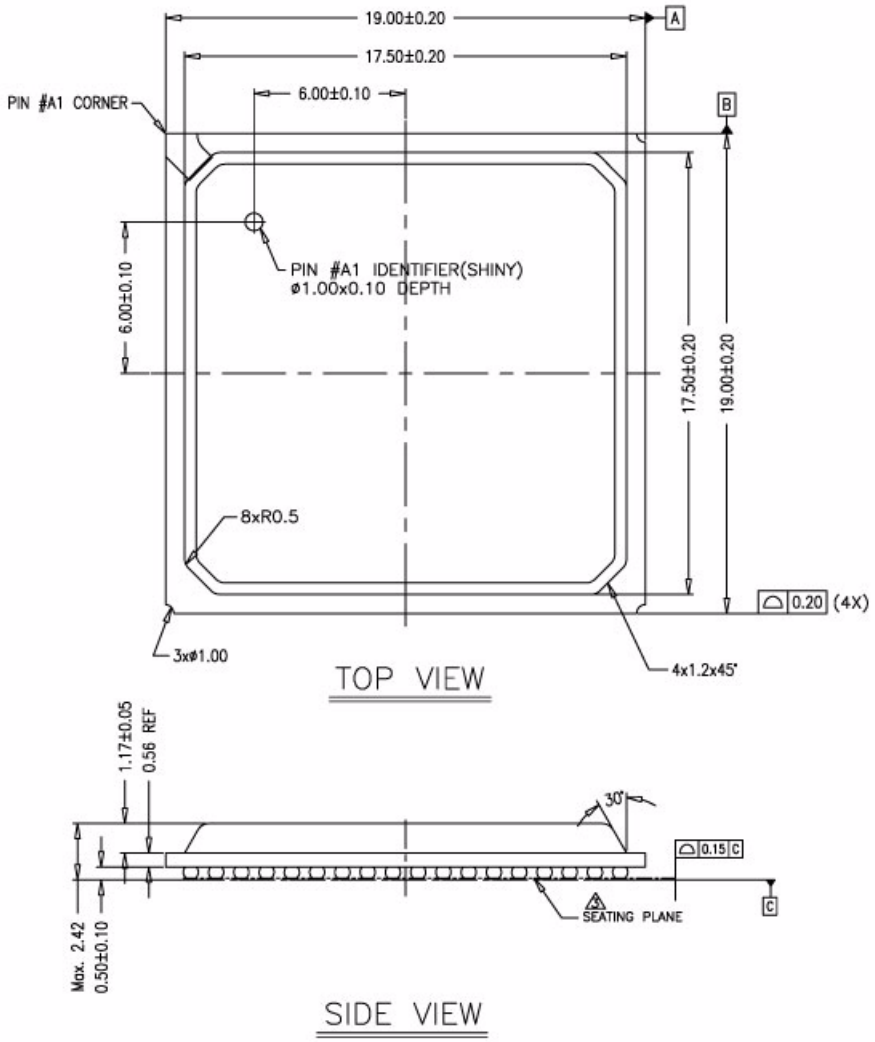
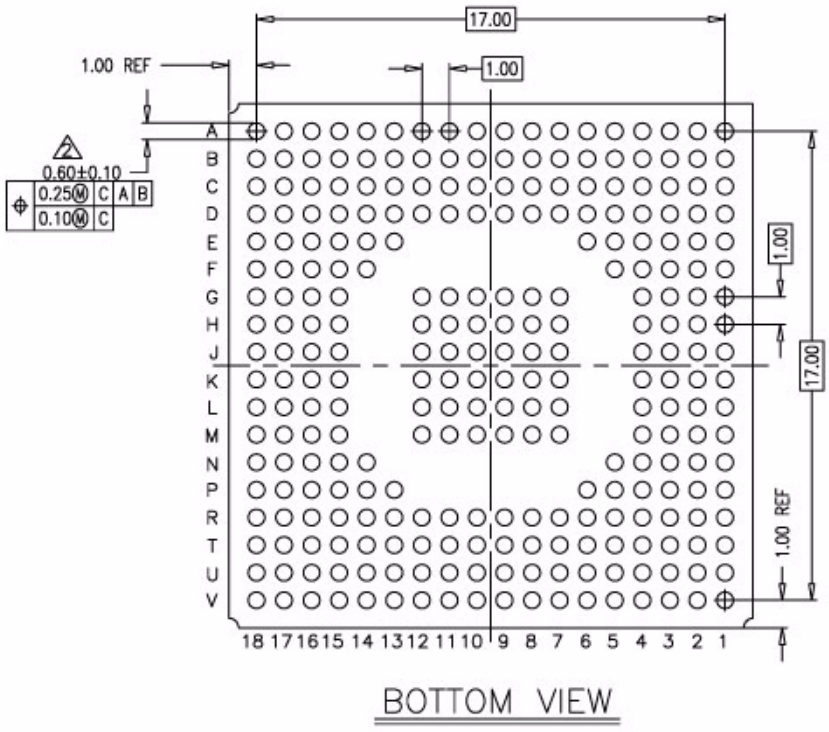


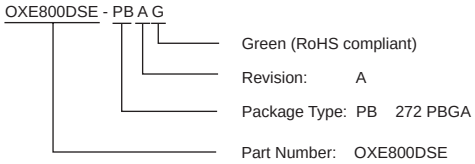
***Figure 6 OXE800DSE Package—Bottom View***




## Ordering Information

The order code for the Oxford Semiconductor OXE800DSE is OXE800DSE-PBAG.

The following conventions are used to identify Oxford Semiconductor products:




## Revision Information

Table 6 documents the revisions of this guide.

*Table 6 Revision Information*

| Revision | Modification |
|---|---|
| Sep 06 | First publication |
| Mar 07 | Package information corrected; device characteristics & operating conditions added; document category changed to External—Free Release |
| Jul 07 | Feature revision |
| Oct 07 | Feature revision |

## Application Notes

The following application notes apply to the OXE800DSE:

TBD

## Contacting Oxford Semi-conductor

See the Oxford Semiconductor website (http://www.oxsemi.com) for further details about Oxford Semiconductor devices, or email sales@oxsemi.com.

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