OZ6812

Designed for
Microsoft®
Windows®2000
Professional
Windows® NT
Workstation 4.0
Windows® 98

ACPI CardBus Controller

FEATURES

The OZ6812 is a PCMCIA R2/CardBus controller, providing the most advanced design flexibility for PC Cards that interface with advanced notebook designs.

- ACPI-PCI Bus Power Management Interface Specification Rev 1.1 Compliant
- Supports OnNow LAN wakeup, OnNow Ring Indicate, PCI CLKRUN#, PME#, and CardBus CCLKRUN#
- Compliant with PCI specification V2.2, 1998 PC Card Standard 7.0
- Yenta™ PCI to PCMCIA CardBus Bridge register compatible
- ExCA (Exchangeable Card Architecture) compatible registers mappable in memory and I/O space
- Intel™ 82365SL PCIC Register Compatible
- Supports PCMCIA_ATA Specification
- Supports 5V/3.3V PC Cards and 3.3V CardBus cards
- Supports single PC Card or CardBus slot with hot insertion and removal
- Supports multiple FIFOs for PCI/CardBus data transfer
- Supports Direct Memory Access for PC/PCI and PCI/Way on PC Card socket
- Programmable interrupt protocol: PCI, PCI+ISA, PCI/Way, or PC/PCI interrupt signaling modes
- Win'98 IRQ and PC-98/99 compliant
- Parallel or Serial interface for socket power control devices including Micrel and TI
- Zoomed Video Support
- Integrated PC 98/99 -Subsystem Vendor ID support, with auto lock bit
- LED Activity Pins

ORDERING INFORMATION

OZ6812T - 144pin LQFP
OZ6812B - 144pin Mini-BGA

GENERAL DESCRIPTION

The OZ6812 is an ACPI and PC98/99 logo certified, high performance, single slot PC Card controller with a synchronous 32-bit bus master/target PCI interface. This PC Card t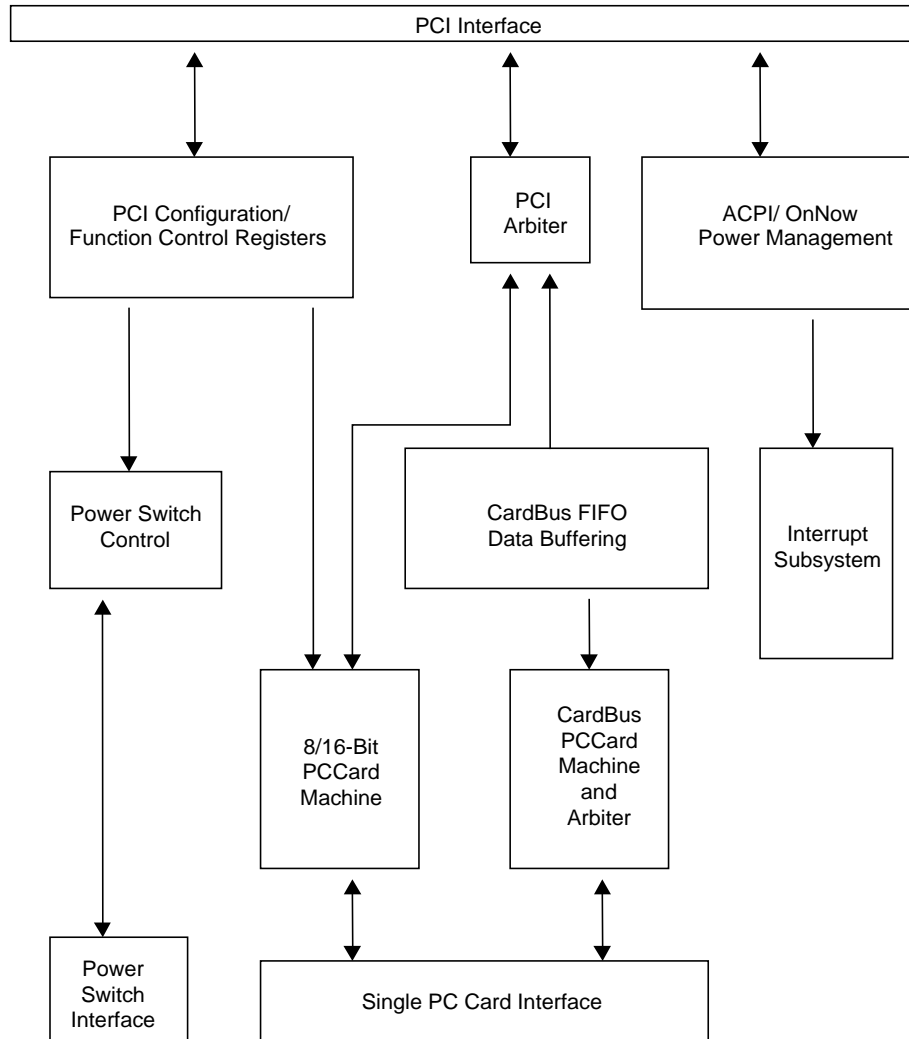o PCI bridge host controller is compliant with the 1998 PC Card Standard. This standard incorporates the new 32-bit CardBus while retaining the 16-bit PC Card specification as defined by PCMCIA release 2.1. CardBus is intended to support "temporal" add-in functions on PC Cards, such as Memory cards, Network interfaces, FAX/Modems and other wireless communication cards, etc. The high performance and capability of the CardBus interface will enable the development of many new functions and applications.

The OZ6812 CardBus controller is compliant with the latest ACPI-PCI Bus Power Management Interface Specification. It supports all four power states and the PME# function for maximum power savings and ACPI compliance. The device also provides a power-down mode to allow host software to reduce power consumption further by stopping internal clock distribution as well as the PC Card socket clock. In addition, an advanced CMOS process is utilized to minimize system power consumption.
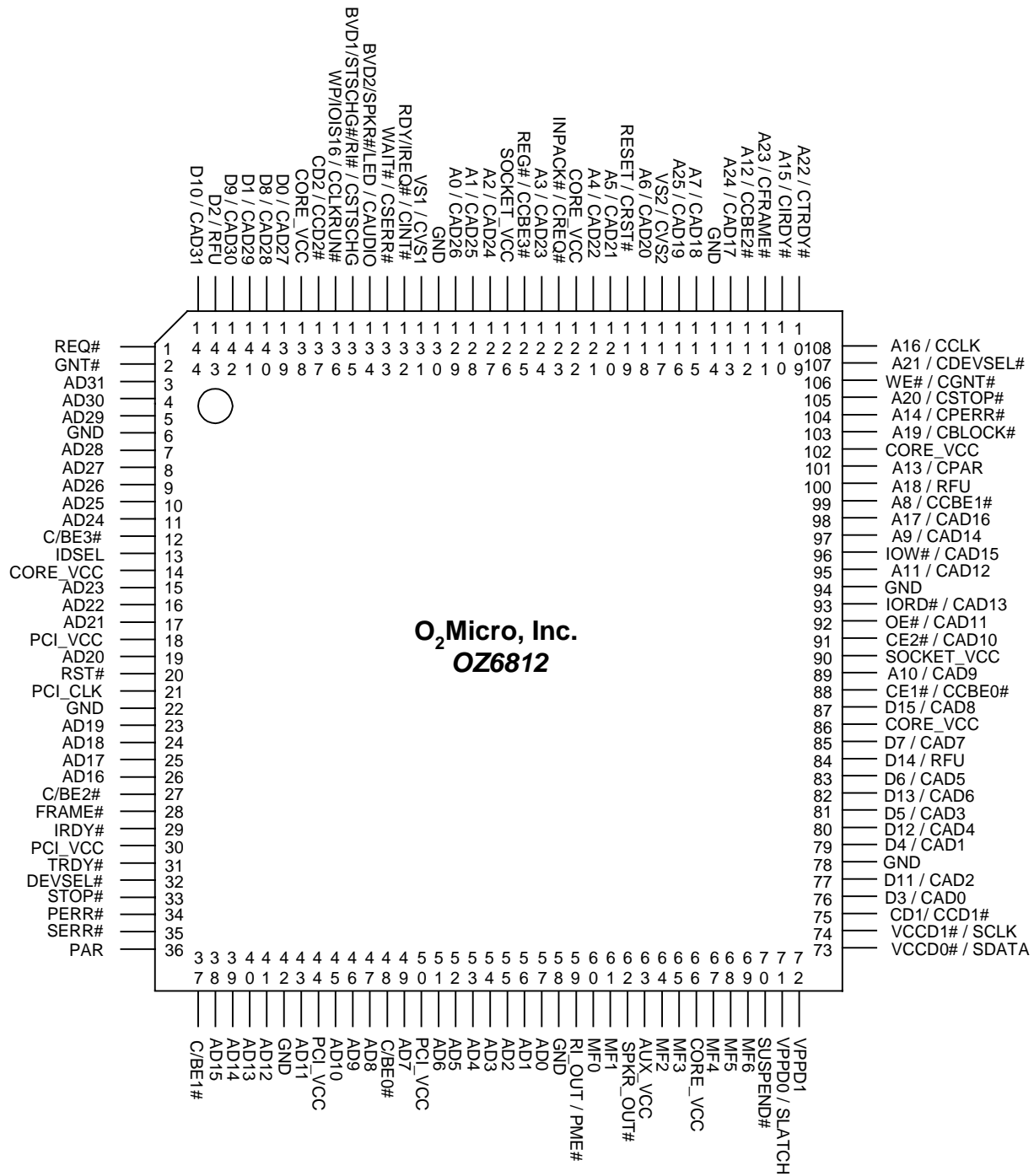
The OZ6812 single PCMCIA socket supports 3.3V/5V 8/16-bit PC Card R2 card or 32-bit CardBus R3 card. The R2 card support is compatible with the Intel 82365SL PCIC controller, and the R3 card support is fully compliant with the 1998 PC Card Standard CardBus specification. The OZ6812 is a stand alone device, which means that it does not require an additional buffer chip for the PC Card socket interface. In addition, the OZ6812 supports dynamic PC Card hot insertion and removal, with auto configuration capabilities.

The OZ6812 is fully compliant with the 33Mhz PCI Bus specification, V2.2. It supports a master device with internal CardBus direct data transfer. The OZ6812 implements a FIFO data buffer architecture between the PCI bus and CardBus socket interface to enhance data transfers to CardBus devices. The bi-directional FIFO buffer (composed of 16 double words) permits the OZ6812 to accept data from a target bus (PCI or CardBus interface) while simultaneously transferring data. This architecture not only speeds up data transfers but also prevents system deadlocks.

Functional Block Diagram

```
┌──────────────────────────────────────────────────────────────────────────┐
│                              PCI Interface                                 │
└──────────────────────────────────────────────────────────────────────────┘

┌───────────────────────┐      ┌──────────┐      ┌───────────────────────┐
│  PCI Configuration/   │      │   PCI    │      │     ACPI/ OnNow       │
│ Function Control      │      │  Arbiter │      │   Power Management     │
│ Registers             │      │          │      │                        │
└───────────────────────┘      └──────────┘      └───────────────────────┘

┌───────────────┐      ┌────────────────────┐      ┌───────────────┐
│ Power Switch  │      │   CardBus FIFO     │      │  Interrupt    │
│ Control       │      │   Data Buffering   │      │  Subsystem    │
└───────────────┘      └────────────────────┘      └───────────────┘

                  ┌──────────┐    ┌──────────┐
                  │ 8/16-Bit │    │ CardBus  │
                  │ PCCard   │    │ PCCard   │
                  │ Machine  │    │ Machine  │
                  │          │    │ and      │
                  │          │    │ Arbiter  │
                  └──────────┘    └──────────┘

┌───────────────┐      ┌────────────────────────────────────┐
│ Power         │      │      Single PC Card Interface        │
│ Switch        │      │                                      │
│ Interface     │      │                                      │
└───────────────┘      └────────────────────────────────────┘
```

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PIN DIAGRAM - 144 Pin LQFP

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Left side (pins 1–36):

Pin	Signal
1	REQ#
2	GNT#
3	AD31
4	AD30
5	AD29
6	GND
7	AD28
8	AD27
9	AD26
10	AD25
11	AD24
12	C/BE3#
13	IDSEL
14	CORE_VCC
15	AD23
16	AD22
17	AD21
18	PCI_VCC
19	AD20
20	RST#
21	PCI_CLK
22	GND
23	AD19
24	AD18
25	AD17
26	AD16
27	C/BE2#
28	FRAME#
29	IRDY#
30	PCI_VCC
31	TRDY#
32	DEVSEL#
33	STOP#
34	PERR#
35	SERR#
36	PAR

Right side (pins 108–73):

Pin	Signal
108	A16 / CCLK
107	A21 / CDEVSEL#
106	WE# / CGNT#
105	A20 / CSTOP#
104	A14 / CPERR#
103	A19 / CBLOCK#
102	CORE_VCC
101	A13 / CPAR
100	A18 / RFU
99	A8 / CCBE1#
98	A17 / CAD16
97	A9 / CAD14
96	IOW# / CAD15
95	A11 / CAD12
94	GND
93	IORD# / CAD13
92	OE# / CAD11
91	CE2# / CAD10
90	SOCKET_VCC
89	A10 / CAD9
88	CE1# / CCBE0#
87	D15 / CAD8
86	CORE_VCC
85	D7 / CAD7
84	D14 / RFU
83	D6 / CAD5
82	D13 / CAD6
81	D5 / CAD3
80	D12 / CAD4
79	D4 / CAD1
78	GND
77	D11 / CAD2
76	D3 / CAD0
75	CD1 / CCD1#
74	VCCD1# / SCLK
73	VCCD0# / SDATA

Top side (pins 144–109):

Pin	Signal
144	D10 / CAD31
143	D2 / RFU
142	D9 / CAD30
141	D1 / CAD29
140	D8 / CAD28
139	D0 / CAD27
138	CORE_VCC
137	CD2 / CCD2#
136	WP/IOIS16 / CCLKRUN#
135	BVD1/STSCHG#/RI# / CSTSCHG
134	BVD2/SPKR#/LED / CAUDIO
133	RDY/IREQ# / CINT#
132	WAIT# / CSERR#
131	VS1 / CVS1
130	A0 / CAD26
129	A1 / CAD25
128	A2 / CAD24
127	SOCKET_VCC
126	REG# / CCBE3#
125	A3 / CAD23
124	INPACK# / CREQ#
123	CORE_VCC
122	A4 / CAD22
121	A5 / CAD21
120	A6 / CAD20
119	RESET / CRST#
118	VS2 / CVS2
117	A25 / CAD19
116	A7 / CAD18
115	GND
114	A24 / CAD17
113	A12 / CCBE2#
112	A23 / CFRAME#
111	A15 / CIRDY#
110	A22 / CTRDY#

Bottom side (pins 37–72):

Pin	Signal
37	C/BE1#
38	AD15
39	AD14
40	AD13
41	AD12
42	GND
43	PCI_VCC
44	AD11
45	AD10
46	AD9
47	AD8
48	C/BE0#
49	AD7
50	PCI_VCC
51	AD6
52	AD5
53	AD4
54	AD3
55	AD2
56	AD1
57	AD0
58	GND
59	RI_OUT / PME#
60	MF0
61	MF1
62	SPKR_OUT#
63	AUX_VCC
64	MF2
65	MF3
66	CORE_VCC
67	MF4
68	MF5
69	MF6
70	SUSPEND#
71	VPPD0 / SLATCH
72	VPPD1

Pin List

Bold Text = Normal Default Pin Name

PCI Bus Interface Pins

Pin Name	Description	Pin Number		Input	Type	Power Rail	Drive
		LQFP	BGA				
AD[31:0]	**PCI Bus Address Input / Data:** These pins connect to PCI bus signals AD[31:0]. A Bus transaction consists of an address phase followed by one or more data phases.	3-5, 7-11, 15-17, 19, 23-26, 38-41, 43, 45-47, 49, 51-57	D4, B1, C2-1, D2, E4, D1, E3, F3, F1, F2, G1, H2-3, J1, H4, M2, K4, N2, M3, N3, K5, N4, L5, N5, L6, N6, M6, L7, N7, M7, K7	TTL	I/O	PCI_Vcc	PCI Spec
C/BE[3:0]#	**PCI Bus Command / Byte Enable:** The command signaling and byte enables are multiplexed on the same pins. During the address phase of a transaction, C/BE[3:0]# are interpreted as the bus commands. During the data phase, C/BE[3:0]# are interpreted as byte enables. The byte enables are to be valid for the entirety of each data phase, and they indicate which bytes in the 32-bit data path are to carry meaningful data for the current data phase.	12, 27, 37, 48	E2, J2, N1, M5	TTL	I/O	PCI_Vcc	PCI Spec
FRAME#	**Cycle Frame:** This input indicates to the OZ6812 that a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is de-asserted, the transaction is in its final phase.	28	K1	TTL	I/O	PCI_Vcc	PCI Spec
IRDY#	**Initiator Ready:** This input indicates the initiating agent's ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#.	29	J3	TTL	I/O	PCI_Vcc	PCI Spec
TRDY#	**Target Ready:** This output indicates target Agent's the OZ6812's ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#.	31	L1	TTL	I/O	PCI_Vcc	PCI Spec
STOP#	**Stop:** This output indicates the current target is requesting the master to stop the current transaction.	33	K3	TTL	I/O	PCI_Vcc	PCI Spec
IDSEL	**Initialization Device Select:** This input is used as a chip select during configuration read and write transactions. This is a point-to-point signal. IDSEL can be used as a chip select during configuration read and write transactions.	13	E1	TTL	I	PCI_Vcc	PCI Spec
DEVSEL#	**Device Select:** This output is driven active LOW when the PCI address is recognized as supported, thereby acting as the target for the current PCI cycle. The Target must respond before timeout occurs or the cycle will terminate.	32	J4	TTL	I/O	PCI_Vcc	PCI Spec
PERR#	**Parity Error:** The output is driven active LOW when a data parity error is detected during a write phase.	34	M1	-	TO	PCI_Vcc	PCI Spec
SERR#	**System Error:** This output is driven active LOW to indicate an address parity error.	35	L2	-	TO	PCI_Vcc	PCI Spec

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Pin Name	Description	Pin Number LQFP	Pin Number BGA	Input	Type	Power Rail	Drive
PAR	**Parity:** This pin generates PCI parity and ensures even parity across AD[31:0] and C/BE[3:0]#. During the address phase, PAR is valid after one clock. With data phases, PAR is stable one clock after a write or read transaction.	36	L3	TTL	I/O	PCI_Vcc	PCI Spec
PCI_CLK	**PCI Clock:** This input provides timing for all transactions on the PCI bus to and from the OZ6812. All PCI bus signals, except RST#, are sampled and driven on the rising edge of PCI_CLK. This input can be operated at frequencies from 0 to 33 MHz.	21	G4	-	I	PCI_Vcc	-
RST#	**Device Reset:** This input is used to initialize all registers and internal logic to their reset states and place most OZ6812 pins in a HIGH-impedance state.	20	G2	-	I	AUX_Vcc	-
GNT#	**Grant**: This signal indicates that access to the bus has been granted.	2	B2	TTL	I	PCI_Vcc	PCI Spec
REQ#	**Request**: This signal indicates to the arbiter that the OZ6812 requests use of the bus.	1	A1	-	TO	PCI_Vcc	PCI Spec

Power Control and General Interface Pins

Pin Name	Description	Pin Number LQFP	Pin Number BGA	Input	Type	Power Rail	Drive
RI_OUT/ PME#	**Ring Indicate Out:** This pin is Ring Indicate when the following occurs while O$_2$ Mode Control B Register (index 2Eh) bit 7 is set to 1: 1) Power Control (Index+02h) bit 7 set to 1 2) Interrupt and General Control (Index+03h) bit 7 set to 1 3) PCI O2Micro Control 2 (Offset: D4h) bit X = 0 **Power Management Event:** A power management event is the process by which the OZ6812 can request a change of its power consumption state. Usually, a PME occurs during a request to change from a power saving state to the fully operational state.	59	M8	-	TO	Aux_Vcc	4mA
SPKR_OUT#	**Speaker Output:** This output can be used to support PC Card audio output. See O2 Mode E Register (Index + 3Eh), bit 1.	62	K8	TTL	I/O	Aux_Vcc	12mA
MF[6:0]	**Multifunction Terminal [6:0]:** See PCI Multifunction MUX Register (Offset:08h).	69-67, 65-64, 61-60	L10, K9, N11, L9, N10-9, L8	TTL	I/O	Aux_Vcc	12mA
SUSPEND#	**Suspend:** This signal is used to protect the internal registers from clearing when the PCI RST# signal is asserted. When low, this signal is used to mask the PCI RESET during suspend. This pin can be used during suspend to prevent controller reset.	70	N12	TTL	I	Aux_Vcc	-

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Pin Name	Description	Pin Number		Input	Type	Power Rail	Drive
		LQFP	BGA				
VPPD0/ SLATCH	**VPPD0:** This power input is used with parallel power control chip **SLATCH:** This output controls a serial interface power control chip.	71	M11	TTL	I/O	Aux_Vcc	12mA
VPPD1	**VPPD1:** This power input is used a parallel power interface chip.	72	L11	-	TO	Aux_Vcc	12mA
VCCD0#/ SDATA	**VCCD0#:** Rail power inputs for use with a parallel power control chip. **Serial Data:** This pin serves as output DATA pin when used with a serial interface of serial power control chip.	73	N13	TTL	I/O	Aux_Vcc	12mA
VCCD1#/ SCLK	**VCCD1#:** Rail power inputs for use with a parallel power control chip. **Serial Clock:** The input is used as a reference clock (10-100kHz, usually 32kHz) to control a serial power control chips. By setting PCI O2Micro Control 2 register (Offset:D4h) bit 13 to 1, SCLK is an output. Default is input mode.	74	M12	TTL	I/O	Aux_Vcc	12mA

PC Card Socket Interface Pins

Refer to PCI Bus Interface pin descriptions for details on CardBus function.
EXCEPTIONS: CCD[2:1]#, CAUDIO, CSTSCHG, CVS[2:1]

Pin Name	Description	Pin Number		Input	Type	Power Rail	Drive
		LQFP	BGA				
REG#/ CCBE3#	**Register Access:** During PC Card memory cycles, this output chooses between Attribute and Common Memory. During I/O cycles for non-DMA transfers, this signal is active (low). During ATA mode, this signal is always inactive. For DMA cycles on the OZ6812 to a DMA-capable card, REG# becomes DACK to the PCMCIA card. **CardBus Command Byte Enable:** In CardBus mode, this pin is the CCBE3#.	125	B8	TTL	I/O	Socket _Vcc	CardBus spec.
A[25:24]/ CAD[19, 17]	**Address:** PC Card socket address 25:24 outputs. **CardBus Address/Data:** CardBus mode, these pins are the CAD bits 19 and 17.	116, 113	B10, B11	TTL	I/O	Socket _Vcc	CardBus spec.
A23/ CFRAME#	**Address:** PC Card socket address 23 output. **CardBus Frame:** In CardBus mode, this pin is the CFRAME# signal.	111	D10	TTL	I/O	Socket _Vcc	CardBus spec.
A22/ CTRDY#	**Address:** PC Card socket address 22 output. **CardBus Target Ready:** In CardBus mode, this pin is the CTRDY# signal.	109	A13	TTL	I/O-PU	Socket _Vcc	CardBus spec.
A21/ CDEVSEL#	**Address:** PC Card socket address 21 output. **CardBus Device Select:** In CardBus mode, this pin is the CDEVSEL# signal.	107	C12	TTL	I/O-PU	Socket _Vcc	CardBus spec.
A20/ CSTOP#	**Address:** PC Card socket address 20 output. **CardBus Stop:** In CardBus mode, this pin is the CSTOP# signal.	105	D11	TTL	I/O-PU	Socket _Vcc	CardBus spec.
A19/ CBLOCK#	**Address:** PC Card socket address 19 output. **CardBus Lock:** In CardBus mode, this signal is the CBLOCK# signal used for locked transactions.	103	C13	TTL	I/O-PU	Socket _Vcc	CardBus spec.
A18/ RFU	**Address:** PC Card socket address 18 output. **Reserved:** In CardBus mode, this pin is reserved for future use.	100	D13	TTL	TO	Socket _Vcc	CardBus spec.
A17/ CAD16	**Address:** PC Card socket address 17 output. **CardBus Address/Data:** In CardBus mode, this pin is the CAD bit 16.	98	F10	TTL	I/O	Socket _Vcc	CardBus spec.
A16/ CCLK#	**Address:** PC Card socket address 16 output. **CardBus Clock:** In CardBus mode, this pin supplies the clock to the inserted card.	108	C11	TTL	I/O	Socket _Vcc	CardBus spec.

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Pin Name	Description	Pin Number		Input	Type	Power Rail	Drive
		LQFP	BGA				
A15/ CIRDY#	**Address:** PC Card socket address 15 output. **CardBus Initiator Ready:** In CardBus mode, this pin is the CIRDY# signal.	110	B12	TTL	I/O-PU	Socket _Vcc	CardBus spec.
A14/ CPERR#	**Address:** PC Card socket address 14 output. **CardBus Parity Error:** CardBus mode, this pin is the CPERR# signal.	104	E10	TTL	I/O-PU	Socket _Vcc	CardBus spec.
A13/ CPAR	**Address:** PC Card socket address 13 output. **CardBus Parity:** In CardBus mode, this pin is the CPAR signal.	101	E11	TTL	I/O	Socket _Vcc	CardBus spec.
A12/ CCBE2#	**Address:** PC Card socket address 12 output. **CardBus Command/Byte Enable:** In CardBus mode, this pin is the CCBE2# signal.	112	A12	TTL	I/O	Socket _Vcc	CardBus spec.
A[11:9]/ CAD [12,9,14]	**Address:** PC Card socket address 11:9 output. **CardBus Address/Data:** In CardBus mode, these pins are the CAD bits 12, 9 and 14.	95, 89, 97	F12, H12, E13	TTL	I/O	Socket _Vcc	CardBus spec.
A8/ CCBE1#	**Address:** PC Card socket address 8 output. **CardBus Command/Byte Enable:** In CardBus mode, this pin is the CCBE1# signal.	99	E12	TTL	I/O	Socket _Vcc	CardBus spec.
A[7:0]/ CAD[18] [20:26]	**Address:** PC Card socket address 7:0 outputs. **CardBus Address/Data:** In CardBus mode, these pins are the CAD bits 18 and 20:26.	115, 118, 120, 121, 124, 127, 128, 129	A11-10, B9, A9-7, B7, D7	TTL	I/O	Socket _Vcc	CardBus spec.
D15/ CAD8	**Data:** PC Card socket I/O data bit 15. **CardBus Address/Data:** In CardBus mode, this pin is the CAD bit 8.	87	H11	TTL	I/O	Socket _Vcc	CardBus spec.
D14/ RFU	**Data:** PC Card socket I/O data bit 14. **Reserved:** In CardBus mode, this pin is reserved for future use.	84	J12	TTL	I/O	Socket _Vcc	CardBus spec.
D[13:3]/ CAD[6, 4, 2, 31, 30, 28, 7, 5, 3, 1, 0]	**Data:** PC Card socket I/O data bits 13:3. **CardBus Address/Data:** In CardBus mode, this pin is the CAD bit 6 4, 2, 31, 30, 28, 7, 5, 3, 1, and 0, respectively.	82, 80, 77, 144, 142, 140, 85, 83, 81, 79, 76	K13-12, L12, C3, A2, D5, J13, J11, J10, L13, M13	TTL	I/O	Socket _Vcc	CardBus spec.
D2/ RFU	**Data:** PC Card socket I/O data bit 2. **Reserved:** In CardBus mode, this pin is reserved for future use.	143	B3	TTL	I/O	Socket _Vcc	CardBus spec.
D[1:0]/ CAD[29,27]	**Data:** PC Card socket I/O data bits 1:0. **CardBus Address/Data:** In CardBus mode, these pins are the CAD bits 29 and 27, respectively.	141, 139	C4, A3	TTL	I/O	Socket _Vcc	CardBus spec.
OE#/ CAD11	**Output Enable**: This output goes active (low) to indicate a memory read from the OZ6812 to PC Card. **CardBus Address/Data:** In CardBus mode, this pin is the CAD bit 11.	92	G12	TTL	I/O	Socket _Vcc	CardBus spec.
WE#/ CGNT#	**Write Enable**: This output goes active (low) to indicate a memory write from the OZ6812 to the PC Card socket. **CardBus Grant:** In CardBus mode, this pin is the CGNT# signal.	106	B13	TTL	TO	Socket _Vcc	CardBus spec.

Pin Name	Description	Pin Number		Input	Type	Power Rail	Drive
		LQFP	**BGA**				
IORD#/ CAD13	**I/O Read**: This output goes active (low) for I/O reads from the OZ6812 to the socket. **CardBus Address/Data:** In CardBus mode, this pin is the CAD bit 13.	93	G10	TTL	I/O	Socket _Vcc	CardBus spec.
IOW#/ CAD15	**I/O Write**: This output goes active (low) for I/O writes from the OZ6812 to the socket. **CardBus Address/Data:** In CardBus mode, this pin is the CAD bit 15.	96	F11	TTL	I/O	Socket _Vcc	CardBus spec.
WP/ IOIS16#/ CCLKRUN#	**Write Protect / I/O is 16-Bit:** In Memory mode, this input is indicates the status of the write protect switch on the PC Card. In I/O mode, this input indicates the size of current data transfer on the PC Card. **CardBus Clock Run:** In CardBus mode, this pin is the CCLKRUN# signal, which starts and stops the CardBus CCLK. To enable the CLKRUN# signal, ExCA register 3Bh bit[3:2] must be enabled.	136	A4	TTL	I/O-PU	Socket _Vcc	CardBus spec.
INPACK#/ CREQ#	**Input Acknowledge:** The INPACK# function is not applicable in PCI bus environments. This pin is provided for Legacy card compatibility. **CardBus Request:** In CardBus mode, this pin is the CREQ# signal.	123	C8	-	I-PU	Socket _Vcc	CardBus spec.
RDY/IREQ#/ CINT#	**Ready / Interrupt Request:** In Memory mode, this input indicates that the card is ready or busy. In I/O mode, this input indicates a card interrupt request. **CardBus Interrupt:** In CardBus mode, this pin is the CINT# signal. This signal is active-low and level-sensitive.	132	C6	-	I-PU	Socket _Vcc	CardBus spec.
WAIT#/ CSERR#	**Wait:** This pin is driven by the PC Card to delay completion of the current cycle. **CardBus System Error:** In CardBus mode, this pin is the CSERR# signal.	133	A5	TTL	I-PU	Socket _Vcc	CardBus spec.
CD[2:1]/ CCD[2:1]#	**Card Detect**: These inputs indicate a card is present in the socket. They are internally pulled high to AUX_VCC. **CardBus Card Detect:** In CardBus mode, these inputs are used with CVS[2:1] to detect presence and type of card.	137, 75	C5, K10	TTL	I-PU-Schmitt	Aux_Vcc	CardBus spec.
CE2#/ CAD10	**Card Enable 2:** This pin is driven low to control byte/word card access. CE2# enables odd-numbered address bytes. **CardBus Address/Data:** In CardBus mode, this pin is the CAD bit 10.	91	G13	TTL	I/O	Socket _Vcc	CardBus spec.
CE1#/ CCBE0#	**Card Enable 1:** This pin is driven low to control byte/word card access. CE1# enables even-numbered address bytes. When configured for 8-bit cards, CE1# is active and A0 is used to indicate access of odd- or even-numbered bytes. **CardBus Command/Byte Enable:** In CardBus mode, this pin is the CCBEO# signal.	88	H13	TTL	I/O	Socket _Vcc	CardBus spec.

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| Pin Name	Description	Pin Number		Input	Type	Power Rail	Drive
		LQFP	BGA				
RESET/ CRST#	**Reset:** This active high output resets the card. To prevent reset glitches, this signal is high-impedance unless a card is seated in the socket, card power is applied, and the card's interface signals are enabled. **CardBus Reset:** In CardBus mode, this pin is the CRST# output.	119	C9	TTL	TO	Socket _Vcc	CardBus spec.
BVD2/SPKR#/ LED / CAUDIO	**Battery Voltage Detect 2 / Speaker / LED:** In Memory mode, this input serves as the BVD2 (battery warning status) input. In I/O mode, this input can be configured as the card's SPKR# audio input or drive-active LED input. **CardBus Audio:** In CardBus mode, this pin is the CAUDIO input.	134	D6	-	I-PU	Socket _Vcc	-
BVD1/ STSCHG#/RI#/ CSTSCHG	**Battery Voltage Detect 1 / Status Change / Ring Indicate:** In Memory mode, this is the BVD1 (battery-dead status) input. In I/O mode, this is the STSCHG# input indicating that the card's internal status has changed, or the ring indicates input for wakeup-on-ring system power management support. See bit 7 of the Interrupt and General Control register (03h). **CardBus Status Change:** In CardBus mode, this pin is the CSTSCHG. This pin can be used to generate PME#.	135	B5	-	I-PU	Socket _Vcc	-
VS[2:1]/ CVS[2:1]	**Voltage Sense:** These pins are used in conjunction with CD[2:1] to determine the type and voltage of a card. These pins are internally pulled high to AUX_VCC. See Table 1. **CardBus Voltage Sense:** In CardBus mode, these pins are the CVS[2:1] pins.	117, 131	D9, B6	TTL	I/O-PU	Aux_Vcc	CardBus spec.
SOCKET_VCC	**Socket Power:** These pins are the power rail input for the socket interface control logic. These pins can be 0, 3.3, or 5 V,. The socket interface outputs will operate at the voltage applied to these pins.	90, 126	G11, C7	-	PWR	-	-

OZ6812

Power, Ground, and Reserved Pins

Pin Name	Description	Pin Number		Input	Type	Power Rail	Drive
		LQFP	BGA				
Aux_VCC	**Auxiliary VCC**: This pin is connected to the system's 3.3/5V power supply. For the device to 5V tolerant, connect to +5V power.	63	M9	-	PWR	-	-
CORE_VCC	**CORE_VCC:** This pin provides power to the core circuitry of the OZ6812. It must be connected to a 3.3V power supply.	14, 66, 86, 102, 122, 138	F4, M10, H10, D12, D8, B4	-	PWR	-	-
PCI_VCC	**PCI Bus VCC:** These pins can be connected to either a 3.3V or5V power supply. The PCI bus interface will operate at the voltage applied to these pins, independent of the voltage applied to other OZ6812 pin groups.	18, 30, 44, 50	G3, K2, M4, K6	-	PWR	-	-
GND	**System Ground**	6, 22, 42, 58, 78, 94, 114, 130	D3, H1, L4, N8, K11, F13, C10, A6	-	GND	-	-

Legend

| I/O Type	Description
I	Input Pin
I-PU	Input pin with internal pull-up
I-PU Schmitt	Input pin with internal pull-up and Schmitt trigger
O	Output
OD	Open-drain
TO	Tri-state output
TO-PU	Tri-state output with internal pull-up
OD-PU	Open-drain output with internal pull-up
PWR	Power pin

| Power Rail	Source of Output's Power
1	AUX_VCC: outputs powered from AUX_VCC
2	SOCKET_VCC: outputs powered from the socket
3	PCI_VCC: outputs powered from PCI bus power supply
4	CORE_VCC: outputs powered from the CORE_VCC

OZ6812

Package Information - 144 Pin LQFP
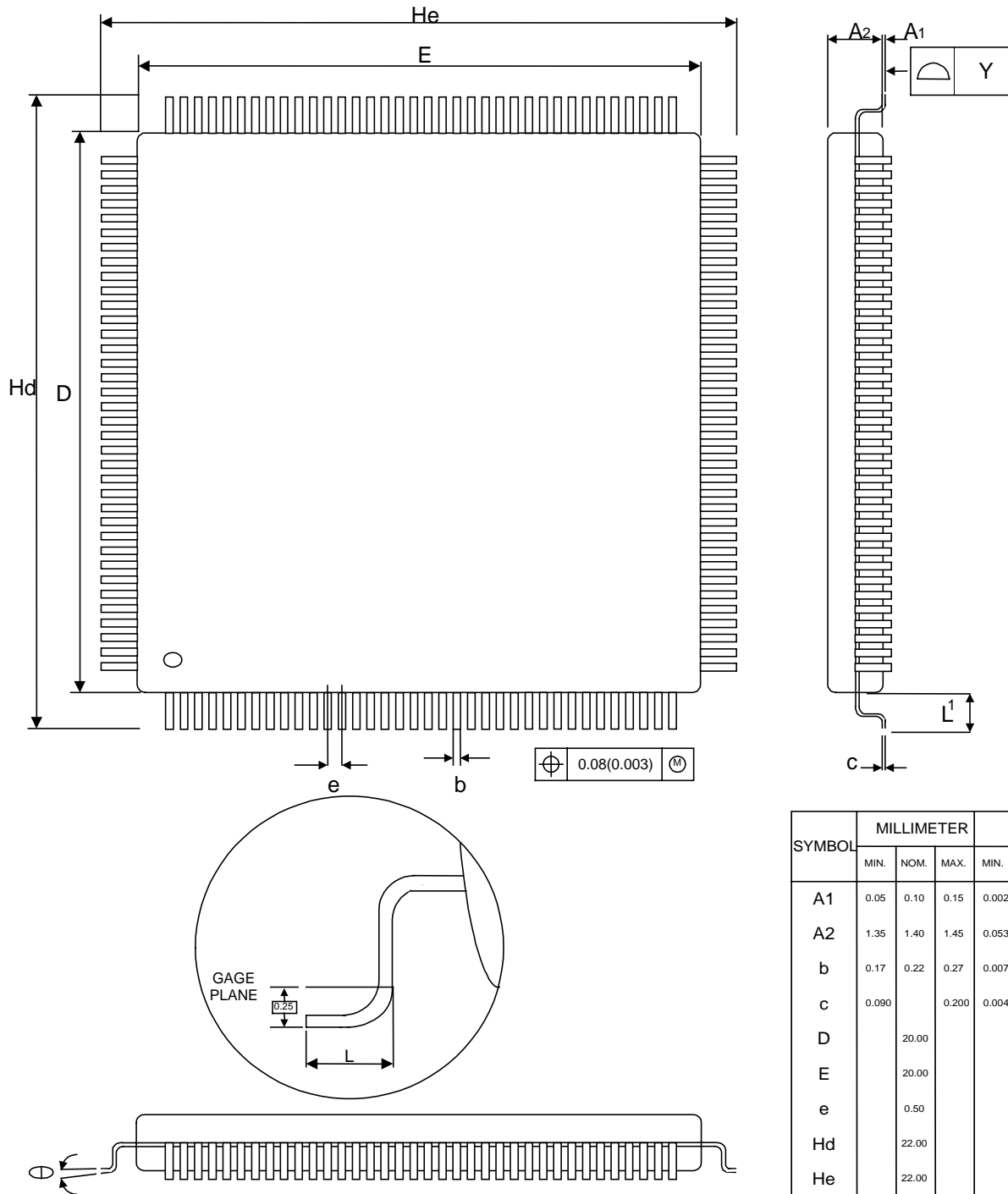
SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.090		0.200	0.004		0.008
D		20.00			0.787	
E		20.00			0.787	
e		0.50			0.020	
Hd		22.00			0.866	
He		22.00			0.866	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
Y			0.08			0.003
θ	0		7	0		7

144 Pin Mini - BGA

TOP VIEW
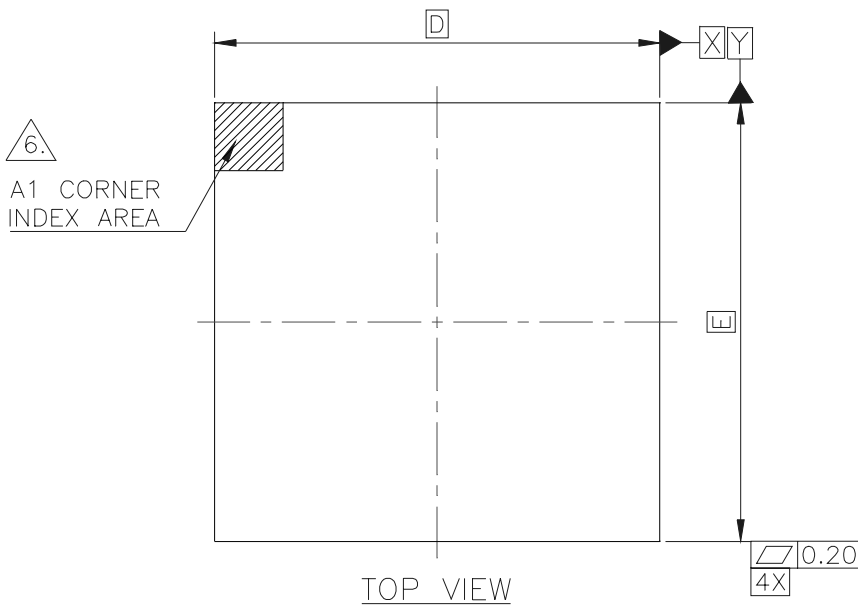
PACKAGE SPECIFICATION			
SYMBOL	MIN	NOM	MAX
D	12.80	13.00	13.20
E	12.80	13.00	13.20
D1		9.60	
E1		9.60	
e		0.80	
A	1.24	1.34	1.44
A1	0.33	0.38	0.43
A2	0.55	0.60	0.65
c	0.32	0.36	0.40
b	0.43	0.48	0.53
G		1.70	
G1		1.70	
aaa		0.12	
bbb		0.10	
ccc		0.10	
M1		13	
M2		13	
N		169	

BOTTOM VIEW
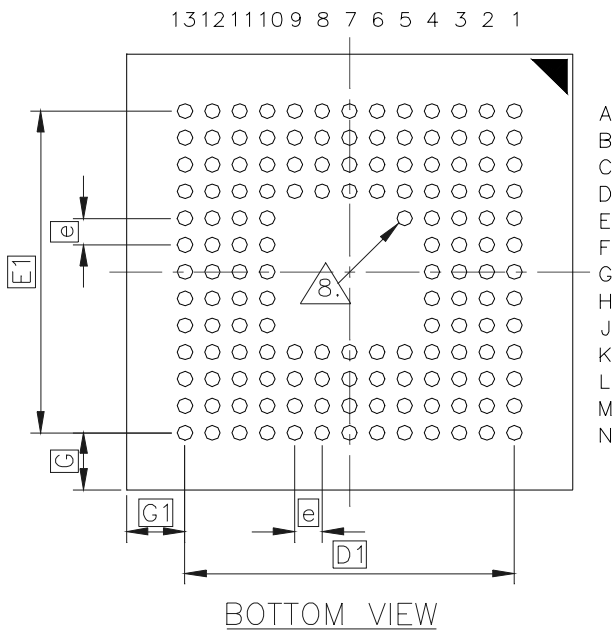
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
3. "N" REPRESENTS THE MAXIMUM NUMBER OF SOLDER BALLS FOR MATRIX SIZE M1 AND M2.
4. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER AFTER REFLOW AND PARALLEL TO PRIMARY DATUM Z, THE ORIGINAL SOLDER BALL DIAMETER IS 0.45 mm.
5. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. A1 CORNER MUST BE IDENTIFIED BY INK MARK, METALLIZED MARKINGS, IDENTATION OR OTHER FEATURE OF PACKAGE BODY, LID OR INTEGRAL HEATSLUG, ON THE TOP SURFACE OF THE PACKAGE.
7. SOLDER BALL DEPOPULATION IS ALLOWED. DEPOPULATION IS THE OMISSION OF BALLS FROM A FULL MATRIX (M1 OR M2).
8. BALL PAD A1 CORNER INDICATOR (NC) SOLDER BALL

SIDE VIEW