High-High Accuracy Battery (Gas) Gauge for High Power Batteries

FEATURES

- Integrated 8-bit microcontroller with high performance and low power consumption
- Integrated, highly accurate ADC works with a variety of BMU ICs, including::
  - OZ890 +OZ9313: 5~13 Cells
  - OZ8920+OZ9313: 5~ 8 Cells
  - OZ8930+OZ9313: 3~ 6 Cells
  - OZ8940+OZ9313: 6~12 Cells
  - Supported Stacked Protection ICs + OZ9313
- Smart Battery Specification (SBS) v 1.1 compatible
- Compliant with JEITA safety guidelines
- Measures charge/discharge current with a dedicated 16-bit ADC:
  - 0.27 nVhr resolution
  - Automatic On-line Calibration to improve accuracy
- Monitors individual cell voltages, terminal voltage and external temperature from BMU (Battery Management Unit) chips
- Integrated internal temperature sensor
- Programmed to scan BMU protections that include:
  - Over voltage Protection
  - Under voltage Protection
  - Over current Protection
  - Short circuit Protection
  - Over temperature Protection
  - Under temperature Protection
- Embedded 64 k bytes flash and 1 k bytes SRAM to support variety of battery characteristics in high power application
- Integrated 8-bit PWM with 2 bit pre-scaler and multi-GPIOs (GPIO0~GPIO9) and 2 GPO (GPIO10, GPIO11)
- Integrated 1.8V voltage regulator (LDO18)
- Power Modes: Full and Sleep
- Low sleep mode current: less than 10 µA (typ.)
- TSSOP30 Package with 0.50 mm pitch

APPLICATIONS

- Electric Bicycles
- Electric Motorcycles
- Power Tools
- Backup Battery Packs

GENERAL DESCRIPTION

OZ9313 is a highly accurate battery (gas) gauge designed to work with high power Battery Management Units (BMUs), specifically O2Micro's industry leading OZ890, OZ8920, OZ8930 and OZ8940.

OZ9313 directly measures charge current and discharge current with an integrated high-accuracy and low-power sigma-delta ADC. Furthermore, OZ9313 is programmed to constantly scan individual cell voltages, the terminal voltage of the battery pack and external temperature in order to continually update SOC (State of Charge) and SOH (State of Health) of a high power battery pack.

With O2Micro's innovative Battery Gauge Software (BGS) firmware, OZ9313 automatically self-calibrates without waiting to complete a charge/discharge cycle. Moreover, this automatic calibration successfully increases the reliability and accuracy of a variety of high power battery packs.

For safety reasons, BMUs invoke their own hardware based protection mechanisms and prohibit OZ9313 from triggering protection except what is specifically related to the gas gauge function. This is illustrated in the table shown below:

BMU chip	Trigger protection	Release protection	Gas Gauge Trigger/Release protection
OZ890	OZ890	***OZ9313***	***OZ9313***
OZ8920	OZ8920	OZ8920	***OZ9313***
OZ8930	OZ8930	OZ8930	***OZ9313***
OZ8940	OZ8940	OZ8940	***OZ9313***

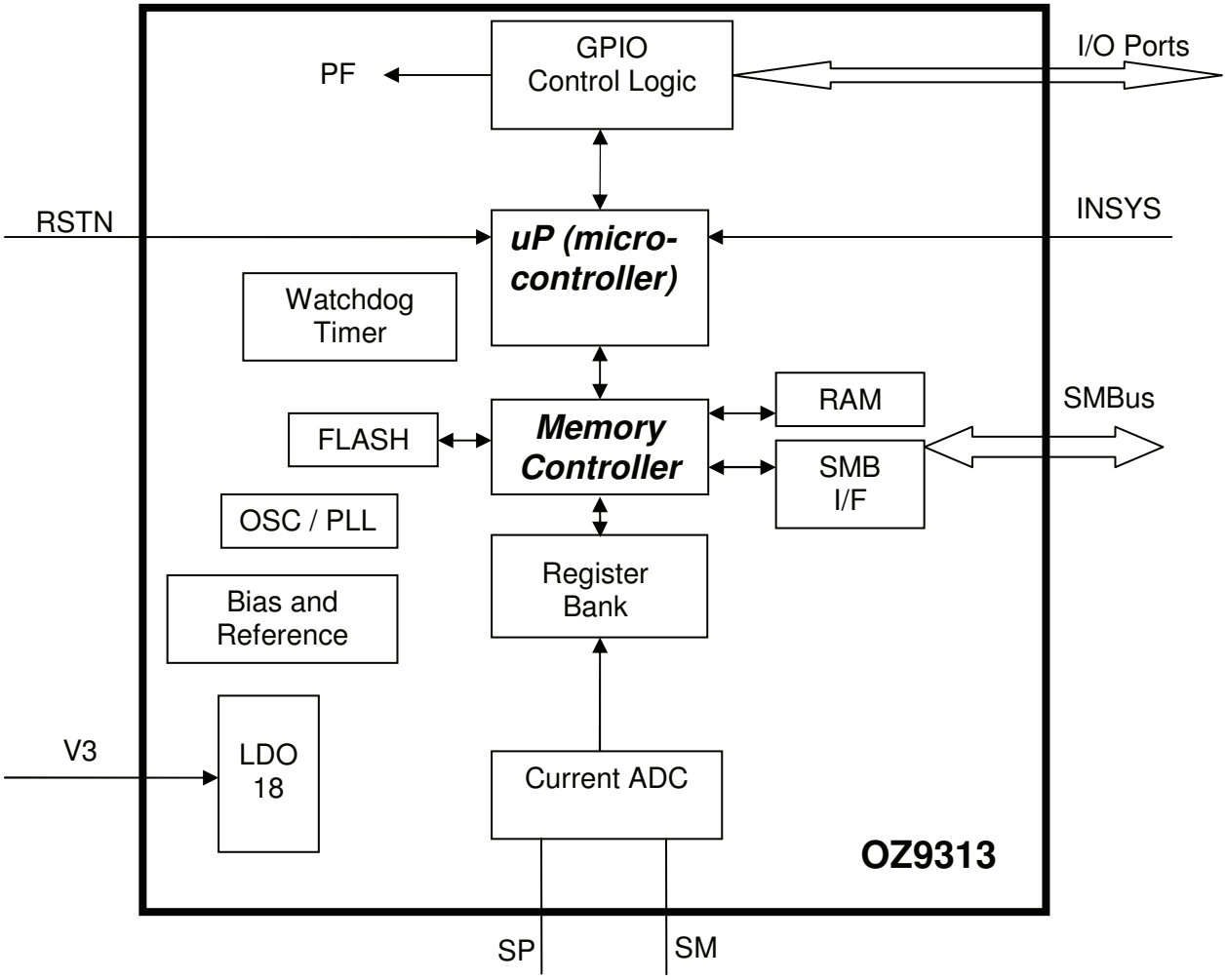
OZ9313 monitors cell voltage and sends cell balancing commands to the BMU. Cell balancing increases the overall life of a battery pack.

OZ9313 is compliant with SBS Data Specification v1.1 (See section on *SBS v1.1 Functions* for detailed information) and can be easily modified to support additional, optional manufacturer functions, protocol extensions, and gauge functionality.

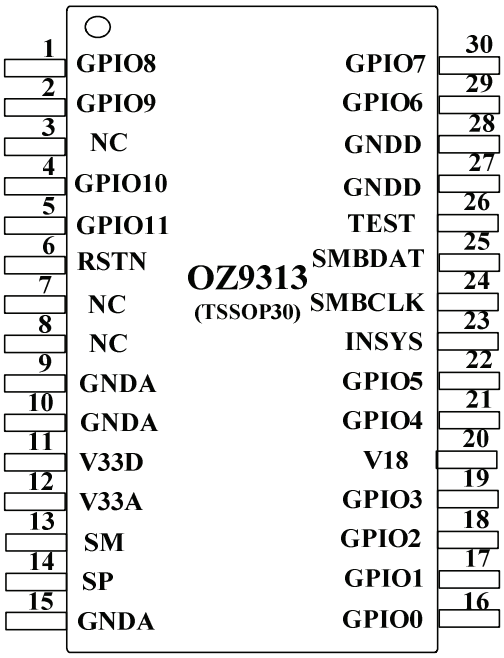
ORDERING INFORMATION

Part Number	Temp Range	Package
OZ9313RN	-40°C to 85°C	TSSOP30

BLOCK DIAGRAM



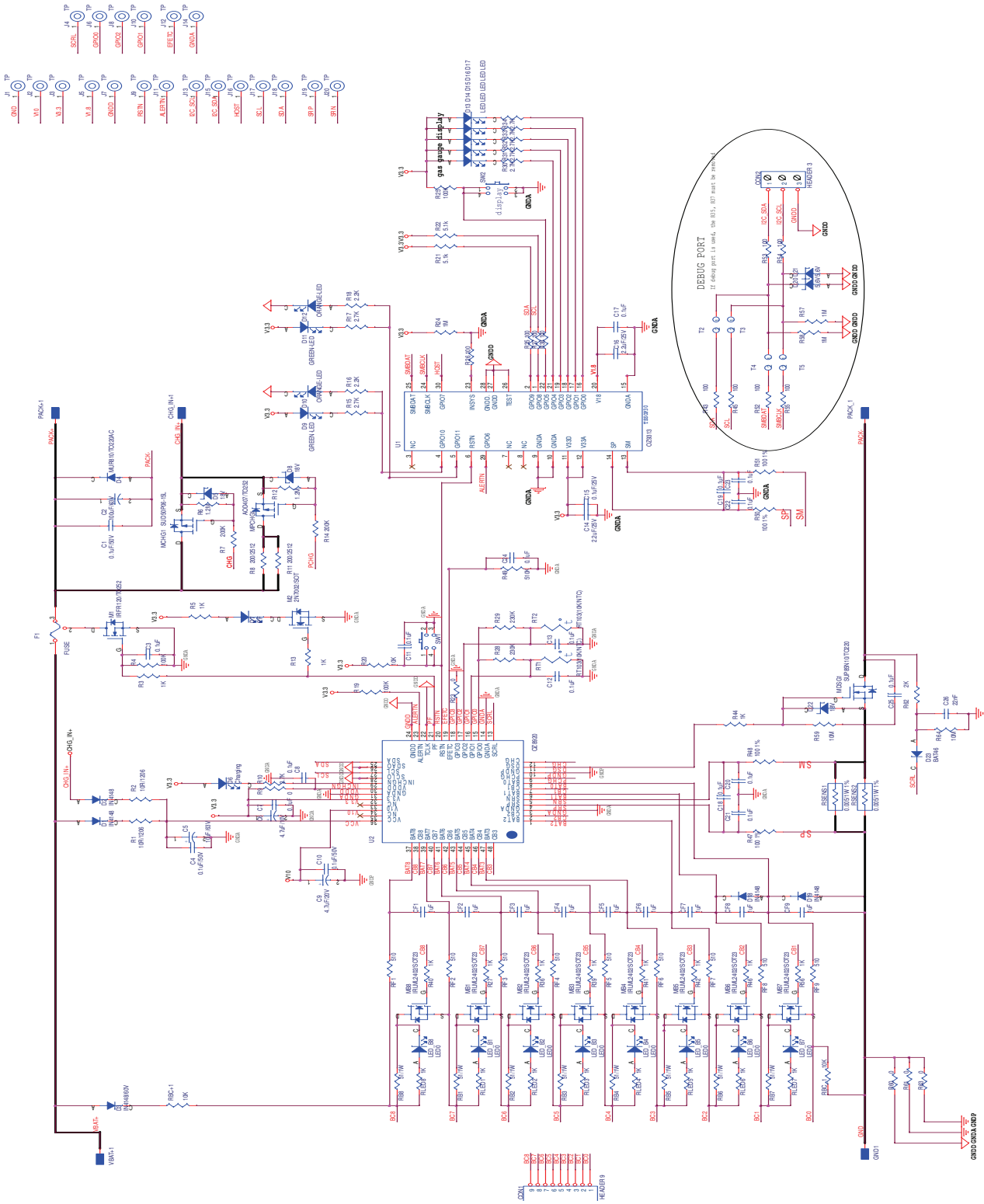
PIN DIAGRAM



PIN DESCRIPTION

Name	Pin #	I/O	Description
GPIO8	1	IO	General purpose input/output.
GPIO9	2	IO	General purpose input/output.
NC	3	-	No Connect (not electrically connected)
GPIO10	4	O	General purpose output
GPIO11	5	O	General purpose output
RSTN	6	IO	Reset input/output. Active low. (connect with BMU)
NC	7	-	No Connect (not electrically connected)
NC	8	-	No Connect (not electrically connected)
GNDA	9	GND	Analog ground
GNDA	10	GND	Analog ground
V33D	11	Power	Digital 3.3V power supply. (connect with BMU)
V33A	12	Power	Analog 3.3V power supply. (connect with BMU)
SM	13	I	External small sense resistor negative terminal.
SP	14	I	External small sense resistor positive terminal.
GNDA	15	GND	Analog ground.
GPIO0	16	IO	General purpose input/output
GPIO1	17	IO	General purpose input/output
GPIO2	18	IO	General purpose input/output
GPIO3	19	IO	General purpose input/output.
V18	20	Power	Internal generated 1.8V for digital core. Add 2.2~4.7 µF external capacitor
GPIO4	21	IO	General purpose input/output.
GPIO5	22	IO	General purpose input/output
INSYS	23	I	System insertion detect pin.
SMBCLK	24	I	SMBus clock
SMBDAT	25	IO	SMBus data
TEST	26	TEST	Chip test pin (Open, or tie to GNDD in application)
GNDD	27	GND	Digital ground
GNDD	28	GND	Digital ground
GPIO6	29	IO	General purpose input/output.
GPIO7	30	IO	General purpose input/output.

Application Schematic (e.g. OZ8920+OZ9313)



DC CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Operating at ambient temperature (T_A) = 25°C, unless otherwise noted(1)

Parameter	*Pin*	*Min*	*Max*	*UNIT*
Supply voltage range	V33D,V33A	-0.5	5.0	V
Input voltage range	SM, SP	-0.3	3.6	V
	All other input pins	-0.5	V33 + 0.3	V
Output voltage range	V18	-0.5	3.6	V
	All other output pins	-0.5	5.0	V
Operating free-air temperature range, T_A		-40	85	°C
Storage temperature range, T_{STG}		-55	150	°C
Lead temperature (soldering, 10 sec)			300	°C

***Note 1**: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are for stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute maximum rated conditions for extended time may affect device reliability.*

***Note 2**: All voltages are with respect to ground of this device.*

***Note 3**: Ground refers to common node of GNDA, GNDD.*

RECOMMENDED OPERATING RANGE

Operating at ambient temperature (T_A) = 25°C, unless otherwise noted

Parameter	*Pin*	*Min*	*Typ*	*Max*	*UNIT*
Power supply	V33D,V33A	3	3.3	3.6	V
Input voltage range	SM, SP	-0.3		0.5	V
	V(SP,SM)	-0.25		0.25	V
	All other input pins	0		V33	V
Operating free-air temperature range, T_A		-40		85	°C
LDO capacitor	V18	2.2	4.7	10.0	µF

ELECTRICAL SPECIFICATIONS

Operating at ambient temperature (T_A) = 25℃, V33D=V33A=3.3V, unless otherwise noted

Power supply

Parameter	*Test Conditions*	*MIN*	*TYP*	*MAX*	*Unit*
Supply voltage	V33D,V33A	3.0	3.3	3.6	V
Supply current	Full power mode, ADC 4Hz, System Clock=2MHz		525	800	µA
	Sleep mode In system		15	30	µA
	Sleep mode (1)		10	20	µA
	Shut down mode		0		µA

Note 1: microcontroller, *Coulomb counter halted*

General purpose digital inputs and outputs

Parameter	*Test Conditions*	*MIN*	*TYP*	*MAX*	*Unit*
High-level input voltage		2			V
Low-level input voltage				0.8	V
Output voltage high	Iload = -0.5mA	V33D-0.7			V
Output voltage low	Iload = 0.5mA			0.4	V
Current drive capability	GP0 ~ GP3		4		mA
	GP4 ~ GP7		8		mA
	GP8 ~ GP9		8		mA

1.8V LDO

Parameter	*Test Conditions*	*MIN*	*TYP*	*MAX*	*Unit*
Output voltage	V33D=V33A=3.3V, Io<20mA	1.76	1.87	1.98	V
Line Regulation	I_O=1mA, 3.0V ≤ V33D=V33A ≤ 3.6V			5	mV
Load regulation	0.1mA ≤ I_O ≤ 20mA ; V33D=V33A=3.3V			30	mV

1.8V backup LDO(1)

Parameter	*Test Conditions*	*MIN*	*TYP*	*MAX*	*Unit*
Output voltage	V33D=V33A=3.3V; 1 µA ≤ I_O ≤ 100 µA; Chip enters sleep mode.	1.6	1.87	2.2	V

Note 1: *The 1.8V backup LDO is active only in sleep mode, to maintain circuit functionality.*

Current channel 16-bit sigma-delta ADC

Parameter	*Test Conditions*	*MIN*	*TYP*	*MAX*	*Unit*
LSB resolution	V33D=V33A=3V~3.6V Input full scale range Vin=-240mV~240mV		7.8		µV
Resolution			16		Bit
Conversion Time(1)			125		ms
Effective input resistance	Measure at Vsp-sm=100mV	3			MΩ

Note 1: *Single conversion*

Internal Oscillator

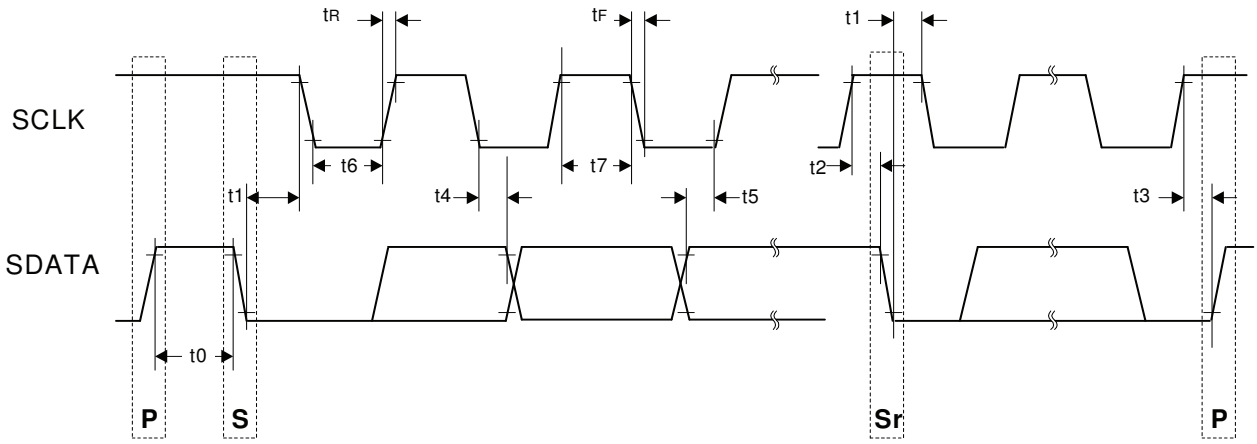
Parameter	*Test Conditions*	*MIN*	*TYP*	*MAX*	*Unit*
64 kHz Oscillator Frequency	TA=-40℃ ~85℃	62000	65536	68000	Hz
Start-up time(1)				200	µs
PLL output		1986	2048	2109	kHz
PLL start-up time(2)				7	ms

Note 1: *The start-up time is defined as the time it takes for the oscillator output frequency to be within 5% of the specified frequency.*

Note 2: *The PLL start-up time is defined as the time it takes for the PLL output frequency to be within 3% of the specified frequency.*

AC TIMING

SMBus Timing



Symbol	Parameter	Limits		Unit	Note
		Min	Max		
FSMB	SMBus Operating Frequency	10	100	kHz	
t0	Bus free time between Stop and Start condition	4.7	-	µs	
t1	Hold time after (Repeated) Start condition. After this period, the first clock is generated	4.0	-	µs	
t2	Repeated Start condition set up time	4.7	--	µs	
t3	Stop Condition setup time	4.0	-	µs	
t4	Data hold time	150	-	ns	
t5	Data setup time	250	-	ns	
TIMOUT		25	35	ms	See **Note 1**
t6	Clock low period	4.7	-	µs	
t7	Clock high period	4.0	50	µs	See **Note 2**
TLOW:SEXT	Cumulative clock low extend time (slave device)	-	25	ms	See **Note 3**
TLOW:MEXT	Cumulative clock low extend time (master dvice)	-	10	ms	See **Note 4**
tF	Clock/Data Fall time	-	300	ns	See **Note 5**
tR	Clock/Data Rise Time	-	1000	ns	See **Note 5**

Note 1: A device will timeout when any clock low exceeds this value

Note 2: t5 Max provides a simple guaranteed method for devices to detect bus idle conditions.

Note 3: TLOW:SEXT is the cumulative time a slave device is allowed to extend the clock cycles in one message from the initial start to stop. If a slave device exceeds this time, it is expected to release both its clock and data lines and reset itself.

Note 4: TLOW:MEXT is the cumulative time a master device is allowed to extend its clock cycles within one byte of a message as defined from start-to-ack, ack-to-ack, or ack-to-stop.

Note 5: Rise and Fall times are measured between 10% to 90% of the signal amplitude.

FUNCTIONAL DESCRIPTION

General Operation

OZ9313 constantly scans the state of charge (SOC) and state of health (SOH) of a battery pack by working with different types of BMU, and it includes the charge/discharge current, each individual cell voltage, and the temperature of high power battery pack. The Battery Gauge Software (BGS) combines this measured data with calculated corrections for self discharge, capacity loss, and other second order effects to compute the true capacity of the high power battery pack.

BMUs have their own hardware protection to protect the high power battery pack against over-charging, over-discharging, over-heating, under-temperature, over-voltage, under-voltage, and short-circuit by properly setting related parameters in EEPROM or OTP, e.g. voltage threshold, current threshold, temperature limit, and delay time.

In order to ensure safety of the pack, OZ9313 is prohibited from triggering hardware protections and OZ9313 only scans events once hardware protections are triggered by the BMU.

To support non-balanced or slightly off balanced cells in a high power battery pack, BMUs have integrated their own cell balancing circuits. Once BMU receives the balancing command from OZ9313, BMU immediately allows each cell to be balanced effectively during both the charging state and idle state.

Current Measurement

OZ9313 has a dedicated 16-bit sigma-delta current ADC for Coulomb counting measurements of the current across a sense resistor (1mΩ to 50mΩ), across pin 13(SM) and 14(SP), during charging and discharging of high power battery pack. The resolution of the coulomb counter is 0.27nVh with an input voltage range of –240mV to +240mV. The measurement period is programmable from 125ms to 64 seconds. The current ADC data will be stored in register 32h ~ 33h.

Computing Capacity

With coulomb counting, the amount of charge added to or removed from high power battery pack can be properly accounted for. However, calibration is necessary to continually re-adjust the battery gauge to the proper reference point. Calibration is performed automatically when necessary.

The self-discharge rate of a rechargeable battery depends on the capacity and temperature of the battery. This factor is taken into account when computing the overall capacity of the battery pack.

Gas Gauge Protection

Inside the high power battery pack, the OZ9313 is implemented with Battery Gauge Software (BGS) and embedded with 3 types of gas gauge protection: End of Discharge, End of Charge, and Lower Capacity.

Gas Gauge protection is only permitted to be triggered by BGS (Battery Gauge Software). Once the Gas Gauge Protection is triggered by the OZ9313 BGS, OZ9313 instantly sends a command to the BMU and then the BMU turns off the MOSFET to immediately cut off the charge or discharge loop.

I. End of Discharge

In order to implement End of Discharge protection, the BGS examines DsgCellLowMV, a voltage threshold parameter representing the cell voltage when the cell capacity is zero.

When the voltage of any cell drops below the DsgCellLowMV value, it means that the cell capacity is zero at that time. In this case, BGS sends a command to the BMU to turn off the DISCHARGE MOSFET to cut off the discharge loop. End of Discharge Protection is most like the under voltage protection of the BMU. Most Battery Management Systems (BMS) implement a combination of protection using the BGS for a tighter range with BMU acting as a hardware protection with a wider range.

II. End of Charge

The BGS uses ChargeEndMA and RstFCAlarmCellMV parameters to implement the End of Charge protection. ChargeEndMA is a current threshold and the RstFCAlarmCellMV is a voltage threshold. In charge status, when the charging current is less than CHrargeEndMA and the voltage of one of the cells is higher than RstFCAlarmCellMV at the same time, it means that the cell capacity is full. In this case, the BGS sends a command to the BMU to turn off the CHARGE MOSFET to cut off the charge loop. End of Charge protection is most like the over voltage protection of the BMU but with higher accuracy.

III. Low Capacity

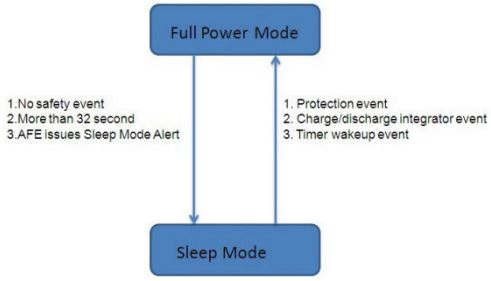
Through coulomb counting of BGS which is inside the OZ9313, the RSOC (Relative State of Charge) is highly accurate for capacity counting in high power battery pack. With the RSOC, the discharge loop must be cut off if the RSOC decreases to reach a value which presents lowest capacity of high power battery pack. To implement this protection of Low Capacity, BGS examines DsgMinRSOC which indicates the minimum RSOC during discharge. RSOC and DsgMinRSOC are both expressed as a percentage ratio. If the RSOC is lower than the DsgMInRSOC, the discharge loop must be cut off by turning off the DISCHARGE MOSFET. The BMU turns off the DISCHARGE MOSFET at the command of the BGS.

.Power Management [1]

At present, OZ9313 supports Full Power Mode and Sleep Mode for high power battery pack applications.

To save energy and reduce power consumption, OZ9313's modular and register programmable design provides flexible power management. The Coulomb Counting ADC's conversion rate can be programmed from 125ms to 64 seconds. The slower the rate, the more power will be saved. When the battery is being charged or discharged, the ADC conversion rate should be fast to get more accurate capacity information. When battery is idle or out of the system, the ADC conversion rate can be set slower.

Power mode transition



Note 2: For more power mode implementation detail, Please see Software Mode Gas Gauge Solution Specification.

SMBus Communication

OZ9313 has an SBS v1.1 compatible SMBus port to communicate with the SMBus host and charger. In this way, a system can efficiently monitor and manage the battery. The SMBus interface is a command-based protocol. A processor acting as the bus master initiates a communication to OZ9313 by generating a start condition. A start condition consists of a high-to-low transition of the SDA line while the SCL is high.

The processor completes the access with a stop condition. A stop condition consists of a low-to-high transition of the SDA line while the SCL is high. With SMBus, the most-significant bit (MSB) of a data byte is transmitted first. In some instances, OZ9313 acts as the bus master. This occurs when OZ9313 broadcasts charging requirements and alarm conditions to device addresses 0x12 (SBS Smart Charger) and 0x10 (SBS Host Controller).

OZ9313 supports the following SMBus protocols:

- Read Word
- Write Word
- Block read

A processor acting as the bus master uses the three protocols to communicate with OZ9313. OZ9313 acting as the bus master only uses the write word protocol in application. The SDA and SCL pins are open drain and require external pull-up resistors. OZ9313 supports packet error checking (PEC) as a mechanism to confirm communication accuracy with another SMBus device. Packet error checking requires that both the transmitter and receiver calculate a packet error code (PEC) for each communication message. The device supplies the last byte in the communication message to append the PEC to the message. The receiver compares the transmitted PEC to its PEC results to determine if there is a communication error.

LED Display

OZ9313 has 10 GPIO pins (GP0 ~ GP9) and 2 GPO (GPIO10, GPIO11) that can be configured as LED drivers. Normally, 4 or 5 LEDs are used for battery pack capacity display, with each LED representing 25% or 20% capacity. The displayed remaining capacity can be relative or absolute based on customer's design requirements.

INTERNAL REGISTER INFORMATION

OZ9313 has two sets of internal registers:

- Internal Control Register ---- for I/O ports, coulomb counting, and flash memory control
- SBS v1.1 function register ---- for SBS v1.1 function support

CONTROL REGISTER MAP

OZ9313 has 128 addressable Control Registers. These registers control coulomb counting ADC, and SMBus communication, etc. OZ9313's internal microcontroller can directly access these Control Registers.

After reset, bits in Control Register are cleared to zeroes except as otherwise noted.

Control Register Address Range	Function Description
00h – 03h	Reserved
04h	Main Clock Control of CPU
05h	Sleep mode control
06h ~ 09h	Reserved
0Ah ~ 13h	SMbus control
14h ~ 19h	GPIO0 ~ GPIO9 control
1Ah ~ 24h	Watchdog and timer control
25h	GPIO10 ~ GPIO11 control
26h ~ 2Dh	Reserved
2Eh ~ 30h	Current ADC control
31h ~ 3Eh	Current detection and coulomb counting
3Fh ~ 50h	Reserved
51h ~59h	SMbus control
5Ah	Flash memory control
5Bh ~ 7Fh	Reserved

Note: *The registers in shadow are fully controlled by Battery Gauge Software (BGS), not accessible to the end user*

Detailed Internal Control Register information

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h ~ 03h	Reserved							

Register 00h ~ 03h : Reserved

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
04h	Reserved		Ultra_lowerpower_en		Main Clock control			
05h	Reserved						Sleep_enable	
06h ~ 09h	Reserved							

Register 04h

Bit7 – Bit6 : Reserved

Bit5 – Bit4 : Ultra lower power control of CPU
00, 01, 10: low power mode is disable
11: Enable CPU enter the low power mode

Bit3 – Bit0 : Main clock control
1000: 2MHz
1100: 1MHz
1110: 512KHz
1111: 256KHz

Register 05h

Bit7 – Bit2: Reserved

Bit1 – Bit1: Sleep enable control
00, 01, 10: disable
11: enable

Register 06h ~ 09h: Reserved

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Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Ah	SMbus int.	Time1 int.	Time2 int.	Scan_ADC int.	Reserved	Chgcc int.	Dischcc int.	Reserved
0Bh	GP7 int.	GP6 int.	GP5 int.	GP4 int.	Insys int.	Reserved		
0Ch	SMbus ie.	Time1 ie.	Time2 ie.	Scan_ADC ie.	Reserved	Chgcc ie.	Dischcc ie.	Reserved
0Dh	GP7 ie.	GP6 ie.	GP5 ie.	GP4 int.	Insys int.	Reserved	Insys isc.	
0Eh	GP7 isc.		GP6 isc.		GP5 isc		GP4 isc.	
0Fh	SMbus intpr.	Time1 intpr.	Time2 intpr.	Scan_ADC intpr.	Reserved	GP7 intpr.	GP6 intpr.	insys intpr.
10h ~ 13h	Reserved							

Register 0Ah

Bit7 : SMBus interrupt
Bit6 : Timer1 interrupt
Bit5 : Timer2 interrupt
Bit4 : ADC scan interrupt
Bit3 : Reserved
Bit2 : Charge coulomb counting overflow interrupt.
Bit1 : Discharge coulomb counting overflow interrupt.
Bit0 : Reserved

Register 0Bh

Bit7 : GPIO7 input interrupt if it is configured as digital input pin
Bit6 : GPIO6 input interrupt if it is configured as digital input pin
Bit5 : GPIO5 input interrupt if it is configured as digital input pin
Bit4 : GPIO4 input interrupt if it is configured as digital input pin
Bit3 : Insys input interrupt
Bit2 ~ Bit0 : Reserved

Register 0Ch

Bit7 : SMBus interrupt enable
Bit6 : Timer1 interrupt enable
Bit5 : Timer2 interrupt enable
Bit4 : ADC scan interrupt enable
Bit3 : Reserved
Bit2 : Charge coulomb counting overflow interrupt enable
Bit1 : Discharge coulomb counting overflow interrupt enable
Bit0 : Reserved

Register 0Dh
- Bit7 : GPIO7 input interrupt enable
- Bit6 : GPIO6 input interrupt enable
- Bit5 : GPIO5 input interrupt enable
- Bit4 : GPIO4 input interrupt enable
- Bit3 : Insys input interrupt enable
- Bit2 : Reserved
- Bit 1~ Bit0 : INSYS Pin Input Interrupt Sense Control
  - 00 : falling edge and low level
  - 01 : rising edge only
  - 10 : falling edge only
  - 11 : falling and rising edge.

Register 0Eh
- Bit7 ~ Bit6 : GPIO7 Interrupt Sense Control
  - 00: low level only;
  - 01: rising edge only;
  - 10: falling edge only;
  - 11: falling and rising edge.
- Bit5 ~ Bit4 : GPIO6 Interrupt Sense Control
  - 00: low level only;
  - 01: rising edge only;
  - 10: falling edge only;
  - 11: falling and rising edge.
- Bit3 ~ Bit2 : GPIO5 Interrupt Sense Control
  - 00: low level only;
  - 01: rising edge only;
  - 10: falling edge only;
  - 11: falling and rising edge.
- Bit1 ~ Bit0 : GPIO4 Interrupt Sense Control
  - 00: low level only;
  - 01: rising edge only;
  - 10: falling edge only;
  - 11: falling and rising edge.

Register 0Fh
- Bit7 : SMBus interrupt priority
- Bit6 : Timer1 interrupt priority
- Bit5 : Timer2 interrupt priority
- Bit4 : ADC scan interrupt priority
- Bit3 : Reserved
- Bit2 : GPIO7 interrupt priority
- Bit1 : GPIO6 interrupt priority
- Bit0 : Insys interrupt priority

Register 10h ~ 13h : Reserved

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Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
14h	GP3 mode		GP2 mode		GP1 mode		GP0 mode	
15h	GP9 ctrl.	GP8 ctrl.	GP7 ctrl.	GP6 ctrl.	GP5 ctrl.	GP4 ctrl.	Reserved	
16h	GP7 dout.	GP6 dout.	GP5 dout.	GP4 dout.	GP3 dout.	GP2 dout.	GP1 dout.	GP0 dout.
17h	GP9 dout	GP8 dout	PF en.	PF nen.	Reserved			
18h	GP7 din.	GP6 din.	GP5 din.	GP4 din.	GP3 din.	GP2 din.	GP1 din.	GP0 din.
19h	GP9 din.	GP8 din.	Insys in.	Reserved				

Register 14h

Bit7 ~ Bit6 : GPIO3 mode Control
00: digital input;
01: digital input;
10: digital output;
11: analog pin.

Bit5 ~ Bit4 : GPIO2 mode Control
00: digital input;
01: digital input;
10: digital output;
11: analog pin.

Bit3 ~ Bit2 : GPIO1 mode Control
00: digital input;
01: digital input;
10: digital output;
11: analog pin.

Bit1 ~ Bit0 : GPIO0 mode Control
00: digital input;
01: digital input;
10: digital output;
11: analog pin.

Register 15h

Bit7 : GPIO9 configuration
Bit6 : GPIO8 configuration
Bit5 : GPIO7 configuration
Bit4 : GPIO6 configuration
Bit3 : GPIO5 configuration
Bit2 : GPIO4 configuration
Bit1 ~ Bit0 : Reserved

Register 16h

Bit7 : GPIO7 output data
Bit6 : GPIO6 output data
Bit5 : GPIO5 output data
Bit4 : GPIO4 output data
Bit3 : GPIO3 output data
Bit2 : GPIO2 output data
Bit1 : GPIO1 output data
Bit0 : GPIO0 output data

Register 17h

Bit7 : GPIO9 output data
Bit6 : GPIO8 output data
Bit5 ~ Bit4 : PF enable control
Bit3 ~ Bit0 : Reserved

Register 18h
Bit7 : GPIO7 input data
Bit6 : GPIO6 input data
Bit5 : GPIO5 input data
Bit4 : GPIO4 input data
Bit3 : GPIO3 input data
Bit2 : GPIO2 input data
Bit1 : GPIO1 input data
Bit0 : GPIO0 input data

Register 19h
Bit7 : GPIO9 input data
Bit6 : GPIO8 input data
Bit5 : Insys input, sampled at every 125ms from INSYS pin
Bit4 ~ Bit0 : Reserved

****

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1Ah	Clear wdt.	Clear wdt. flag	Wdt. enable	Wdt. nenable	Reserved	Wrt. time		
1Bh	Timer1 enable	Timer1 nenable	Reserved			Timer1 prescale		
1Ch	Timer21 enable	Timer1 nenable	Reserved			Timer1 prescale		
1Dh	Timer1 High byte							
1Eh	Timer Low byte							
1Fh	Timer1 Counter High byte							
20h	Timer1 Counter Low byte							
21h	Timer1 High byte							
22h	Timer Low byte							
23h	Timer1 Counter High byte							
24h	Timer1 Counter Low byte							

Register 1Ah
Bit7 : Writing “1” to clear the watchdog by firmware. Read always as “0”.

Bit6 : Set by hardware once firmware clears the watchdog, cleared by firmware writing 1 to this bit.

Bit5 : Hardware watchdog enable.
0 : disable watchdog
1 : enable watchdog

Bit4 : Complementary Hardware Watchdog Enable
0 : enable watchdog
1 : disable watchdog

Bit3 : Reserved

Bit2 ~ Bit0 : watchdog time set
000 : 0.25s
001 : 0.5s
010 : 1s
011 : 2s
100 : 4s
101 : 8s
110 : 16s
111 : 32s

Register 1Bh

Bit7 : Timer1 enable.
1 : enable the timer1
0 : disable the timer1

Bit6 : Complementary Timer1 Enable
1 : disable the timer1
0 : enable the timer1

Bit5 ~ Bit3 : Reserved

Bit2 ~ Bit0 : Timer1 pre-scale
000 = 1:1
001 = 1:2
010 = 1:4
011 = 1:8
100 = 1:16
101 = 1:32
110 = 1:64
111 = 1:128

Register 1Ch

Bit7 : Timer2 enable.
1 : enable the timer1
0 : disable the timer1

Bit6 : Complementary Timer2 Enable
1 : disable the timer1
0 : enable the timer1

Bit5 ~ Bit3 : Reserved

Bit2 ~ Bit0 : Timer2 pre-scale
000 = 1:1
001 = 1:2
010 = 1:4
011 = 1:8
100 = 1:16
101 = 1:32
110 = 1:64
111 = 1:128

Register 1Dh : Timer1 High byte

Register 1Eh : Timer1 Low byte

Register 1Fh : Timer1 Counter High byte

Register 20h : Timer1 Counter Low byte

Register 21h : Timer2 High byte

Register 22h : Timer2 Low byte

Register 23h : Timer2 Counter High byte

Register 24h : Timer2 Counter Low byte

****

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
25h	Reserved				GPIO10 control		GPIO11 control	
26h~2Dh	Reserved							

Register 25h
Bit3 ~ Bit2 : 01, GPIO10 = ”0”
Bit3 ~ Bit2 : 10, GPIO10 = ”1”
Bit1 ~ Bit0 : 01, GPIO11 = ”0”
Bit1 ~ Bit0 : 01, GPIO11 = ”1”

****

Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2Eh	ADC scan rate			Do offset	Reserved			
2Fh	Reserved		Current ADC Scan en.		Reserved			
30h	Reserved				In chg.	In dsg.	Reserved	Current ADC rst.

Register 2Eh
Bit7 ~ Bit5: ADC scan rate
000: disable ADC scan;
111: Enable current channel ADC

Bit4 : “1”: request doing offset for Current ADC; this bit is set by firmware, cleared by hardware automatically when the offset ADC is finished. Don’t generate interrupt after offset ADC is finished.
Bit3 ~ Bit0 : Reserved

Register 2Fh
Bit7 ~ Bit6 : Reserved

Bit5 ~ Bit4 : Current ADC scan enable
00: Disable the current ADC, and, coulomb counting is also disabled.
01: Enable the current ADC channel with fixed 16bits resolution, and disable coulomb counting.
10: Enable the current ADC channel with fixed 16bits resolution, and disable coulomb counting.
11: Enable the current ADC channel with fixed 16bits resolution, and enable coulomb counting.

Bit3 ~ Bit0 : Reserved

Register 30h
Bit7 ~ Bit4 : Reserved

Bit3 : Active high (read only) indicates the battery is being charged when the charge current is more than the charge threshold defined in the register “0x38”.

Bit2 : Active high (read only) indicates the battery is being discharged when the discharge current is more than the charge threshold defined in the register “0x38”.

Bit1 ~ Bit0 : Reserved

****

Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
31h	Reserved							
32h	Current ADC high byte							
33h	Current ADC low byte							
34h	Reserved							
35h	Reserved							
36h	Board current offset high byte							
37h	Board current offset low byte							
38h	Charge threshold							
39h	Discharge threshold							
3Ah	Chgcch bit 15	Charger coulomb counter high byte						
3Bh	Charger coulomb counter low byte							
3Ch	Dsgcch bit 15	Discharger coulomb counter high byte						
3Dh	Discharger coulomb counter low byte							
3Eh	Self discharge current							

Register 31h : Reserved

Register 32h : Current ADC sample register, high byte bit15 ~ bit8

Register 33h : Current ADC sample register, low byte bit7 ~ bit0

Register 34h ~ 35h : Reserved

Register 36h : Board current offset, high byte bit15 ~ bit8

Register 37h : Board current offset, low byte bit7 ~ bit0

Register 38h : This register is used to decide if the system is in charge state or not. If the detected current is positive and small enough (smaller than this value), the coulomb counter will not add the small current. This byte is always positive without sign.

When voltage LSB=7.8125μv,
If sense resistor = 20mΩ, current LSB is 0.390625mA, so the charge threshold range is 0.39~99.6mA;
If sense resistor = 10mΩ, current LSB is 0.78125mA, so the charge threshold range is 0.78~199.2mA.

Register 39h : This register is used to decide if the system is in charge state or not. If the detected current is positive and small enough (smaller than this value), the coulomb counter will not add the small current. This byte is always negative without sign.

When voltage LSB=7.8125μv,
If sense resistor = 20mΩ, current LSB is 0.390625mA, so the charge threshold range is 0.39~99.6mA;
If sense resistor = 10mΩ, current LSB is 0.78125mA, so the charge threshold range is 0.78~199.2mA.

Register 3Ah: Charge coulomb counter
Bit7 : Always be read as “0”, indicates this counter is always positive..
Bit6 ~ Bit0: Charge coulomb counter high byte

Register 3Bh: Charge coulomb counter low byte

Register 3Ch : Discharge coulomb counter
Bit7 : Always be read as “0”, indicates this counter is always positive..
Bit6 ~ Bit0: Discharge coulomb counter high byte

Register 3Dh : Discharge coulomb counter low byte

Register 3Eh : Self discharge current. The discharge counter will always add this value.

This byte is always positive without sign, due to the self discharge current is very small, so this byte will be good defined, and will be added at a fixed period of 64s.

One LSB of the discharge coulomb counter is defined as 4.44 µVhr (if the sense resistor is 20 mΩ, that means 0.2222mAhr). If we use 13 bit counter to count the self discharge current, the LSB is:

LSB = (4.444 µVhr X 3600/64)/8192 = 0.03052 µV (that means LSB = 1.526 µA with Rsense=20 mΩ), so this register can express the current range of 1.526 µA ~ 390.625 µA.

****

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
51h	Reserved							
52h	Reserved							
53h	SMbus mode		SMbus nmode		SMbus bit rate			
54h	Ack enable	SMbus nack.	SMbus start	SMbus stop	General call	Write collision	SMbus busy	R/W flag
55h	Master lost	Nack sent	Nack received	Start detected	Restart detected	Stop detected	Timeout record	SMbus error flag
56h	Core slave address							General call en.
57h	SMbus received command							
58h	SMbus received data							
59h	SMbus transmit data							

OZ9313 also can act as SMBus master to send critical information to Smart Battery charger or other SMBus device. Please refer to “Smart Battery Data Specification, Revision 1.1” section 6.1, section 6.2, section 6.3 for detailed protocol information.

Register 51h ~ 52h : Reserved

Register 53h

Bit7 ~ Bit6 : SMBus Mode Selection: This is one of the most critical registers. An EMC reset will be generated if there is a mismatch with its complementary bit5~bit4 when the EMC reset function is enabled.

00: Slave mode;
01: Master Receive mode;
10: Master Transmit mode with Arbitration: Hardware goes to Slave Receive mode “00” if arbitration is lost. Stays in this mode after the byte is transmitted;
11: Master Transmit Mode without Arbitration: Stays in this mode after the byte has been transmitted.

Bit5 ~ Bit4 : Complementary SMBus Mode Selection: This is one of the most critical registers. An EMC reset will be generated if there is a mismatch with its complementary bit7~bit6 when the EMC reset function is enabled.

11: Slave mode;
10: Master Receive mode;
01: Master Transmit mode with Arbitration: Hardware goes to Slave Receive mode “00” if arbitration is lost. Stays in this mode after the byte is transmitted;
00: Master Transmit Mode without Arbitration: Stays in this mode after the byte has been transmitted.

Bit3 ~ Bit0 : Bit Rate Setting in Master mode:
This register selects a division factor for the bit rate generator, which generates the SMBCLK clock frequency in the master mode. SMBCLK = clk1MHz / (2X(N+1))

Register 54h

Bit7 : Acknowledge Enable Bit:
This bit controls the generation of the acknowledge pulse. If this bit is written to 0, the device can be virtually disconnected from the SMBus.

Bit6 : NACK Send Request:
Set by firmware if need to force sending NACK to external host, and automatically cleared by hardware after sending NACK.

Bit5 : START Generation Bit:
This bit is written to 1 when OZ9313 wants to become a Master on the SMBus. The hardware checks if the bus is available, and generates a START on the bus if it is free. After START has been transmitted, this bit is automatically cleared by hardware, meanwhile it generates an interrupt.

Bit4 : STOP Generation Bit:
Written to 1 will generate a STOP on the bus in the master mode. After STOP has been transmitted, this bit is automatically cleared by hardware, but doesn't generate interrupt.

Bit3 : General Call Flag:
This bit is set when the general call address is matched, cleared by hardware when STOP is received.

Bit2 : Write Collision Flag:
This bit is set when trying to write the SMBus transmit data register when SMBINT is low, this flag is cleared by writing the SMBus data register when SMBINT is high.

Bit1 : Indicate the SMBus Status:
This bit is set after the START is detected and cleared after the STOP is detected or a NACK is received.
0: The SMBus is free;
1: The SMBus is busy.

Bit0 : Read or Write Flag:
In Slave mode, this flag indicates that the current operation is Slave Transmit or Slave Receive.
0: In Slave Receive Mode (write)
1: In Slave Transmit Mode (read)

Register 55h

Bit7 : Master Arbitration Lost:
Set when arbitration is lost while acting as a bus Master, and can only be cleared by FW writing "1" to this bit.

Bit6 : "1" indicates a NACK is sent on the bus during a receive operation, and cleared by FW writing one to this bit.

Bit5 : "1" indicates a NACK is received during a transmit operation, and cleared by FW writing one to this bit.

Bit4 : "1" indicates that a START condition has been detected on the SMBus, and cleared by FW writing one to this bit.

Bit3 : "1" indicates that a Repeated START condition has been detected on the SMBus, and cleared by FW writing one to this bit.

Bit2 : "1" indicates that a STOP condition has been detected on the SMBus, and cleared by FW writing one to this bit.

Bit1 : Timeout Condition Detected:
To indicate if one of the timeout conditions is detected. The timeout timers for TTimeout (25ms), TLow:sext (25ms), and TLow:mext (10ms), are based on the 64kHz Real Time Clock.
00: No timeout has occurred;
01: TLow:sext (25ms) condition detected in the Slave Mode;
10: TLow:mext (10ms) condition detected in the Master Mode;
11: TTimeout (25ms) condition detected in either Master or Slave Mode.
Timeout_record = 1 indicates one of the above three timeout occurs

Bit0 : Set by hardware when an abnormal NACK is received or time out occurs, or master lost, meanwhile an interrupt is generated to tell firmware what happen. Cleared by firmware writing one to this bit.

Register 56h
Bit7 ~ Bit1 : Slave Address.
The 7 bits are used to assign a slave address for this SMBus controller when in slave-read and slave-write mode, not needed in the Master mode. (the default address is 16h for SBS1.1 data)

Bit0 : General Call Recognition Enable Bit:
If set, this bit enables recognition of the general call address (0x00) in slave mode, if a match is found, an interrupt request is generated.

Register 57h : This 8-bit register (read only) is used to save the command code of the SMBus protocol.

Register 58h : (Read only) In receive mode (including write in slave, and read in master), the SMBDR contains the latest received data byte.

Register 59h : In transmit mode (including read in slave, and write in master), the SMBDR contains the data byte to be transmitted.

****

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
5Ah	Page erase enable			Page num erase				
5Bh ~ 7Fh	Reserved							

****

SBS v1.1 FUNCTIONS

OZ9313 fully supports "Smart Battery Data Specification, revision 1.1" (SBS v1.1). There are up to 64 functions defined by SBS v1.1, so there are 64 registers that correspond to 64 SBS v1.1 functions in OZ9313. Most of them are 16-bit (word) wide, only a few (SBS Function 20h ~ 23h) are strings. OZ9313's internal microcontroller can indirectly access SBS Function registers through Control Registers 53h ~ 59h. End user can directly access SBS v1.1 Functions through SMBus (Pin 28 SCL & Pin 29 SDA).

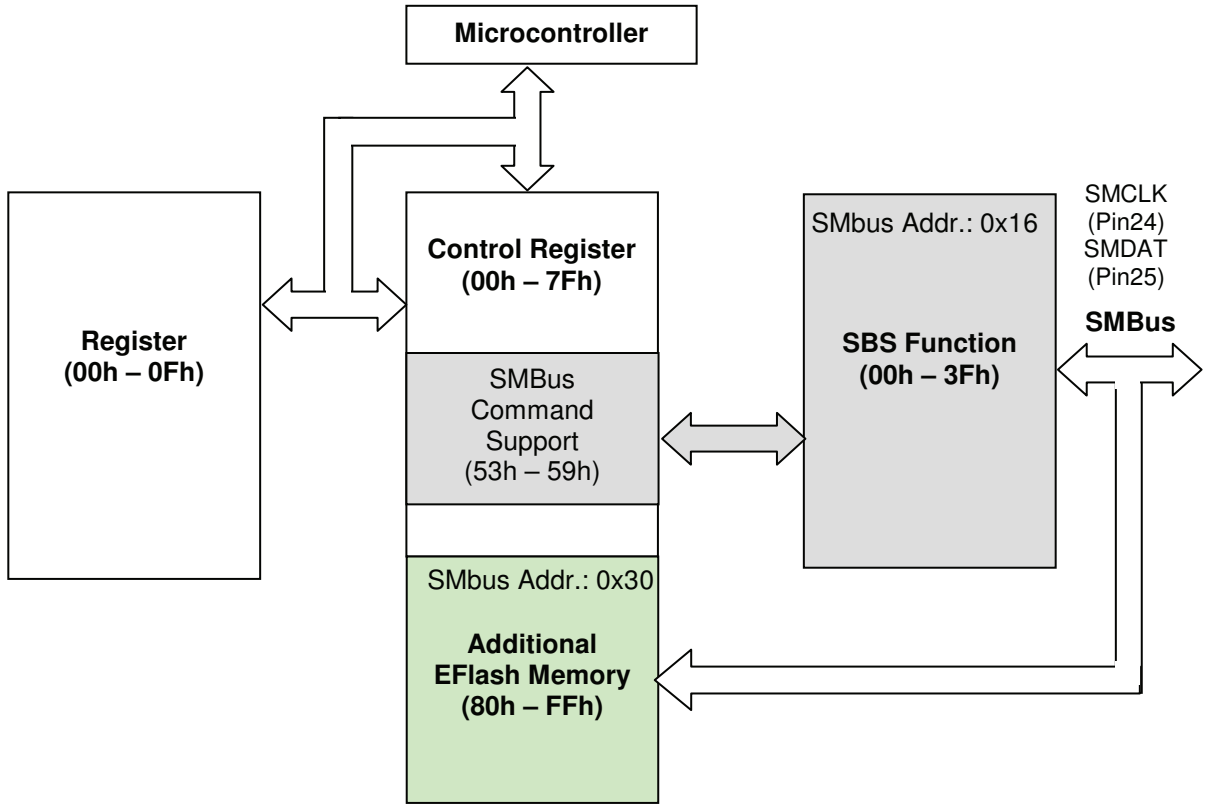
FUNCTION	Code	Access	Units
Manufacturer Access	0x00	r/w	word
RemainingCapacityAlarm	0x01	r/w	mAh or 10mWh
RemainingTimeAlarm	0x02	r/w	minutes
Battery Mode	0x03	r/w	bit flags
AtRate	0x04	r/w	mA or 10mW
AtRateTimeToFull	0x05	r/w	minutes
AtRateTimeToEmpty	0x06	r	minutes
AtRateOK	0x07	r	Boolean
Temperature	0x08	r	0.1°K
Voltage	0x09	r	mV
Current	0x0a	r	mA
AverageCurrent	0x0b	r	mA
MaxError	0x0c	r	percent
RelativeStateOfCharge	0x0d	r	percent
AbsoluteStateOfCharge	0x0e	r	percent
RemainingCapacity	0x0f	r	mAh or 10mWh
FullChargeCapacity	0x10	r	mAH or 10mWh
RunTimeToEmpty	0x11	r	minutes
AverageTimeToEmpty	0x12	r	minutes
AverageTimeToFull	0x13	r	minutes
ChargingCurrent	0x14	r	mA
ChargingVoltage	0x15	r	mV
BatteryStatus	0x16	r	bit flags
CycleCount	0x17	r	count
DesignCapacity	0x18	r	mAh or 10mWh
DesignVoltage	0x19	r	mV
SpecificationInfo	0x1a	r	unsigned int
ManufactureDate	0x1b	r	unsigned int
SerialNumber	0x1c	r	number
Reserved	0x1d – 0x1f	r	
ManufacturerName	0x20	r	string
DeviceName	0x21	r	string
DeviceChemistry	0x22	r	string
ManufacturerData	0x23	r	data
Reserved	0x24 – 0x3f		

INTERNAL REGISTER ACCESS METHODOLOGY

Among the four sets of registers, OZ9313's internal microcontroller can only directly access the Control Registers. However, OZ9313 provides a mechanism for microcontroller to indirectly acess the Protection Registers and SBS Function registers.

As seen in the following diagram, the microcontroller can access Protection Registers through Control Register 38h ~ 3Ah, and the microcontroller can access SBS Functions through Control Register 21h ~ 27h. The microcontroller can support SMBus command through Control Register 28h ~ 2Ch.

External SMBus host can directly access SBS Function Registers by SMBus.



APPLICATION

BMU + OZ9313 Gas Gauge with Table Lookup

BMU+OZ9313 is used to dynamically monitor battery status during charge and discharge and report the battery status through SBS registers. OZ9313 includes a high accuracy coulomb measurement circuit and firmware to monitor coulombs charged into the battery and discharged out of the battery. However, during charge and discharge, the error associated with coulomb counting will be accumulated. Near the end of discharge a lookup table method can compensate for the accumulated coulomb counting errors and thus improve the accuracy of the residual capacity reading.

End of Discharge Residual Capacity Table Lookup Method

When BMU+OZ9313 monitors discharging of the battery and the battery voltage is lower than the predefined threshold in Table (for different type of cells, the maximum voltage in table will be this threshold), BMU+OZ9313 will start using weighted lookup table values to calculate the residual capacity of the battery in addition to the coulomb counting value which is measured and calculated as a function of current and time. This table is created based on the supplied data from the cell manufacturer as well as cell testing conducted by O2Micro.

The lower the voltage, the residual capacity will be closer to the absolute zero point and BMU+OZ9313 will put more weight on using lookup table values rather than coulomb counting values.

The lookup table used by BMU+OZ9313 has three input axes: Temperature, Voltage and Current. To achieve the highest accuracy, different cell models may have different lookup tables. Our software will help customers generate the proper lookup table to use.

A sample portion of the lookup table is shown below. Please note that the input entries and the values in the table can be changed from time to time when more accurate data are available.

Table 1: Sample Residual Capacity Lookup Table

Voltage	**2700**	**2710**	**2725**	**2735**	**2805**	**2885**	**2915**	**2940**	**2965**	**2990**	**3010**	**3060**	**…**
	Temperature = -2.5ºC												
Current													
0.02C	104	105	105	112	116	128	134	139	144	150	1541	166	…
0.2C	458	459	462	464	483	509	521	533	545	553	545	500	…
0.35C	810	810	815	821	863	930	956	939	891	849	844	920	…
0.55C	1507	1520	1542	1551	1632	1650	1671	1682	1744	1749	1790	1959	…
0.8C	2473	2502	2545	2571	2798	3131	3184	3110	3039	3076	3205	3557	…
1.0C	3012	3056	3134	3185	3611	4079	4292	4483	4668	4848	4990	5227	…
1.2C	3581	3689	3786	3876	4506	5100	5290	5454	5611	5767	5892	6164	…
1.5C	5901	5978	6117	6186	6584	6961	7101	7214	7326	7440	7531	7739	…
Voltage	**2700**	**2710**	**2725**	**2735**	**2805**	**2885**	**2915**	**2940**	**2965**	**2990**	**3010**	**3060**	**…**
	Temperature = 5ºC												
Current													
0.02C	47	48	49	57	59	72	78	83	89	94	99	111	…
0.2C	239	241	244	245	256	272	279	286	293	300	304	309	…
0.35C	443	444	448	451	472	505	517	517	519	519	523	564	…
0.55C	827	834	843	849	900	963	964	974	976	995	1031	1141	…
0.8C	1424	1440	1463	1477	1604	1797	1821	1831	1841	1860	1939	2164	…
1.0C	1910	1938	1981	2010	2255	2491	2640	2774	2913	3055	3171	3400	…
1.2C	2324	2384	2445	2500	2910	3304	3440	3583	3732	3885	4011	4310	…
1.5C	3983	4051	4182	4249	4621	5058	5238	5389	5541	5702	5833	6151	…

We can think of residual capacity table lookup values as a function of Temperature, Current and Voltage noted as:

RC = f (*T, I, V*)

Where **RC** is Residual Capacity, ***T*** is Temperature, ***I*** is Current and ***V*** is Voltage.

We can define End of Discharge cutoff voltage at 3.0 V. When the battery is discharging, OZ9313 starts using weighted RC lookup table values when the voltage drops to below 3.5 V.

We will know how much capacity is left in the battery for discharging before shut off by using the following equation:

Useable Capacity = **f (*T*(now), *I*(now), *V*(now)) – f (*T*(now), *I*(now), *V*(3.0V))**

All these have been implemented in the OZ9313 firmware and users can directly read the reported data in SBS registers with confidence.

For more information, please see:

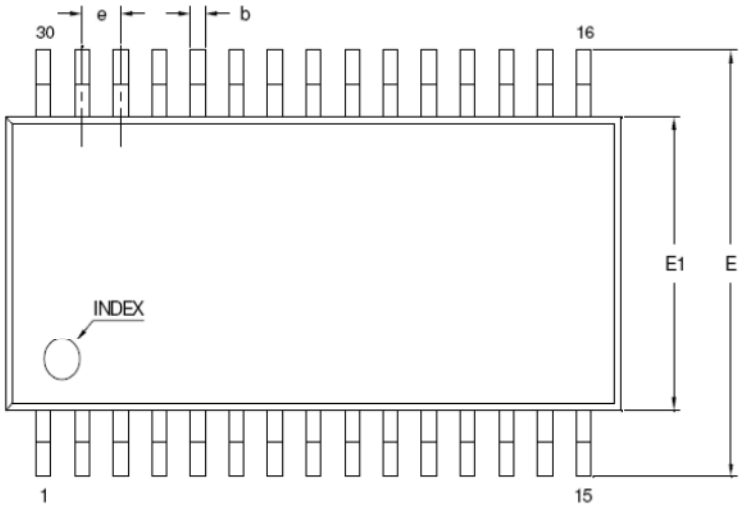
OZ9313 Application Note - 1, Lookup Table Based Gas Gauge Method

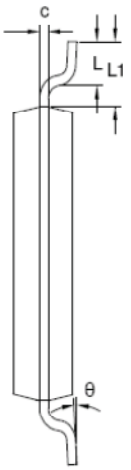
OZ9313 Application Note - 2, Lookup Table Format and Usage

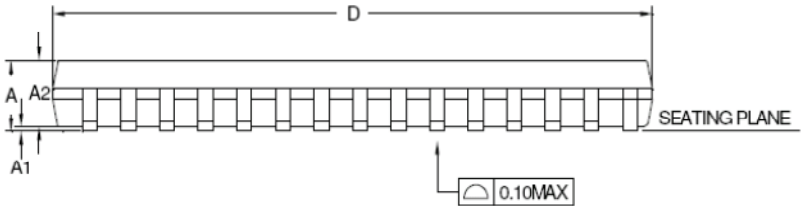
OZ9313 Application Note - 3, Battery Gauge End of Discharge Residual Capacity

PACKAGE INFORMATION– OZ9313RN

30L TSSOP 173mil Package Outline Drawing 0.5mm pitch







SYMBOL	DIMENSION (MM)		
	MIN	NOR	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
b	0.15	-	0.27
c	0.09	-	0.20
D	7.75	7.95	8.15
E	6.40 BSC		
E1	4.20	4.40	4.60
e	0.50 BSC		
L	0.30	0.60	0.75
L1	1.00 REF		
θ	0°	-	10°

NOTE:
1. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END. DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE

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