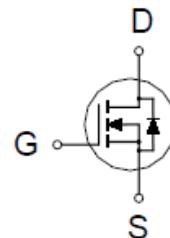


P0260ETF

N-Channel Enhancement Mode MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
600V	4.3Ω @ $V_{GS} = 10V$	2A



TO-220F

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Drain-Source Voltage	V_{DS}	600	V
Gate-Source Voltage	V_{GS}	±30	
Continuous Drain Current ²	I_D	2	A
		1.3	
Pulsed Drain Current ^{1,2}	I_{DM}	8	
Avalanche Current ³	I_{AS}	2	
Avalanche Energy ³	E_{AS}	20	mJ
Power Dissipation	P_D	29	W
		11	
Operating Junction & Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta JC}$	4.3	62.5	°C / W
Junction-to-Ambient	$R_{\theta JA}$			

¹Pulse width limited by maximum junction temperature.

²Limited only by maximum temperature allowed.

³ $V_{DD} = 50V$, $L = 10mH$, starting $T_J = 25^\circ C$

P0260ETF

N-Channel Enhancement Mode MOSFET

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$	600			V
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}, I_D = 250\mu\text{A}$	2	3	4	
Gate-Body Leakage	I_{GSS}	$V_{\text{DS}} = 0\text{V}, V_{\text{GS}} = \pm 30\text{V}$			± 100	nA
Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = 600\text{V}, V_{\text{GS}} = 0\text{V}, T_C = 25^\circ\text{C}$			1	μA
		$V_{\text{DS}} = 480\text{V}, V_{\text{GS}} = 0\text{V}, T_C = 100^\circ\text{C}$			10	
Drain-Source On-State Resistance ¹	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}} = 10\text{V}, I_D = 1\text{A}$		3.4	4.3	Ω
Forward Transconductance ¹	g_{fs}	$V_{\text{DS}} = 15\text{V}, I_D = 2\text{A}$		4		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 25\text{V}, f = 1\text{MHz}$		322		pF
Output Capacitance	C_{oss}			41		
Reverse Transfer Capacitance	C_{rss}			9		
Total Gate Charge ²	Q_g	$V_{\text{DD}} = 480\text{V}, V_{\text{GS}} = 10\text{V}, I_D = 2\text{A}$		10.7		nC
Gate-Source Charge ²	Q_{gs}			1.4		
Gate-Drain Charge ²	Q_{gd}			4.8		
Turn-On Delay Time ²	$t_{\text{d}(\text{on})}$	$V_{\text{GS}} = 10\text{V}, I_D = 2\text{A}, V_{\text{DD}} = 300\text{V}, R_G = 25\Omega$		30		nS
Rise Time ²	t_r			61		
Turn-Off Delay Time ²	$t_{\text{d}(\text{off})}$			59		
Fall Time ²	t_f			67		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_J = 25^\circ\text{C}$)						
Continuous Current ³	I_S				2	A
Forward Voltage ¹	V_{SD}	$I_F = 2\text{A}, V_{\text{GS}} = 0\text{V}$			1.5	V
Reverse Recovery Time	t_{rr}	$I_F = 2\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$		295		nS
Reverse Recovery Charge	Q_{rr}			1.2		uC

¹Pulse test : Pulse Width $\leq 300\ \mu\text{sec}$, Duty Cycle $\leq 2\%$.

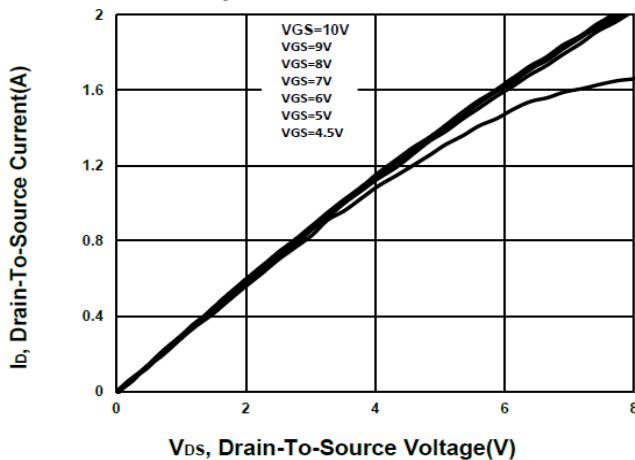
²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

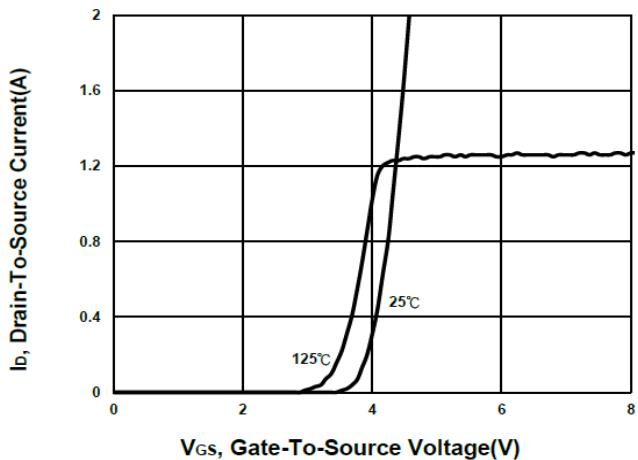
P0260ETF

N-Channel Enhancement Mode MOSFET

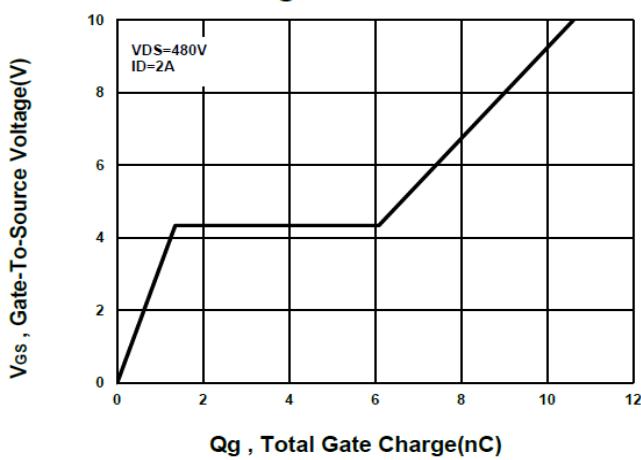
Output Characteristics



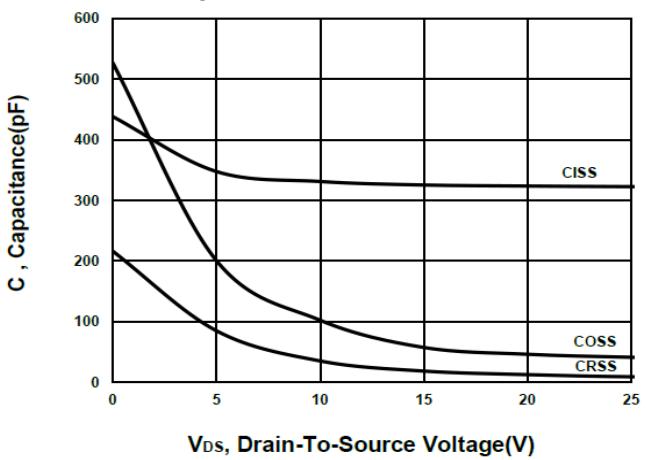
Transfer Characteristics



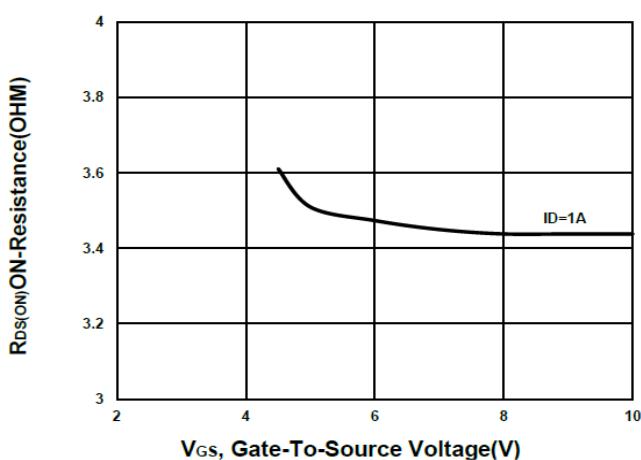
Gate charge Characteristics



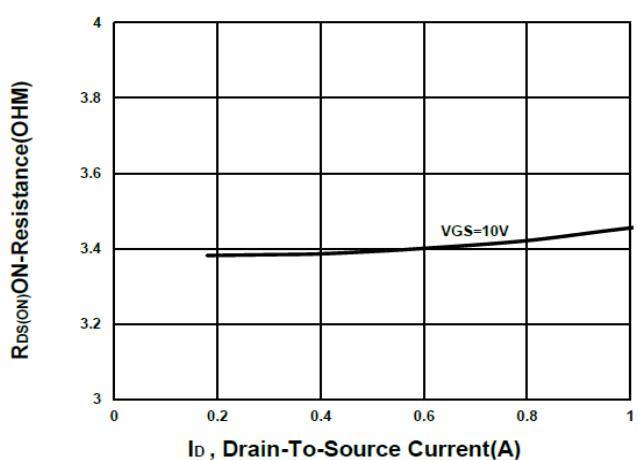
Capacitance Characteristic



On-Resistance VS Gate-To-Source

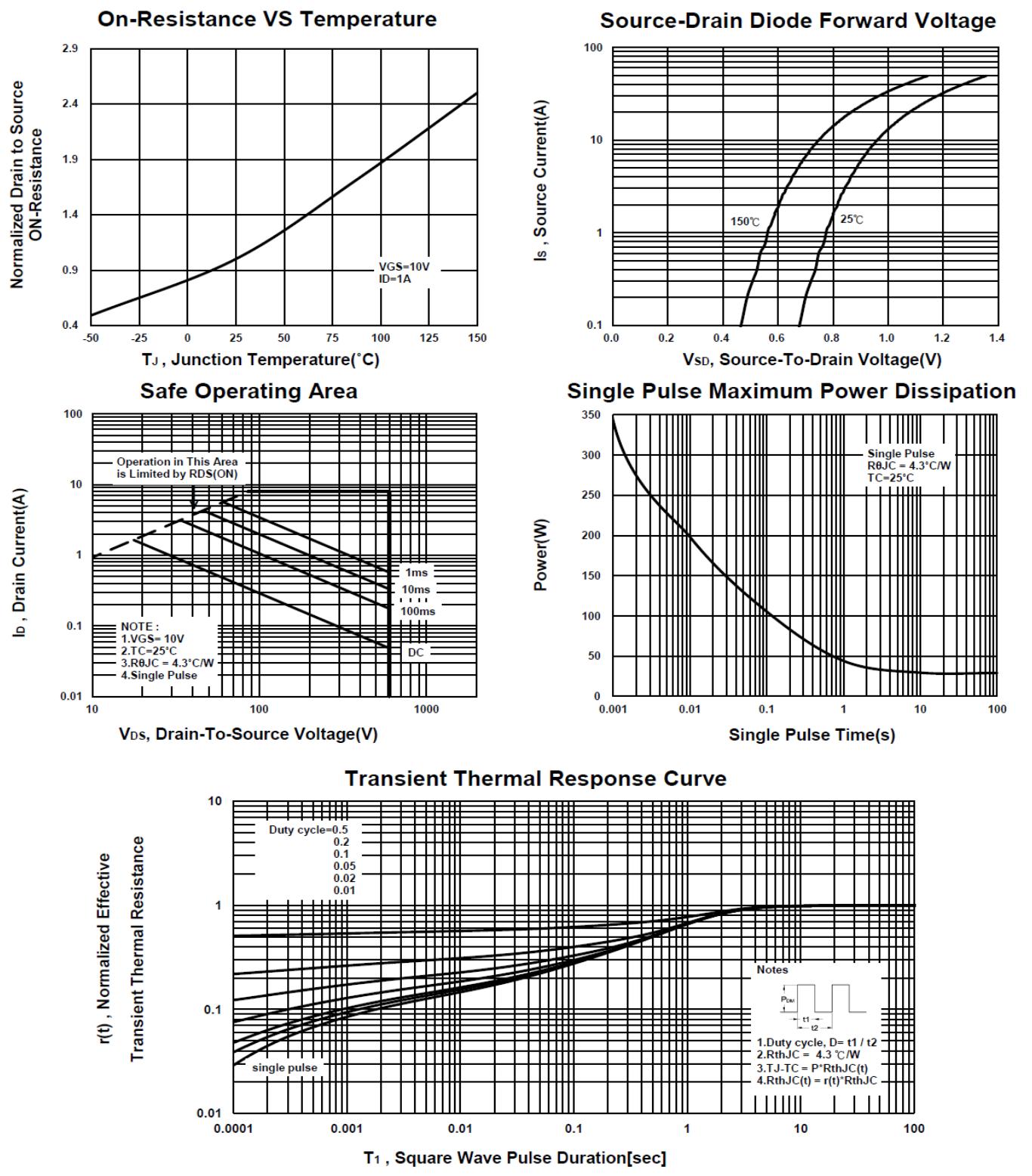


On-Resistance VS Drain Current



P0260ETF

N-Channel Enhancement Mode MOSFET





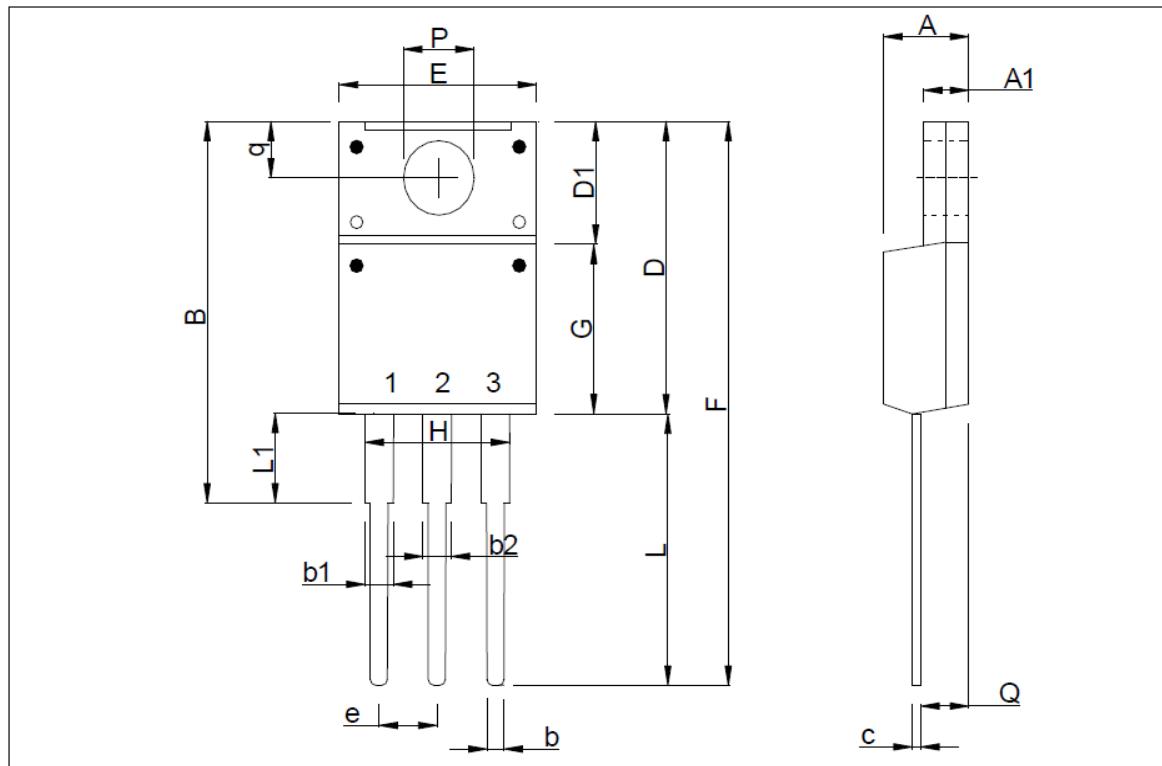
P0260ETF

N-Channel Enhancement Mode MOSFET

Package Dimension

TO-220F (3-Lead) MECHANICAL DATA

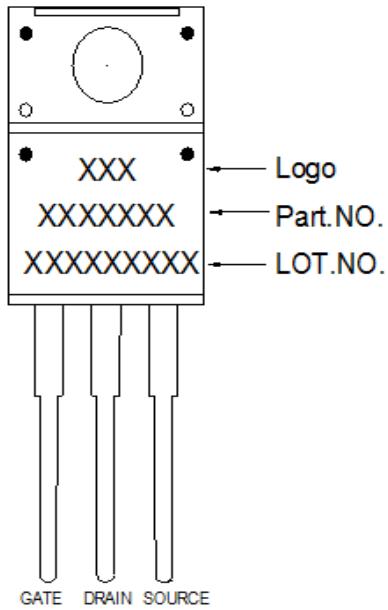
Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	4.2		4.93	e	2.05	2.55	3.05
A1	2.34		3.1	F	27.45		30.6
B	17.77		20.3	G	7.72		9.3
b	0.6		1.05	H	6.1		7.1
b1	0.9	1.23	1.62	L	12.5		14.5
b2	0.6		1.9	L1	1.97		3.8
c	0.4		1.0	P	2.98		3.4
D	14.7		16.4	Q	2.1		2.96
D1	6.4		7.5	q	3.0		3.8
E	9.7		10.4				



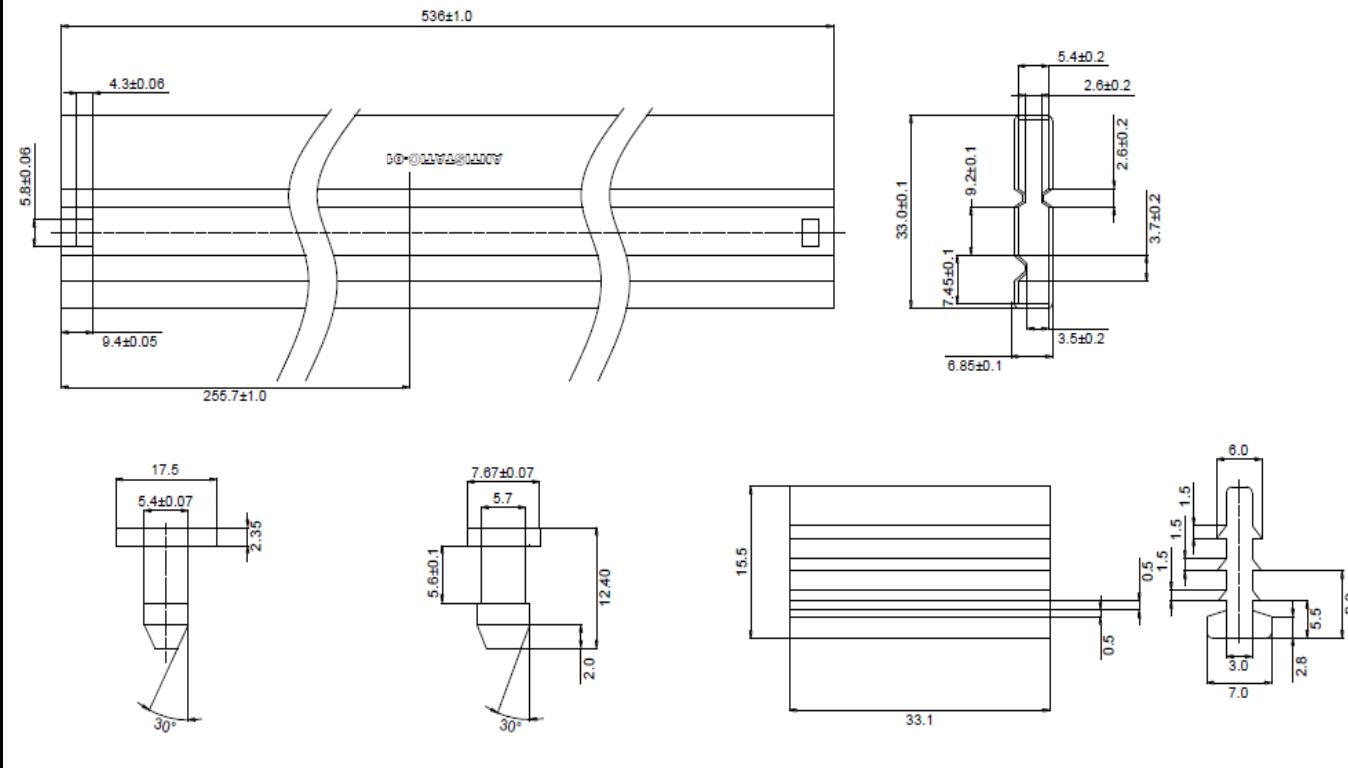
P0260ETF

N-Channel Enhancement Mode MOSFET

A. Marking Information



B. Tape&Reel Information: 50pcs/Tube(2000pcs/Box)



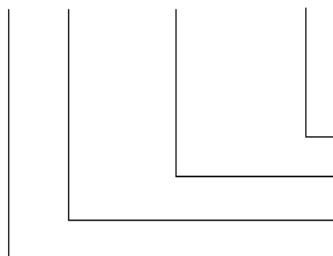
P0260ETF

N-Channel Enhancement Mode MOSFET

C. Lot.No. & Date Code rule

1.LOT.NO.

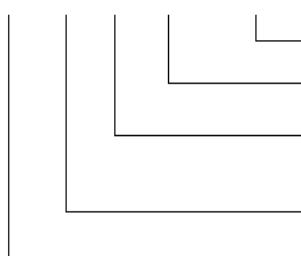
M N 15M21 03



- #8~9 Sub-lot No
- Order series no.
- Foundry site
- Assembly site

2.Date Code

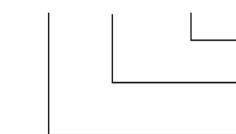
D Y M X XXX



- Order series no. & Sub-lot No
- Week
- M : Month (A:Jan , B:Feb , C:Mar ,D :Apr ,E:May ,F:Jun,G:Jul,H:Aug,I:Sep,J:Oct,K:Nov,L:Dec.)
- Y : Year (N : 2011, O : 2012 ...)
- Assembly site

3.Date Code (for Small package)

XX Y WW



- Week
- Y : Year (9: 2009,A : 2010, B : 2011 ...)
- Device Name

P0260ETF

N-Channel Enhancement Mode MOSFET

D.Label rule

标签内容(Label content)



1	Label Size	30 * 90 mm
2	Font style	Times New Roman or Arial (或可区分英文“0”和数字“0”，“G”和“Q”的字型即可)
3	Great Power	Height: 4 mm
4	Package	Height: 2 mm
5	Date	Height: 2 mm Shipping date: YYYY/MM/DD, ex. 2008/09/12
6	Device	Height: 3 mm (Max: 16 Digit)
7	Lot	Height: 3 mm (Max: 9 Digit) Sub lot
8	D/C	Height: 3 mm (Max: 7 Digit)
9	QTY	Height: 3 mm (Max: 6 Digit) Thousand mark is no needed
10	Pb Free label	 Diameter: 1 cm bottom color: Green Font color: Black Font style: Arial
11	Halogen Free label	 Diameter: 1 cm bottom color: Green Font color: Black Font style: Arial
12	Scan info	Device / Lot / D/C / QTY , Insert “/” between every parts. for example: P3055LDG/G12345601/GGG2301/2000 DPI (Dots per inch): Over 300 dpi Code : Code 128 Height: 6 mm at least