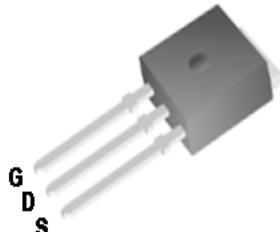


P0460EI

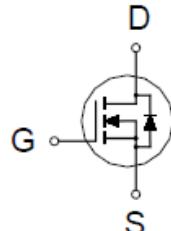
N-Channel Enhancement Mode MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
600V	2.3Ω @ $V_{GS} = 10V$	4A



TO-251



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Drain-Source Voltage	V_{DS}	600	V
Gate-Source Voltage	V_{GS}	± 30	
Continuous Drain Current ²	I_D	4	A
		2.5	
Pulsed Drain Current ^{1,2}	I_{DM}	20	
Avalanche Current ³	I_{AS}	4	
Avalanche Energy ³	E_{AS}	80	mJ
Power Dissipation	P_D	62.5	W
		25	
Operating Junction & Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta JC}$	2	62.5	°C / W
Junction-to-Ambient	$R_{\theta JA}$			

¹Pulse width limited by maximum junction temperature.

²Limited only by maximum temperature allowed

³ $V_{DD} = 50V$, $L = 10mH$, starting $T_J = 25^\circ C$

P0460EI

N-Channel Enhancement Mode MOSFET

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$	600			V
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}, I_D = 250\mu\text{A}$	2	3.2	4	
Gate-Body Leakage	I_{GSS}	$V_{\text{DS}} = 0\text{V}, V_{\text{GS}} = \pm 30\text{V}$			± 100	nA
Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = 600\text{V}, V_{\text{GS}} = 0\text{V}, T_C = 25^\circ\text{C}$			1	μA
		$V_{\text{DS}} = 480\text{V}, V_{\text{GS}} = 0\text{V}, T_C = 100^\circ\text{C}$			10	
Drain-Source On-State Resistance ¹	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}} = 10\text{V}, I_D = 2\text{A}$		1.85	2.3	Ω
Forward Transconductance ¹	g_{fs}	$V_{\text{DS}} = 15\text{V}, I_D = 2\text{A}$		5.8		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 25\text{V}, f = 1\text{MHz}$		517		pF
Output Capacitance	C_{oss}			62		
Reverse Transfer Capacitance	C_{rss}			11		
Total Gate Charge ²	Q_g	$V_{\text{DD}} = 480\text{V}, I_D = 4\text{A}, V_{\text{GS}} = 10\text{V}$		18		nC
Gate-Source Charge ²	Q_{gs}			2.8		
Gate-Drain Charge ²	Q_{gd}			8.3		
Turn-On Delay Time ²	$t_{\text{d}(\text{on})}$	$V_{\text{DD}} = 300\text{V}, I_D = 4\text{A}, V_{\text{GS}} = 10\text{V}, R_G = 25\Omega$		18		nS
Rise Time ²	t_r			46		
Turn-Off Delay Time ²	$t_{\text{d}(\text{off})}$			46		
Fall Time ²	t_f			50		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_J = 25^\circ\text{C}$)						
Continuous Current ³	I_S				4	A
Forward Voltage ¹	V_{SD}	$I_F = 4\text{A}, V_{\text{GS}} = 0\text{V}$			1.5	V
Reverse Recovery Time	t_{rr}	$I_F = 4\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$		383		nS
Reverse Recovery Charge	Q_{rr}			2.2		μC

¹Pulse test : Pulse Width $\leq 300\ \mu\text{sec}$, Duty Cycle $\leq 2\%$.

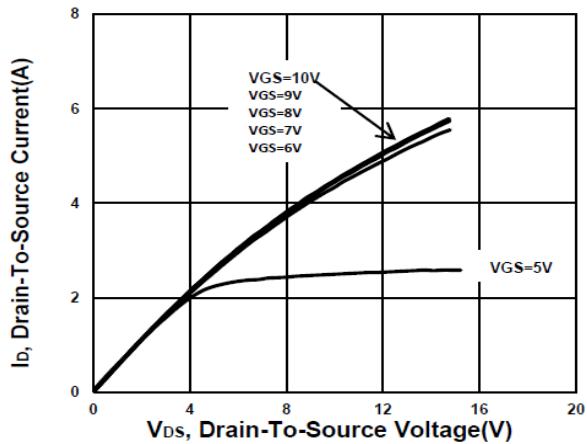
²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

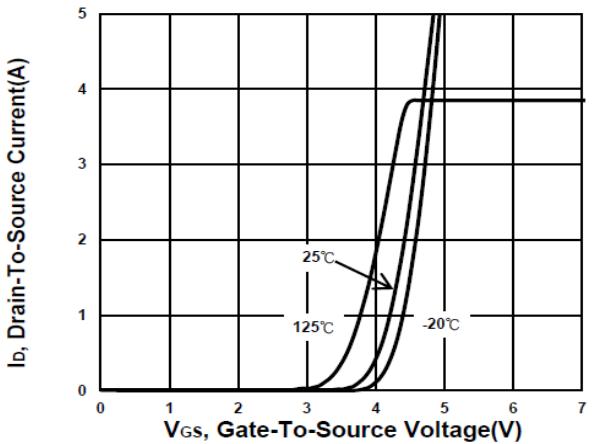
P0460EI

N-Channel Enhancement Mode MOSFET

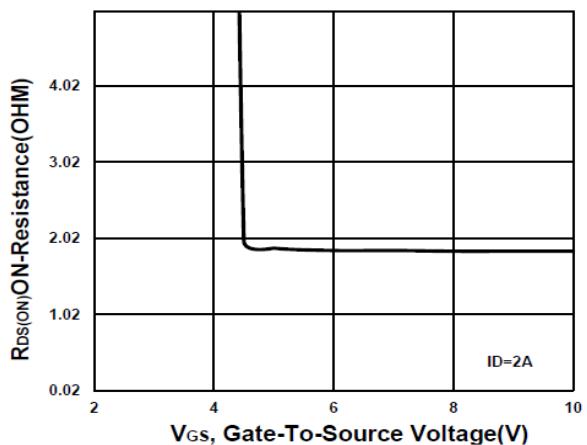
Output Characteristics



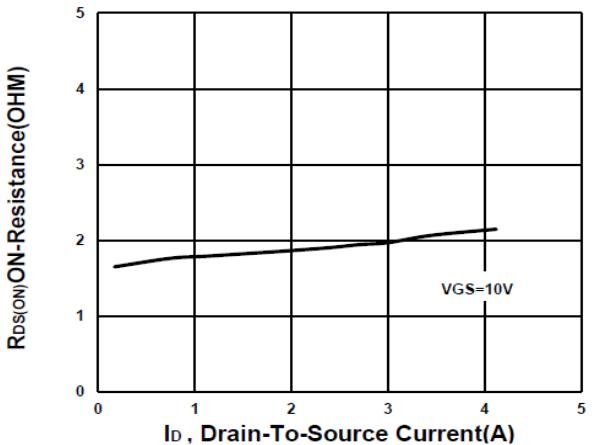
Transfer Characteristics



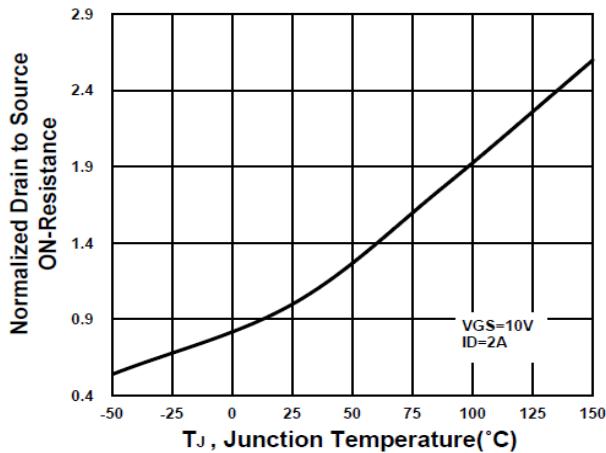
On-Resistance VS Gate-To-Source



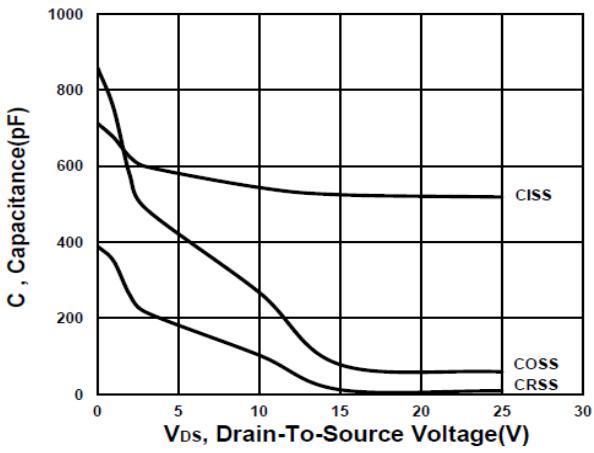
On-Resistance VS Drain Current



On-Resistance VS Temperature

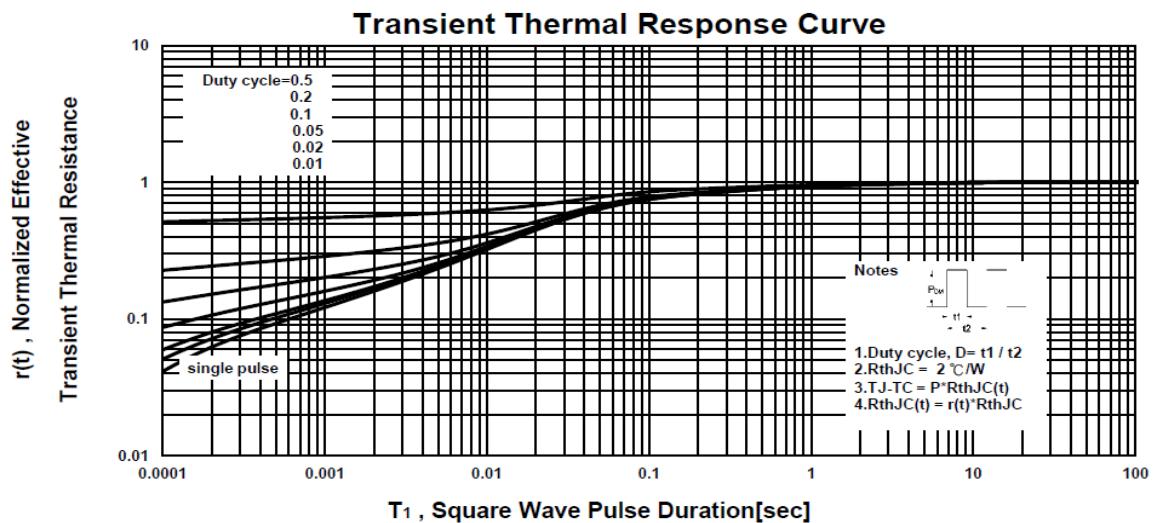
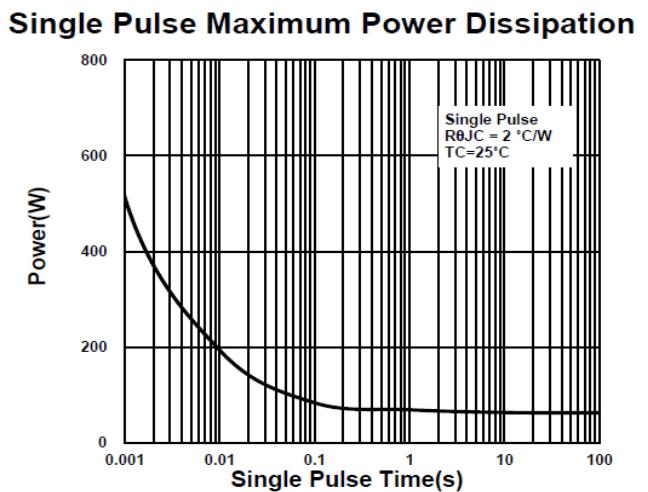
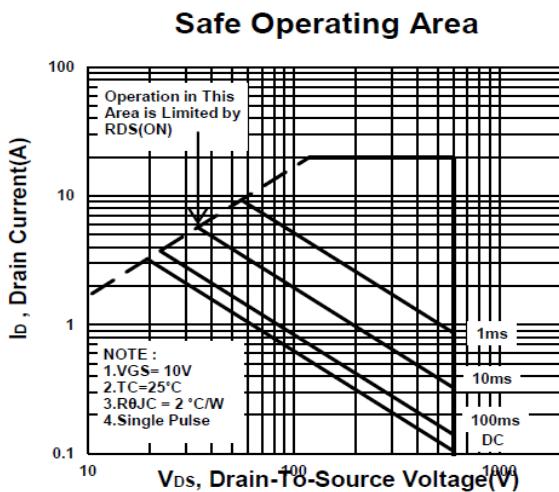
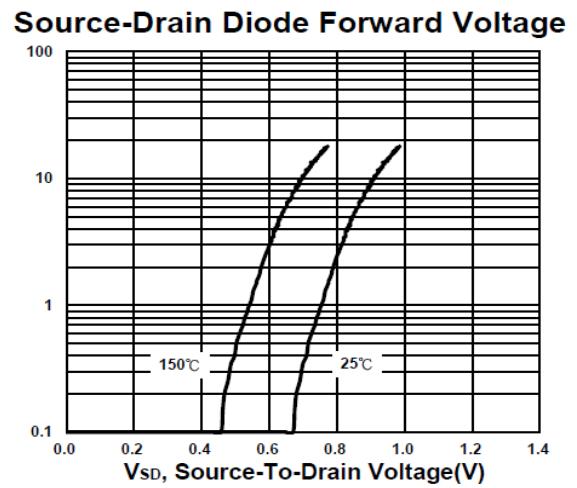
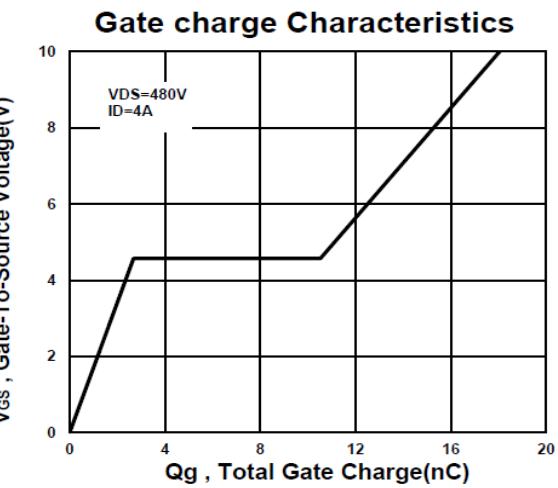


Capacitance Characteristic



P0460EI

N-Channel Enhancement Mode MOSFET



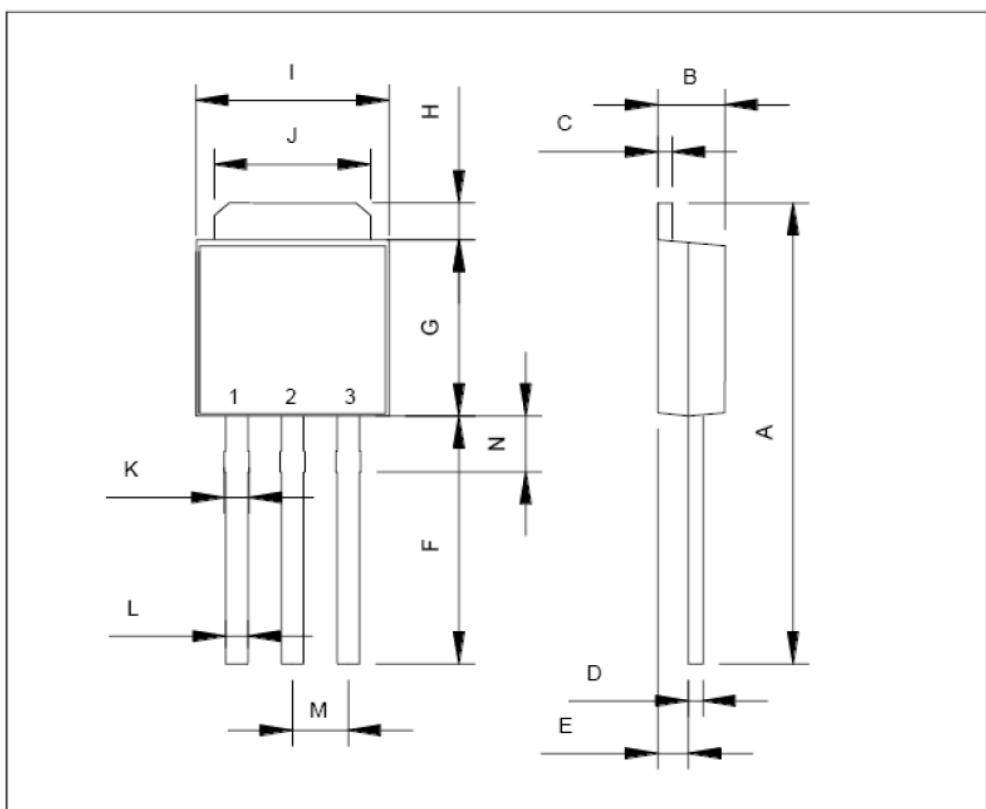
P0460EI

N-Channel Enhancement Mode MOSFET

Package Dimension

TO-251 MECHANICAL DATA

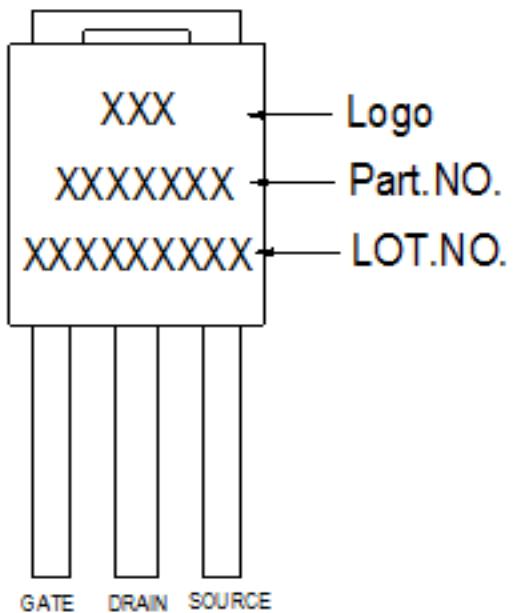
Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	14	15	17.14	H	0.89		1.7
B	2.1	2.3	2.5	I	6.3		6.8
C	0.4	0.5	0.6	J	4.8		5.5
D	0.35	0.5	0.65	K	0.5	0.84	1.14
E	0.9	1.1	1.5	L	0.4	0.76	0.912
F	7		9.65	M		2.3	
G	5.3		6.22	N	1.4	2.16	2.23



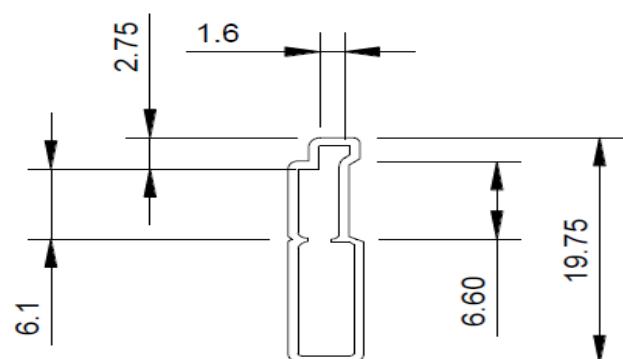
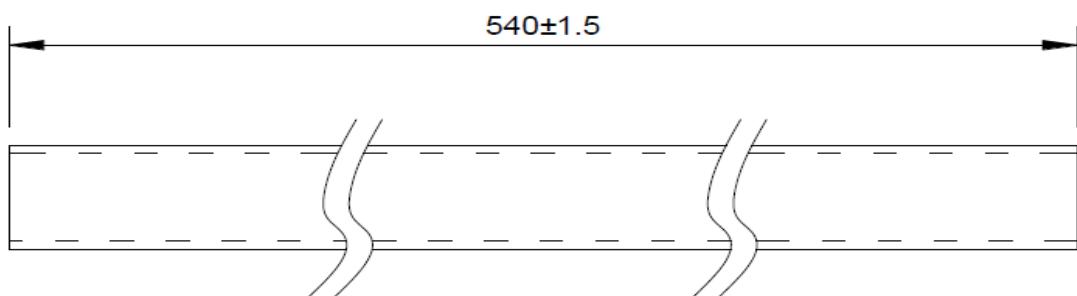
P0460EI

N-Channel Enhancement Mode MOSFET

A. Marking Information



B. Tape&Reel Information: 75pcs/Tube



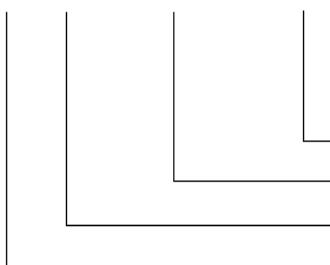
P0460EI

N-Channel Enhancement Mode MOSFET

C. Lot.No. & Date Code rule

1.LOT.NO.

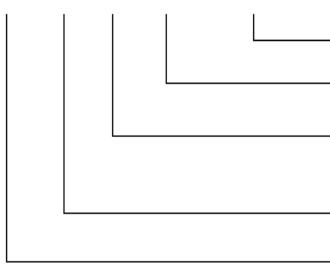
M N 15M21 03



- #8~9 Sub-lot No
- Order series no.
- Foundry site
- Assembly site

2.Date Code

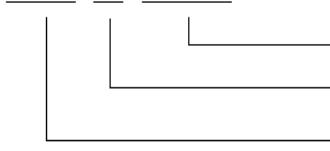
D Y M X XXX



- Order series no. & Sub-lot No
- Week
- M : Month (A:Jan, B:Feb, C:Mar, D:Apr, E:May, F:Jun, G:Jul, H:Aug, I:Sep, J:Oct, K:Nov, L:Dec.)
- Y : Year (N : 2011, O : 2012 ...)
- Assembly site

3.Date Code (for Small package)

XX Y WW



- Week
- Y : Year (9: 2009, A : 2010, B : 2011 ...)
- Device Name

P0460EI

N-Channel Enhancement Mode MOSFET

D.Label rule

标签内容(Label content)



1	Label Size	30 * 90 mm
2	Font style	Times New Roman or Arial (或可区分英文“0”和数字“0”，“G”和“Q”的字型即可)
3	Great Power	Height: 4 mm
4	Package	Height: 2 mm
5	Date	Height: 2 mm Shipping date: YYYY/MM/DD, ex. 2008/09/12
6	Device	Height: 3 mm (Max: 16 Digit)
7	Lot	Height: 3 mm (Max: 9 Digit) Sub lot
8	D/C	Height: 3 mm (Max: 7 Digit)
9	QTY	Height: 3 mm (Max: 6 Digit) Thousand mark is no needed
10	Pb Free label	 Diameter: 1 cm bottom color: Green Font color: Black Font style: Arial
11	Halogen Free label	 Diameter: 1 cm bottom color: Green Font color: Black Font style: Arial
12	Scan info	Device / Lot / D/C / QTY , Insert “ / “ between every parts. for example: P3055LDG/G12345601/GGG2301/2000 DPI (Dots per inch): Over 300 dpi Code : Code 128 Height: 6 mm at least