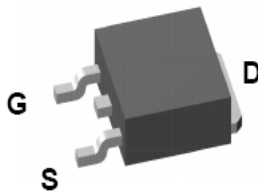


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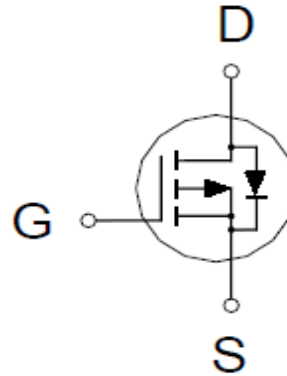
P-Channel Logic Level Enhancement Mode MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
-30V	7.5m Ω @ $V_{GS} = -10V$	-68A



TO-252



ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	± 25	V
Continuous Drain Current ²	$T_C = 25\text{ }^\circ\text{C}$	I_D	-68	A
	$T_C = 100\text{ }^\circ\text{C}$		-43	
Pulsed Drain Current ¹		I_{DM}	-160	
Avalanche Current		I_{AS}	-65	
Avalanche Energy	$L=0.1\text{mH}$	E_{AS}	214	mJ
Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	60	W
	$T_C = 100\text{ }^\circ\text{C}$		24	
Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta JC}$		2.08	$^\circ\text{C} / \text{W}$

¹Pulse width limited by maximum junction temperature.

²The maximum current rating is package limited.

P0703ED

P-Channel Logic Level Enhancement Mode MOSFET

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

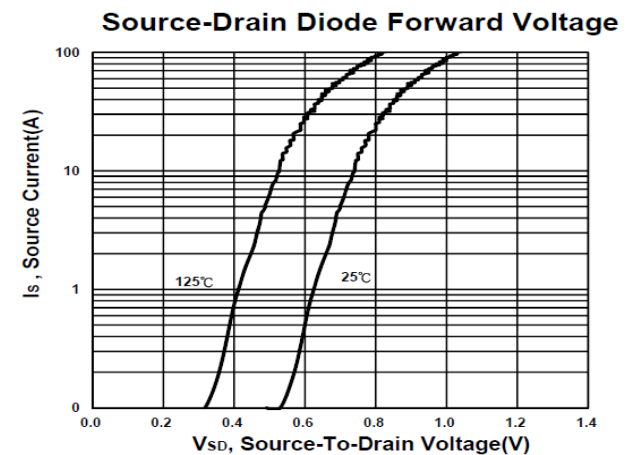
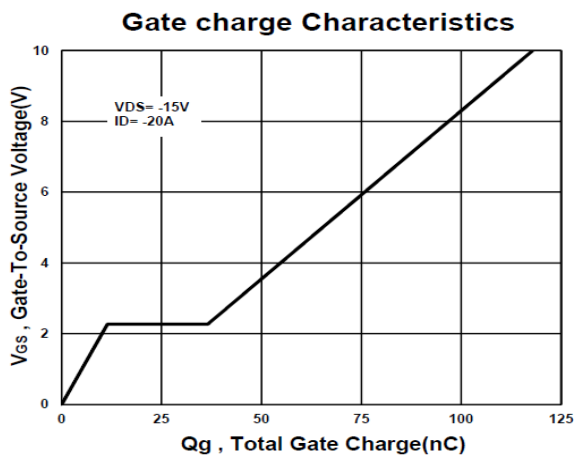
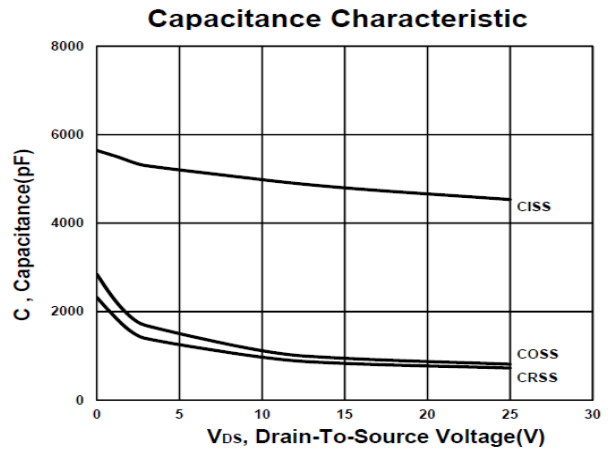
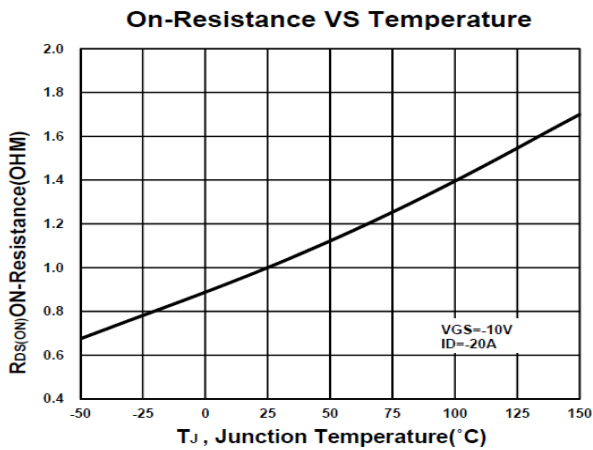
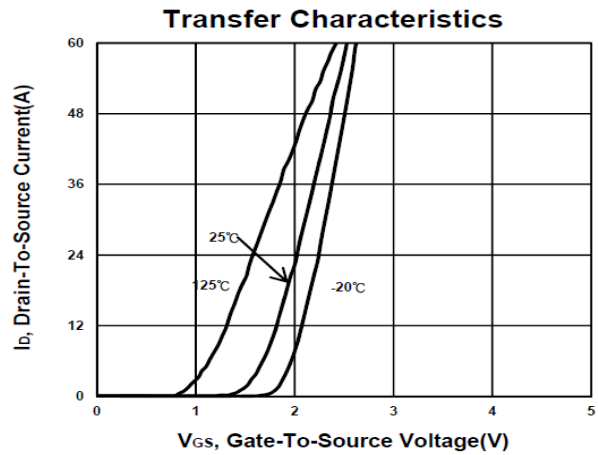
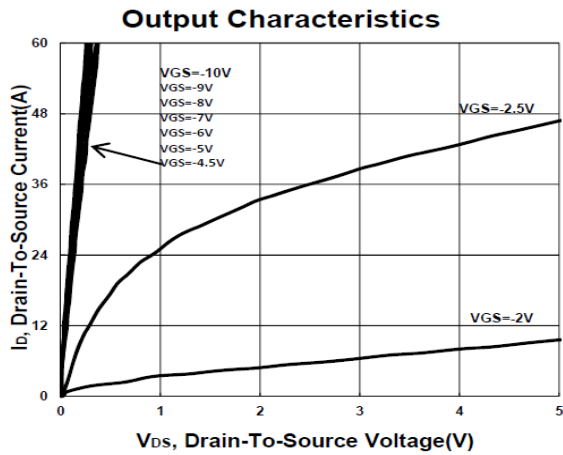
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS	
			MIN	TYP	MAX		
STATIC							
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250μA	-30			V	
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	-1	-1.4	-3	V	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±16V			±30	μA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -24V, V _{GS} = 0V			1	μA	
		V _{DS} = -20V, V _{GS} = 0V, T _J = 125°C			10		
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = -5V, V _{GS} = -10V	-160			A	
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = -4.5V, I _D = -20A		6	12	mΩ	
		V _{GS} = -10V, I _D = -20A		4	7.5		
Forward Transconductance ¹	g _{fs}	V _{DS} = -5V, I _D = -20A		58		S	
DYNAMIC							
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = -15V, f = 1MHz		5110		pF	
Output Capacitance	C _{oss}			995			
Reverse Transfer Capacitance	C _{rss}			850			
Gate Resistance	R _g	V _{GS} = 0V, V _{DS} = 0V, f = 1MHz		2.7		Ω	
Total Gate Charge ²	Q _g	V _{GS} = -10V	V _{DS} = -15V, I _D = -20A		118	nC	
		V _{GS} = -4.5V			61		
Gate-Source Charge ²	Q _{gs}			12			
Gate-Drain Charge ²	Q _{gd}			30			
Turn-On Delay Time ²	t _{d(on)}	V _{DS} = -15V, I _D ≅ -20A, V _{GS} = -10V, R _{GS} = 6Ω			32		nS
Rise Time ²	t _r				24		
Turn-Off Delay Time ²	t _{d(off)}			90			
Fall Time ²	t _f			44			
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_J = 25 °C)							
Continuous Current	I _S				-46	A	
Forward Voltage ¹	V _{SD}	I _F = -10A, V _{GS} = 0V			-1.3	V	
Reverse Recovery Time	t _{rr}	I _F = -20A, dI _F /dt = 100A / μS		33		nS	
Reverse Recovery Charge	Q _{rr}			17		nC	

¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

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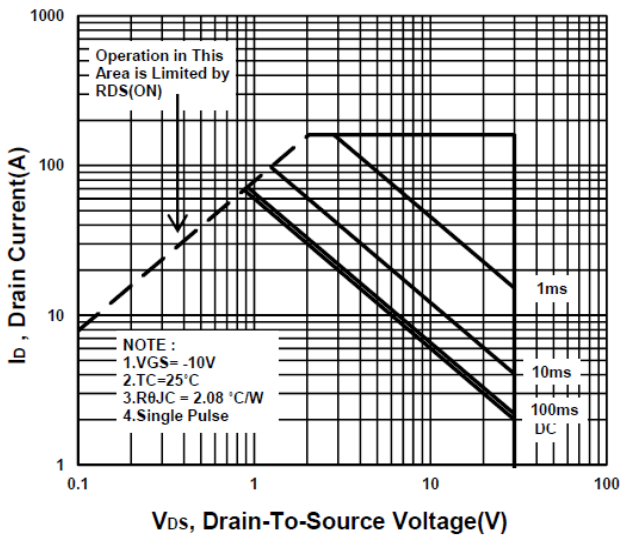
P-Channel Logic Level Enhancement Mode MOSFET



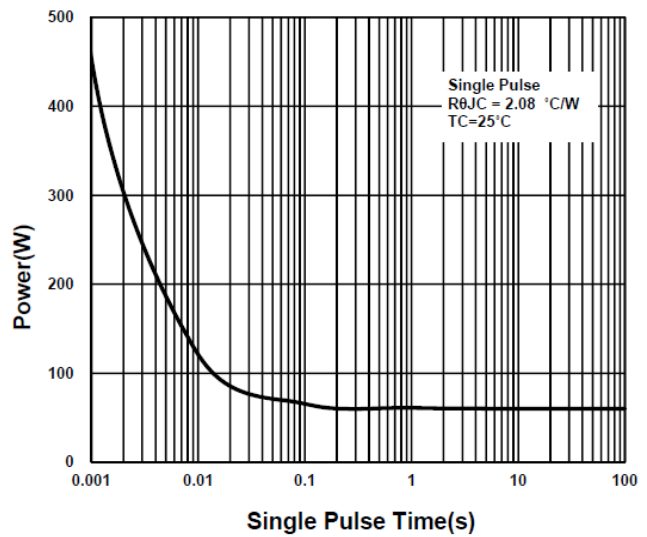
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P-Channel Logic Level Enhancement Mode MOSFET

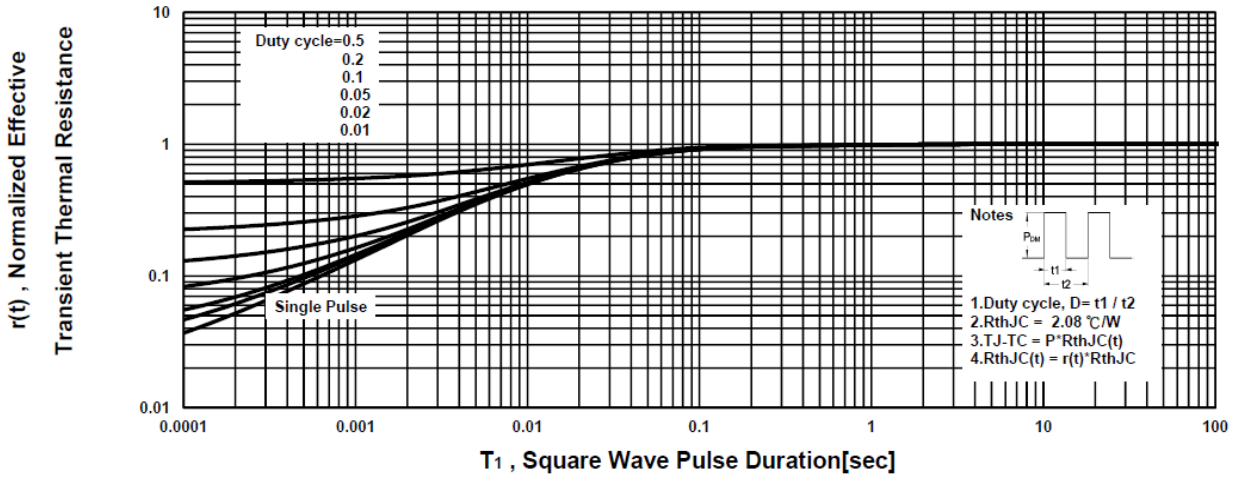
Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve



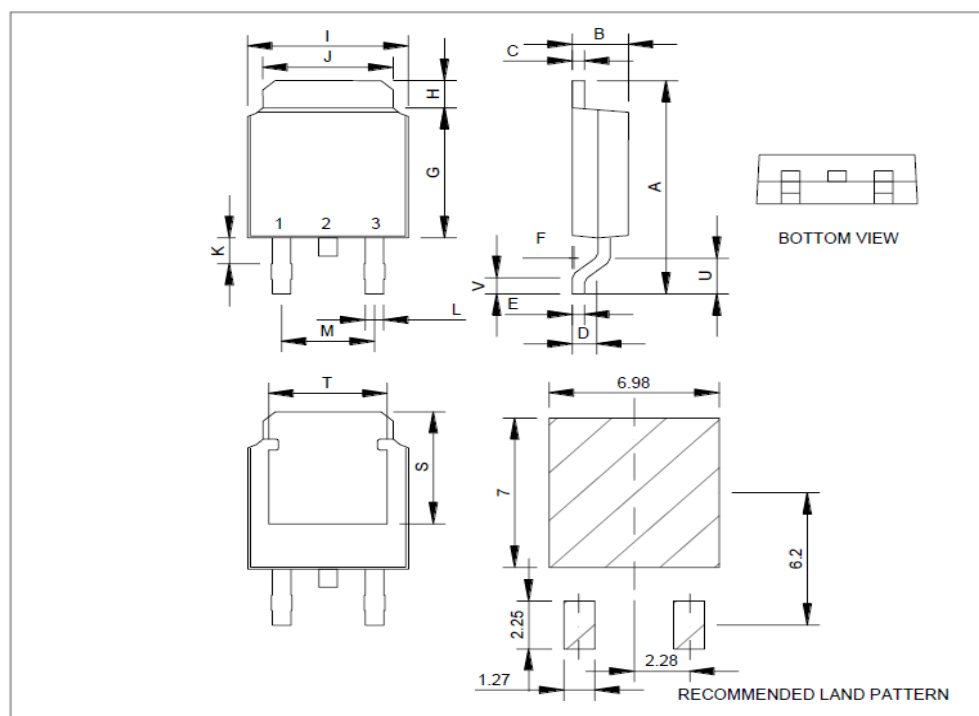
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P-Channel Logic Level Enhancement Mode MOSFET

Package Dimension

TO-252 (DPAK) MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	8.9	10	10.41	J	4.8		5.64
B	2.1	2.2	2.4	K	0.15		1.1
C	0.4	0.5	0.61	L	0.4	0.76	0.89
D	0.82	1.2	1.5	M	4.2	4.58	5
E	0.4	0.5	0.61	S	4.9	5.1	5.3
F	0		0.2	T	4.6	4.75	5.44
G	5.3	6.1	6.3	U	1.4		1.78
H	0.9		1.7	V	0.55	1.25	1.7
I	6.3	6.5	6.8				



*因为各家封装模具不同而外观略有所差异，不影响电性及Layout。