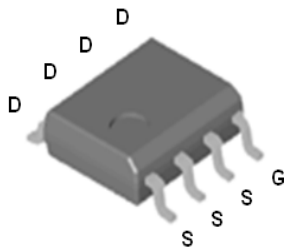


P0804BVG

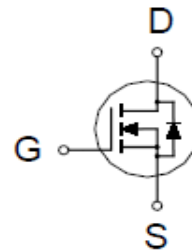
N-Channel Logic Level Enhancement Mode MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
40V	12m Ω @ $V_{GS} = 10V$	12A



SOP-08



100% UIS tested
100% Rg tested

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25\text{ }^\circ\text{C}$	I_D	12	A
	$T_C = 100\text{ }^\circ\text{C}$		8	
Pulsed Drain Current ¹		I_{DM}	50	
Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	2.5	W
	$T_C = 100\text{ }^\circ\text{C}$		1	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	$^\circ\text{C}$
Lead Temperature (¹ / ₁₆ " from case for 10 sec.)		T_L	275	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta JC}$		25	$^\circ\text{C} / \text{W}$
Junction-to-Ambient	$R_{\theta JA}$		50	
Case-to-Heatsink	$R_{\theta CS}$	0.5		

¹Pulse width limited by maximum junction temperature.

P0804BVG

N-Channel Logic Level Enhancement Mode MOSFET

ELECTRICAL CHARACTERISTICS (T_C = 25 °C, Unless Otherwise Noted)

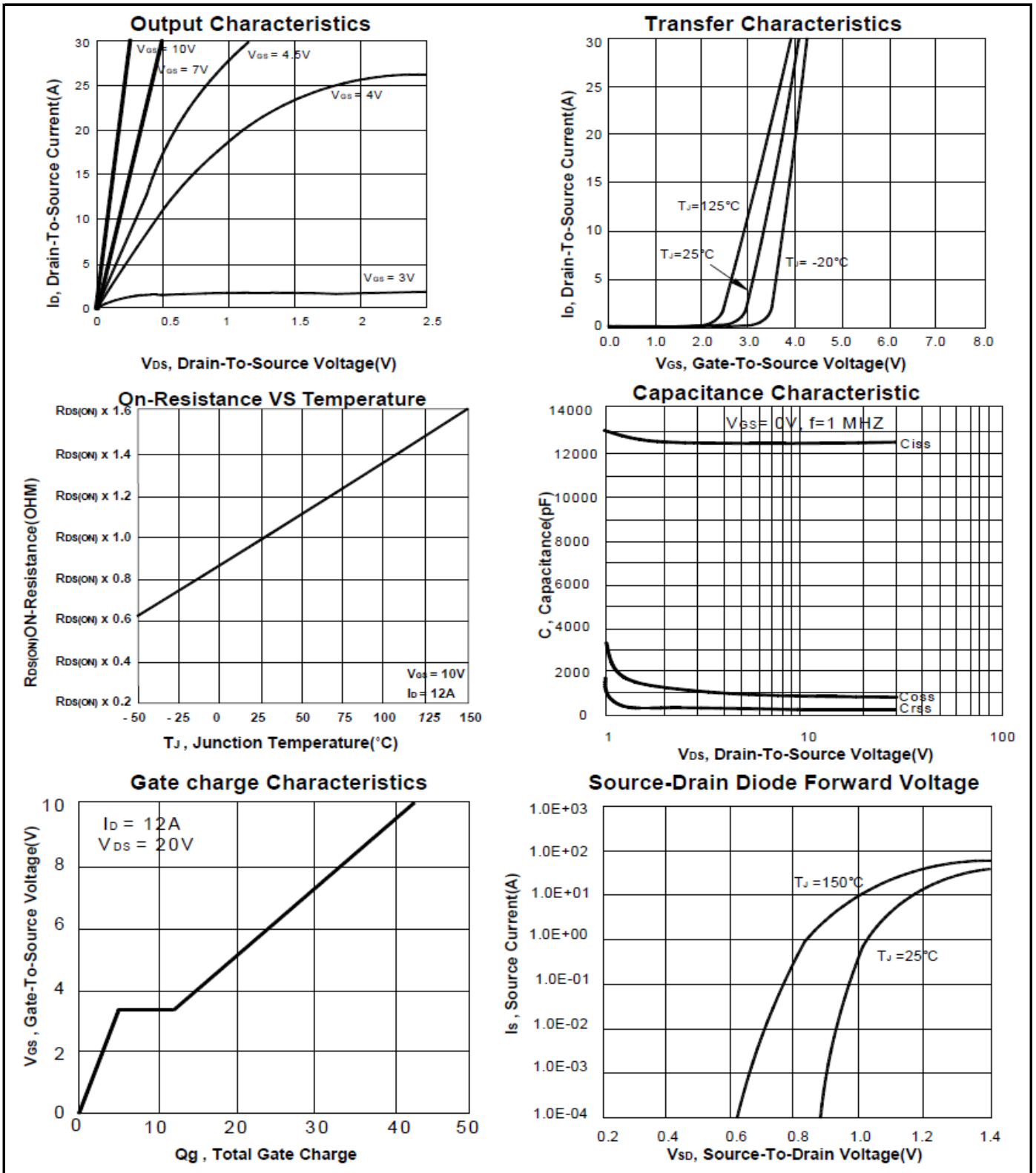
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	40			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1.5	2.0	3.0	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±250	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 32V, V _{GS} = 0V			1	μA
		V _{DS} = 30V, V _{GS} = 0V, T _C = 125 °C			10	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	50			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = 7V, I _D = 12A		11	15	mΩ
		V _{GS} = 10V, I _D = 12A		7	12	
Forward Transconductance ¹	g _{fs}	V _{DS} = 10V, I _D = 12A		25		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = 20V, f = 1MHz		2100	2730	pF
Output Capacitance	C _{oss}			360	450	
Reverse Transfer Capacitance	C _{rss}			330	415	
Total Gate Charge ²	Q _g	V _{DS} = 0.5V _{(BR)DSS} , V _{GS} = 10V, I _D = 12A		43		nC
Gate-Source Charge ²	Q _{gs}			6.3		
Gate-Drain Charge ²	Q _{gd}			5.5		
Turn-On Delay Time ²	t _{d(on)}	V _{DS} = 20V, R _L = 1Ω I _D ≅ 12A, V _{GS} = 10V, R _{GEN} = 6Ω		6.8	11.2	nS
Rise Time ²	t _r			18.0	28.8	
Turn-Off Delay Time ²	t _{d(off)}			26.5	42.5	
Fall Time ²	t _f			8.7	15.8	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I _S				1.7	A
Forward Voltage ¹	V _{SD}	I _F = I _S , V _{GS} = 0V			1.4	V
Reverse Recovery Time	t _{rr}	I _F = 12A, di _F /dt = 100A / μS		75		nS
Reverse Recovery Charge	Q _{rr}			55		nC

¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

P0804BVG

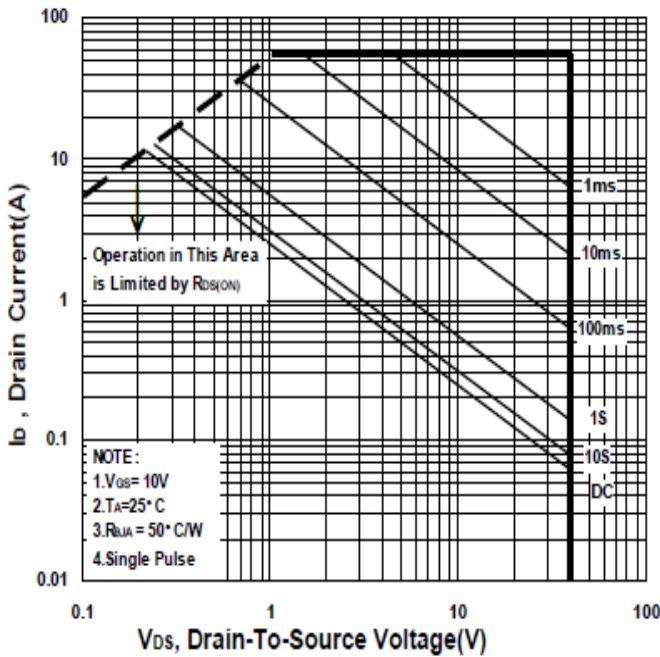
N-Channel Logic Level Enhancement Mode MOSFET



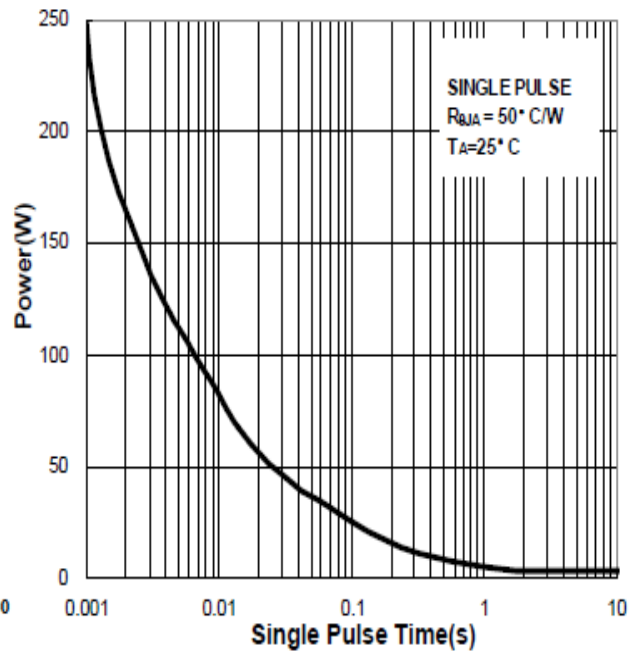
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N-Channel Logic Level Enhancement Mode MOSFET

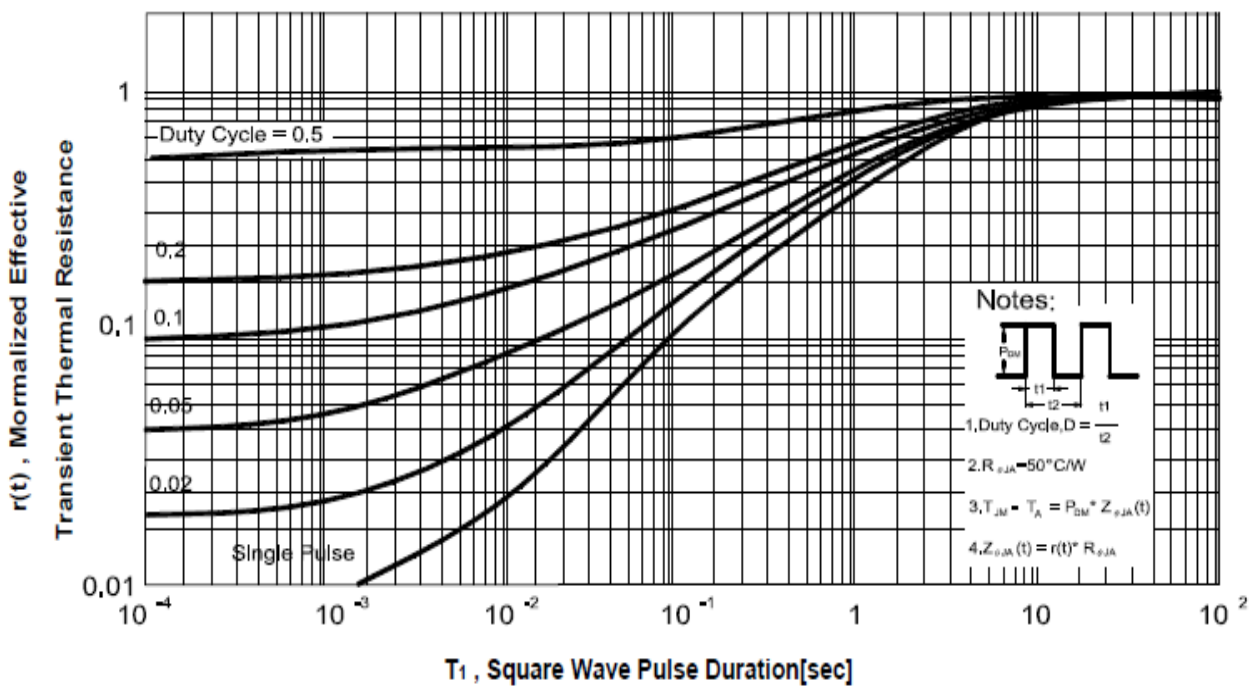
Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve



P0804BVG

N-Channel Logic Level Enhancement Mode MOSFET

Package Dimension

SOP-8 MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	4.8	4.9	5.0	H	0.4	0.6	0.93
B	3.8	3.9	4.0	I	0.19	0.21	0.25
C	5.79	6.0	6.2	J	0.25	0.375	0.5
D	0.33	0.4	0.51	K	0°	3°	18°
E	1.25	1.27	1.29				
F	1.1	1.3	1.65				
G	0.05	0.15	0.25				

