

P1032BF1 Datasheet

ARM Cortex-M3 MCU

Rev 1.3

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Revision History

Date	Revision	Description
2018-9-3	V1.0	
2018-9-28	V1.1	Change the order of the 5 pin and the 6 pin. Modify the Minimum supply voltage at the LDOIN pin.
2018-10	V1.2	1. Modify the package size. 2. Add the description of the GPIO_B4 as the upgrade detection IO.
2019-3	V1.3	1. Modify the UART_RX PIN No. 2. Modify SZ office's TELNo. 3. Modify GPIOB4 description.

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1. Overview

P1032BF1 is an ARM Cortex-M3 based MCU specially designed for Wi-Fi / Bluetooth communication control. P1032BF1 has large embedded SRAM and support large program code, it can also be used in general MCU applications.

1.1 Features

- Core: ARM Cortex-M3, 96MHz max
- Memories:
 - Embedded 8M bits flash for program code and data storage
 - 128K byte SRAM
- Clock, reset and supply management:
 - Embedded LDO, support power supply from 3.3V to 5V
 - Embedded POR, LVD, WDG
 - 32.768KHz oscillator for system PLL and RTC
 - 1 to 30MHz clock input for system PLL
 - Internal 48MHz factory-trimmed RC
- Low power:
 - Sleep, Deep Sleep modes
 - Separated power supply for RTC and 176Byte backup registers
- Audio DAC with volume control
- 5 channels 12-bit SARADC
- Debug mode: Serial Wire Debug(SWD)
- 22 I/O port with interrupt capability
- Connectivity
 - 2 UARTs
 - 1 SPI master, 1 SPI slave
 - 1 SDIO interface
 - OTG 2.0 full-speed controller with OTG PHY
 - IR (NEC) decoder
- Firmware protect and Upgrade:
 - 48-bit unique ID
 - Code encryption mechanism for flash code
 - Firmware can be updated through SD or USB disk
- Timers
 - 3 timers
 - 7 PWM, 1 PWC

2. Pin Description

P1032BF1 is a CMOS device. Floating level on input signals causes unstable device operation and abnormal current consumption. Pull-up or Pull-down resistors should be used appropriately for input or bidirectional pins.

Notation	Description
I	Input
O	Output
I/O	Bidirectional
PWR	Power
GND	Ground

2.1 Pin Description

Table 1 Pin Description

Pin Name	Pin #	Type	Description
GPIO/MCU IO pins			
GPIO_A[1:0]	14:13	I/O	GPIO PORT, bank A
GPIO_A[12:11]	16:15	I/O	
GPIO_A[21:19]	19:17	I/O	
GPIO_A[25:24]	21:20	I/O	
GPIO_B[4]	22	I/O	GPIO PORT, bank B
GPIO_B[9:6]	26:23	I/O	
GPIO_B[24:20]	31:27	I/O	
GPIO_C[2]	32	I/O	GPIO PORT, bank C
GPIO_C[14:13]	2:1	I/O	
Audio DAC interface pins			
DAC_VMID	4	AI	Internal voltage reference
DAC_OUT	5	AO	Audio DAC output
CLK pins			
XI	7	I	32.768KHz Crystal oscillator input for PLL
XO	8	O	32.768KHz Crystal oscillator output for PLL
Power/Ground pins			
DVSS	33	GND	Digital ground @ Epad
LDOIN	10	PWR	LDO power in
LDO330	9	PWR	LDO 3.3V out
LDO120	11	PWR	LDO 1.2V out
RTCVDD	12	PWR	Power for RTC
DACVDD	6	PWR	Power for Audio DAC
AVSS	3	GND	Analog ground for DAC

Pin Name	Default Status @ power-on	Other Function Assignment
GPIO_A[0]	Pull-down	PWM0 / UART TX
GPIO_A[1]	Pull-down	PWM1 / UART RX
GPIO_A[11]	Pull-down	32.768K OUT / BUART CTS
GPIO_A[12]	Pull-down	12M 16M OUT / BUART RTS
GPIO_A[19]	Pull-up	SD1_DAT / SPIM1 MISO
GPIO_A[20]	Pull-up	SD1_CLK / SPIM1 CLK
GPIO_A[21]	Pull-up	SD1_CMD / SPIM1 MOSI
GPIO_A[24]	Floating	BUART_RX / USB1_DP
GPIO_A[25]	Floating	BUART_TX / USB1_DM
GPIO_B[4]	Pull-up	If GPIO_B4 is low when powered on and bootloader is running, the upgrade detection function will be triggered. See note 4.
GPIO_B[6]	Pull-up	ADC1 / PWM4 / UART_RX / WAKEUP
GPIO_B[7]	Pull-up	ADC2 / IR1 / PWC1 / PWM5 / UART_TX / WAKEUP
GPIO_B[8]	Pull-up	BUART_RX / PWM6
GPIO_B[9]	Pull-up	BUART_TX / PWM7
GPIO_B[20]	Pull-up	PWM7 / SD3_CMD / SPIM3_MOSI / SPIS_MOSI
GPIO_B[21]	Pull-up	PWM6 / SD3_CLK / SPIM3_CLK / SPIS_CLK
GPIO_B[22]	Pull-up	ADC3 / PWM5 / SD3_DAT / SPIM3_MISO / SPIS_MISO / WAKEUP
GPIO_B[23]	Pull-up	ADC4 / PWM4 / SPIS_CS / WAKEUP
GPIO_B[24]	Pull-up	ADC5 / PWM3 / WAKEUP
GPIO_C[2]	Pull-up	IR2 / WAKEUP
GPIO_C[13]	Pull-down	SWCLK
GPIO_C[14]	Pull-up	SWD

Notes.

- All GPIOs can be used as external interrupt pins.
- For each of the following modules, only one port group can be activated at any given time

Module	Port Groups
IR	IR1, IR2
SD	SD1, SD3
SPIM	SPIM1, SPIM3

- For the following modules, there are two scenarios:

Scenario 1, the signal bus can be activated separately, e.g., use UART_TX or UART_RX only;

Scenario 2, only one port can be allocated to the signal bus at any given time, e.g., UART_RX can be allocated to GPIO_B[6] or GPIO_A[1].

Module	Signal Bus	Ports
UART	UART TX	GPIO_A[0], GPIO_B[7]
	UART RX	GPIO_A[1], GPIO_B[6]
BUART	BUART TX	GPIO_A[25], GPIO_B[9]
	BUART RX	GPIO_A[24], GPIO_B[8]

- GPIO_B4 triggers firmware upgrade detection:

The chip supports the ability to upgrade flash firmware via USB1 port, which requires GPIO_B4 as the trigger IO for the upgrade. Please refer to the upgrade manual for details.

3. Package

3.1 Package Diagram

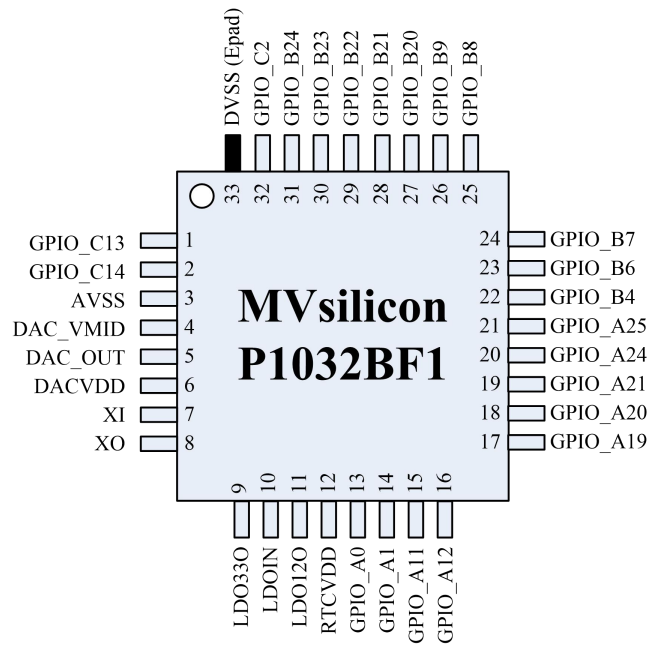


Figure 1 Package Diagram (QFN32-5x5mm / TOP View)

3.2 Package Dimension Parameter

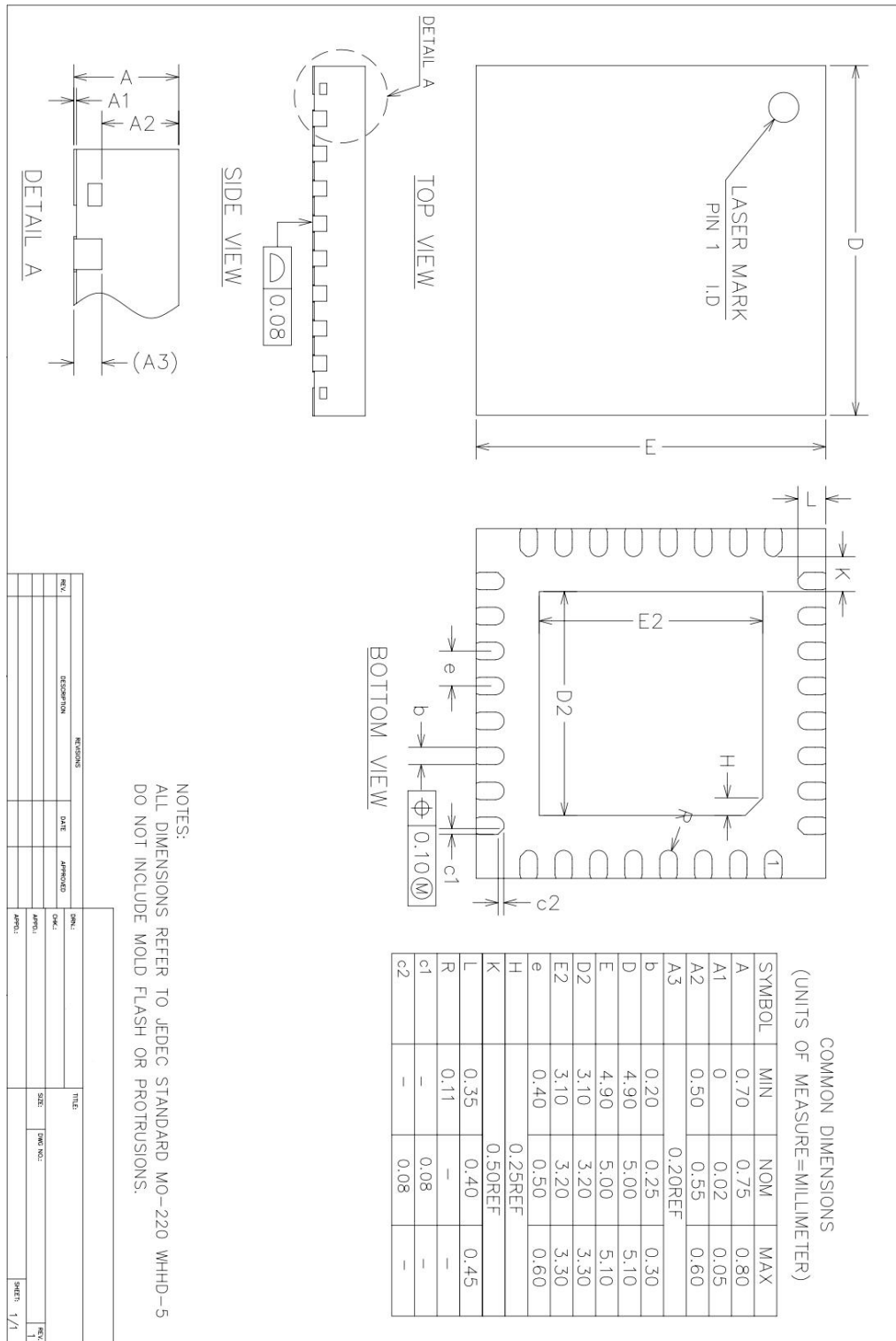


Figure 2 QFN32-5x5mm Package Dimension Parameter

4. Electrical Specification

4.1 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Storage Temperature	TEMP STG	-65 to 150	C

4.2 Recommended Operating Conditions

Table 4 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	LDOIN	2.9	5.0	5.5	V
IO Input Voltage	VIN	0		3.6	V
Operating Free Air Temperature	TEMP OPR	-40		85	C

4.3 Electrical Characteristics

Table 5 Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIH	Input High Voltage		1.6		3.6	V
VIL	Input Low Voltage		-0.3		1.4	V
VOH	Output high voltage	@IOH=2mA	3.0			V
VOL	Output low voltage	@IOL=2mA			0.3	V
IL	Input leakage current		-10		10	uA
Power Down mode current	Current consumption for RTC & backup registers			20		uA
Deep Sleep mode current				2		mA

4.4 LDO330 driving capability

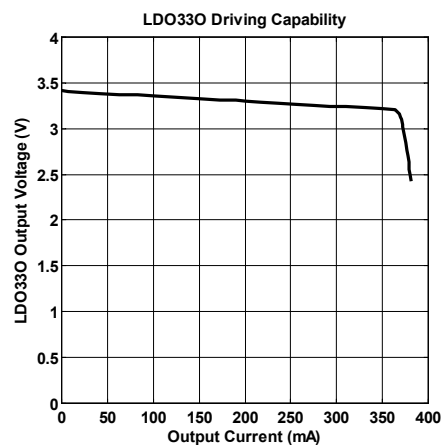


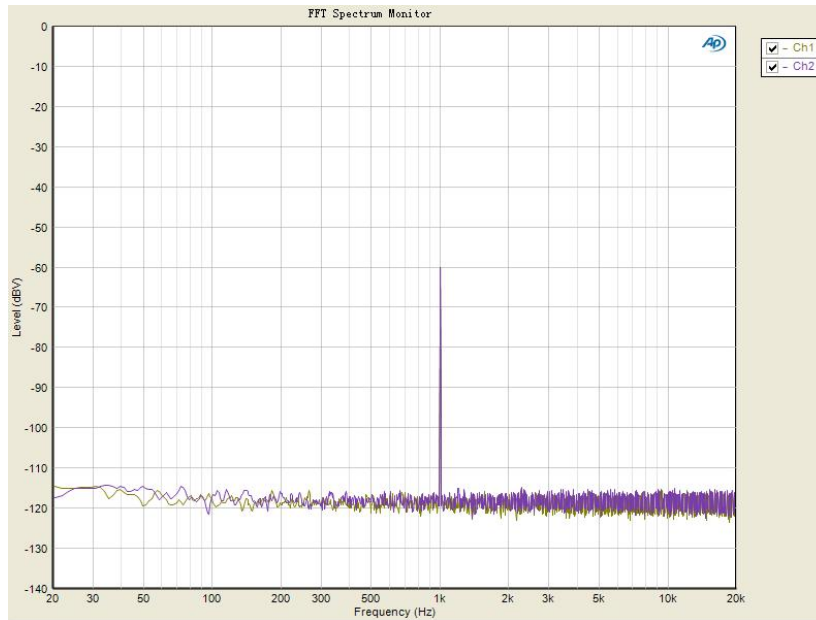
Figure 3 LDO330 driving capability

Note: 1, Not fully tested, characterized only; 2, LDOIN=5V, TA=25°C

4.5 DAC Performance

Table 6 Audio DAC Performance

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dynamic Range	No Filter		93.6/93.6		dB
	With A-Weighted Filter		95/95		dB
Signal-to-Noise Ratio	No Filter		95.5/95.6		dB
	With A-Weighted Filter		98/98		dB
THD+N	Peak THD+N (@0dBFS)		-81/-81		dB
	0dBFS		-75/-75		dB
Frequency Response			0.06		dBV
Output Swing			0.993		Vrms
Inter-channel Gain Mismatch			0.003		dB
Group Delay			80		us
Inter-channel Phase Deviation			0.01		degree
Crosstalk			-99/-98		dB



Note:

1. The measured output audio spectrum when the output is at -60 dBV.
2. “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.

5. Store and Reflow

P1032BF1 is a moisture sensitive component. The moisture sensitivity classification is **Class 3**.

It's important that the parts are handled under precaution and a proper manner.

The handling, baking and out-of-pack storage conditions of the moisture sensitive components are described in IPC/JEDC S-STD-033A.

The Technologies recommends utilizing the standard precautions listed below.

1. Calculated shelf life in Sealed Bag: 12 months at <math><40^{\circ}\text{C}</math> and <math><90\%</math> relative humidity(RH)
2. Peak Package Body Temperature: 250°C
3. After bag is opened, devices that will be subjected to reflow solder of other high temperature process must be:
 - a. Mounted within 168 hours of factory condition $\leq 30^{\circ}\text{C} / 60\% \text{ RH}$
 - b. Stored at <math><10\% \text{ RH}</math> if not used
4. Devices require baking, before mounting if:
 - a. Humidity indicator card is >10% when read at $23\pm 5^{\circ}\text{C}$ immediately after moisture barrier bag is opened
 - b. Items 3a or 3b is not met
5. If baking is required, please refer to J-STD-033 standard for low temperature (40°C) baking requirement in Tape/Reel form.

