UNIKC Semiconductor

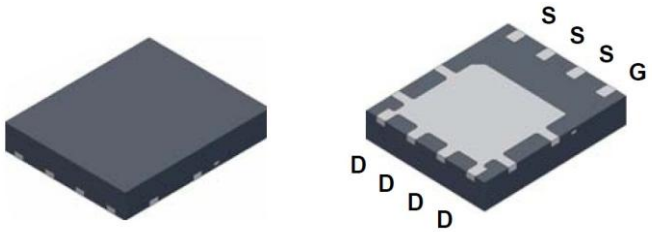
RoHS Compliant

P1203EK

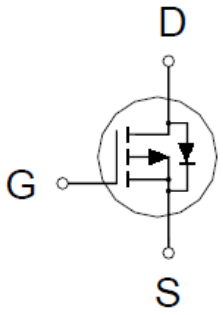
P-Channel Logic Level Enhancement Mode MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
-30V	12mΩ @V_{GS} = 10V	-40A



PDFN 5*6P



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±25	
Continuous Drain Current	T_C = 25 °C	I_D	-40	A
	T_C = 100 °C		-25	
	T_A = 25 °C		-12	
	T_A = 70 °C		-9.6	
Pulsed Drain Current[1]		I_{DM}	-150	
Avalanche Current		I_{AS}	-48	
Avalanche Energy	L = 0.1mH	E_{AS}	117	mJ
Power Dissipation	T_C = 25 °C	P_D	28	W
	T_C = 100 °C		11	
	T_A = 25 °C		2.6	
	T_A = 70 °C		1.6	
Operating Junction & Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

UNIKC Semiconductor

RoHS Compliant

P1203EK

P-Channel Logic Level Enhancement Mode MOSFET

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	Steady-State	$R_{\theta JC}$		4.4	°C / W
Junction-to-Ambient[2]	Steady-State	$R_{\theta JA}$		48	

[1]Pulse width limited by maximum junction temperature.

[2]The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A = 25°C. The value in any given application depends on the user's specific board design.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1	-1.7	-2.5	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±25V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -24V, V_{GS} = 0V			-100	
		V_{DS} = -20V, V_{GS} = 0V , T_J = 125 °C			-1	μA
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = -5V, V_{GS} = -10V	-150			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = -4.5V, I_D = -9A		13	19	mΩ
		V_{GS} = -10V, I_D = -12A		8.3	12	
Forward Transconductance[1]	g_{fs}	V_{DS} = -5V, I_D = -12A		31		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -15V, f = 1MHz		2830		pF
Output Capacitance	C_{oss}			400		
Reverse Transfer Capacitance	C_{rss}			395		
Gate Resistance	R_g	V_{GS} = 0V, V_{DS} = 0V, f = 1MHz		2.3		Ω
Total Gate Charge[2]	Q_g(V_{GS} =-10V)	V_{DS} = 0.5$V_{(BR)DSS}$, I_D = -12A		65		nC
	Q_g(V_{GS} =-4.5V)			34		
Gate-Source Charge[2]	Q_{gs}			9		
Gate-Drain Charge[2]	Q_{gd}			16		
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DS} = -15V, I_D ≅ -1A, V_{GS} = -10V, R_{GS} = 6Ω		10		nS
Rise Time[2]	t_r			16		
Turn-Off Delay Time[2]	$t_{d(off)}$			200		
Fall Time[2]	t_f			100		

UNIKC Semiconductor

RoHS Compliant

P1203EK

P-Channel Logic Level Enhancement Mode MOSFET

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_J = 25 °C)						
Continuous Current	I_S				-40	A
Forward Voltage[1]	V_{SD}	I_F = -12A, V_{GS} = 0V			-1.2	V
Reverse Recovery Time	t_{rr}	I_F = -12A, dI_F/dt = 100A / µS		22.7		nS
Reverse Recovery Charge	Q_{rr}			10		nC

[1]Pulse test : Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.

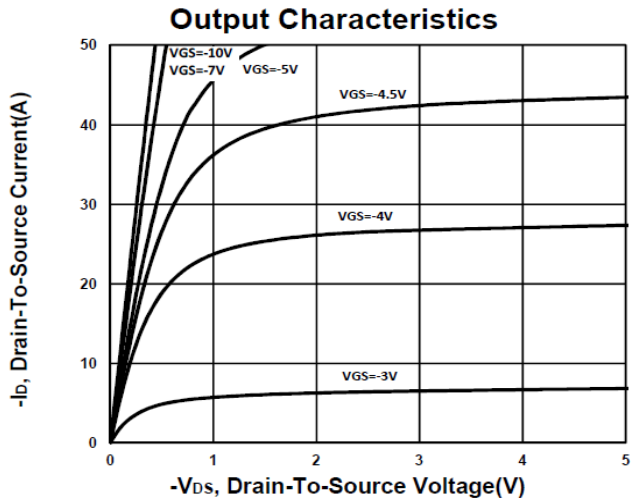
[2]Independent of operating temperature.

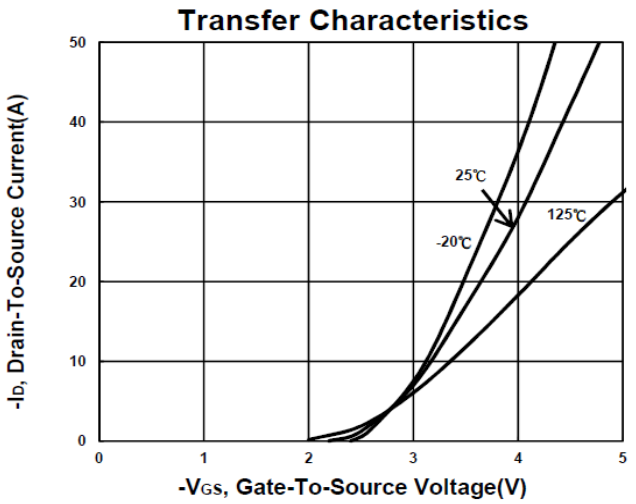
UNIKC Semiconductor

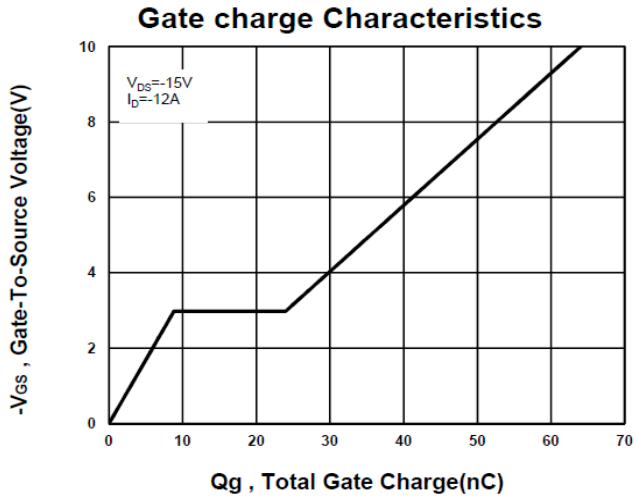
RoHS Compliant

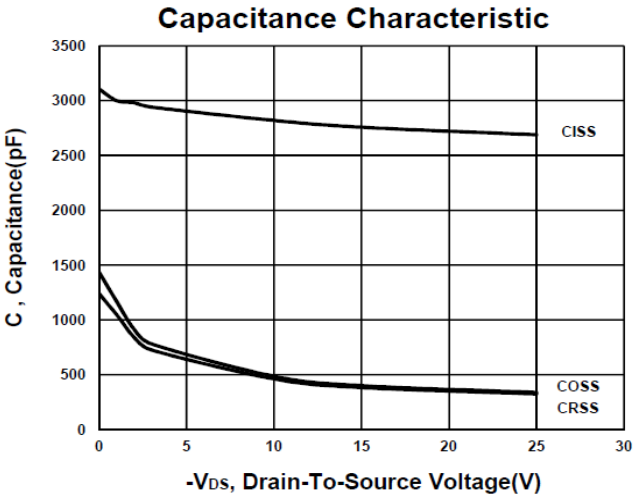
P1203EK

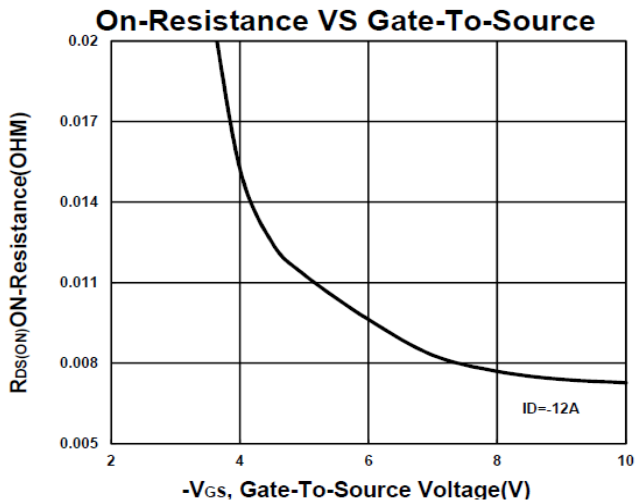
P-Channel Logic Level Enhancement Mode MOSFET

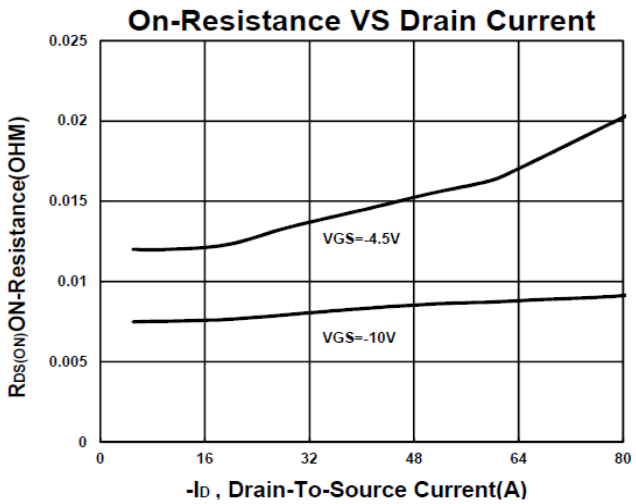












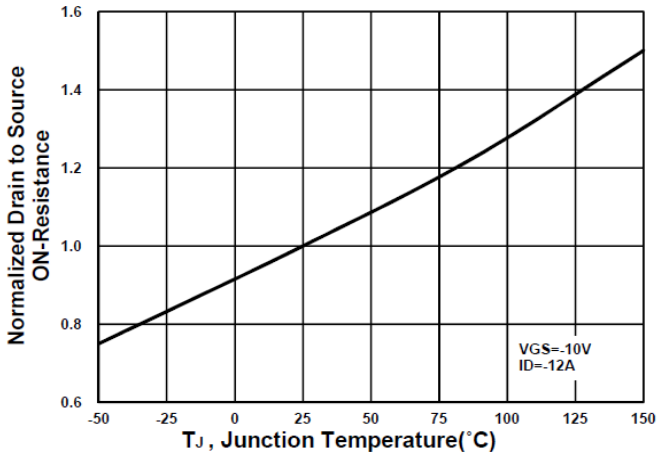
UNIKC Semiconductor

RoHS Compliant

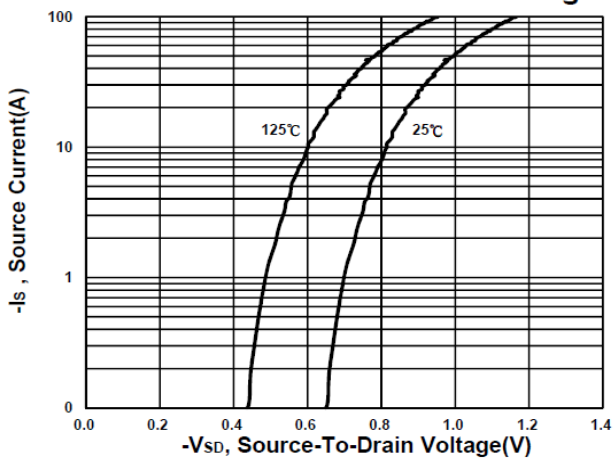
P1203EK

P-Channel Logic Level Enhancement Mode MOSFET

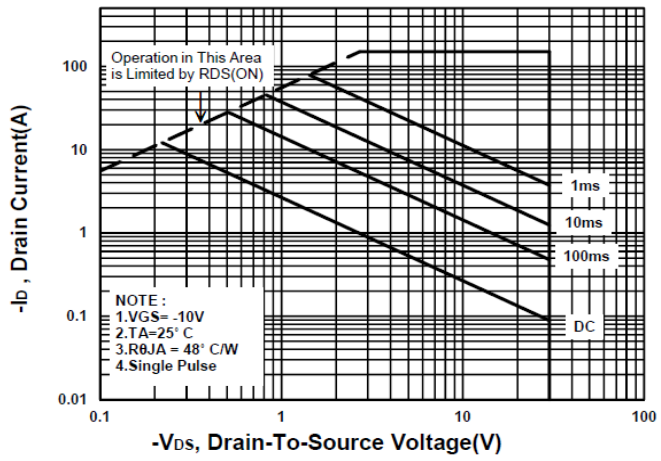
On-Resistance VS Temperature



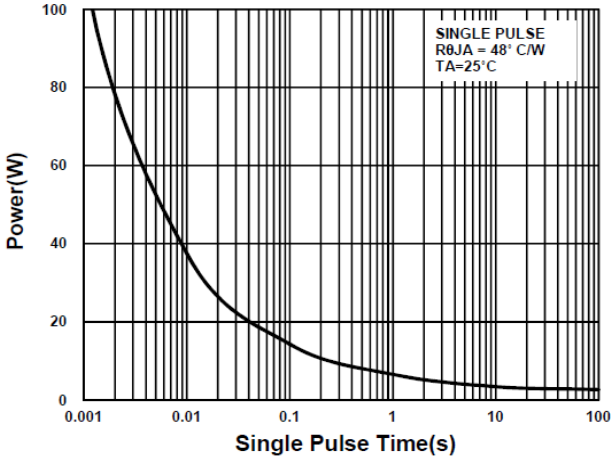
Source-Drain Diode Forward Voltage



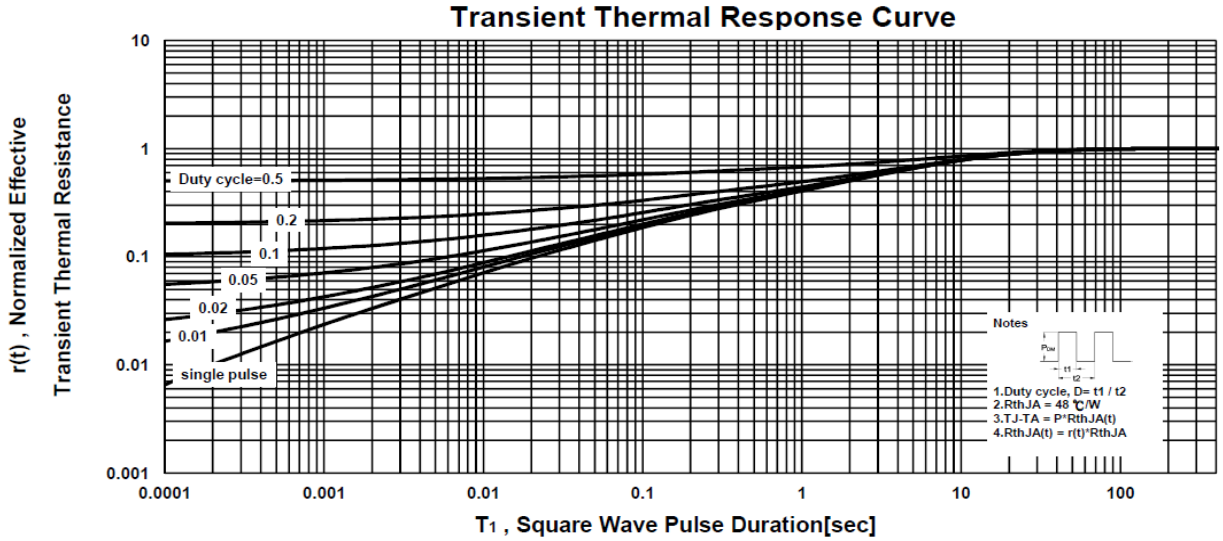
Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve



P1203EK

P-Channel Logic Level Enhancement Mode MOSFET

Package Dimension

PDFN 5x6P MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	4.8		5.15	J	3.33		3.78
B	5.44		5.9	K	0.9		
C	5.9		6.35	L	0.35		0.712
D	0.33		0.51	M	0°		12°
E		1.27		N	4.8		5.5
F	0.8		1.25	O	0.05		0.3
G	0.15		0.34	P	0.06		0.2
H	3.61		4.31	S	3.69		4.19
I	0.35		0.71