

# P12FE7R5SBK

## Power MOSFETs

75V, 12A, N-channel

### Feature

- N-channel
- SMD
- Low Ron
- 4.5V Gate Drive
- Low Capacitance
- Based on AEC-Q101
- Pb free terminal
- RoHS:Yes

### OUTLINE

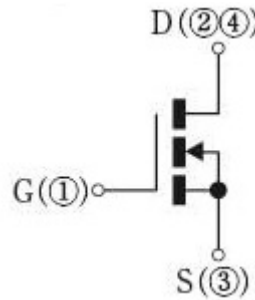
Package (House Name): FE

Package (JEDEC Code): TO-252AB similar

Package (JEITA Code): SC-63



### Equivalent circuit



### Absolute Maximum Ratings (unless otherwise specified : Tc=25°C)

Item	Symbol	Conditions	Ratings	Unit
Storage temperature	Tstg		-55 to 175	°C
Channel temperature	Tch		-55 to 175	°C
Drain-source voltage	V <sub>DSS</sub>		75	V
Gate-source voltage	V <sub>GSS</sub>		±20	V
Continuous drain current(DC)	I <sub>D</sub>		12	A
Continuous drain current(Peak)	I <sub>DP</sub>	Pulse width 10μs, duty=1/100	36	A
Total power dissipation	P <sub>T</sub>		24	W
Single avalanche current	I <sub>AS</sub>	Starting T <sub>ch</sub> =25°C T <sub>ch</sub> ≤150°C	12	A
Single avalanche energy	E <sub>AS</sub>	Starting T <sub>ch</sub> =25°C T <sub>ch</sub> ≤150°C	7.2	mJ

\* : See the original Specifications

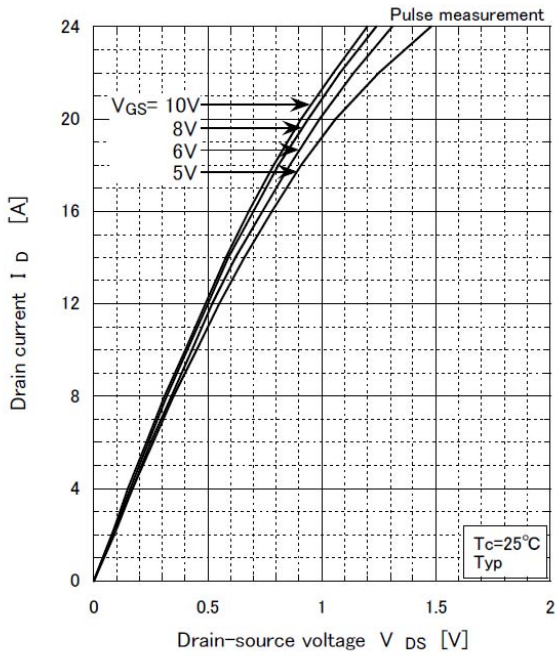
**Electrical Characteristics** (unless otherwise specified : Tc=25°C)

Item	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Drain-Source breakdown voltage	$V_{(BR)DSS}$	ID=1mA, VGS=0V	75			V
Zero gate voltage drain current	$I_{DSS}$	VDS=75V, VGS=0V			1	μA
Gate-source leakage current	$I_{GSS}$	VGS=±20V, VDS=0V			±10	μA
Forward transconductance	$g_{fs}$	ID=6A, VDS=10V	5			S
Static drain-source on-state resistance	$R_{DS(ON)}$	ID=6A, VGS=10V		0.04	0.05	Ω
Static drain-source on-state resistance	$R_{DS(ON)}$	ID=6A, VGS=4.5V		0.047	0.063	Ω
Gate threshold voltage	$V_{th}$	ID=1mA, VDS=10V	1.5	2	2.5	V
Source-drain diode forward voltage	$V_{SD}$	IS=12A, VGS=0V			1.5	V
Thermal resistance	$R_{th(j-c)}$	Junction to case, with heatsink ※			6.2	°C/W
Total gate charge	$Q_g$	VDD=60V, VGS=10V, ID=12A		16.6		nC
Gate to source charge	$Q_{gs}$	VDD=60V, VGS=10V, ID=12A		4.2		nC
Gate to drain charge	$Q_{gd}$	VDD=60V, VGS=10V, ID=12A		3.9		nC
Input capacitance	$C_{iss}$	VDS=25V, VGS=0V, f=1MHz		660		pF
Reverse transfer capacitance	$C_{rss}$	VDS=25V, VGS=0V, f=1MHz		32		pF
Output capacitance	$C_{oss}$	VDS=25V, VGS=0V, f=1MHz		77		pF
Turn-on delay time	$t_{d(on)}$	ID=6A, RL=6.25Ω, VDD=37.5V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		4.5		ns
Rise time	$t_r$	ID=6A, RL=6.25Ω, VDD=37.5V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		7		ns
Turn-off delay time	$t_{d(off)}$	ID=6A, RL=6.25Ω, VDD=37.5V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		14		ns
Fall time	$t_f$	ID=6A, RL=6.25Ω, VDD=37.5V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		4		ns
Diode reverse recovery time	$t_{rr}$	IF=12A, VGS=0V, di/dt=100A/μs		44		ns
Diode reverse recovery charge	$Q_{rr}$	IF=12A, VGS=0V, di/dt=100A/μs		54		nC

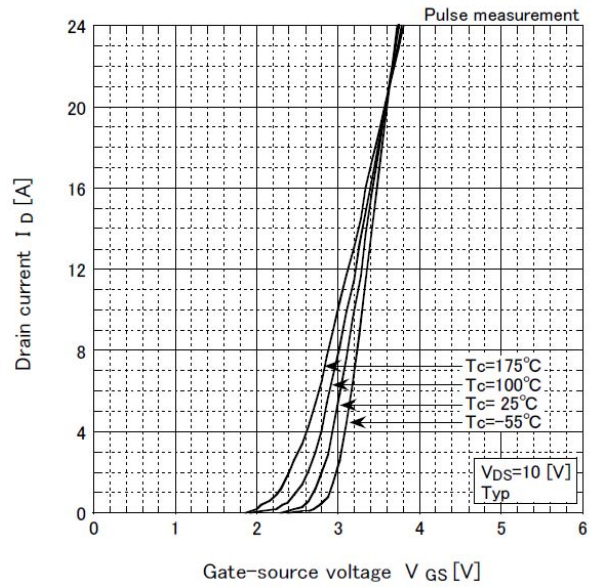
※ : See the original Specifications

# CHARACTERISTIC DIAGRAMS

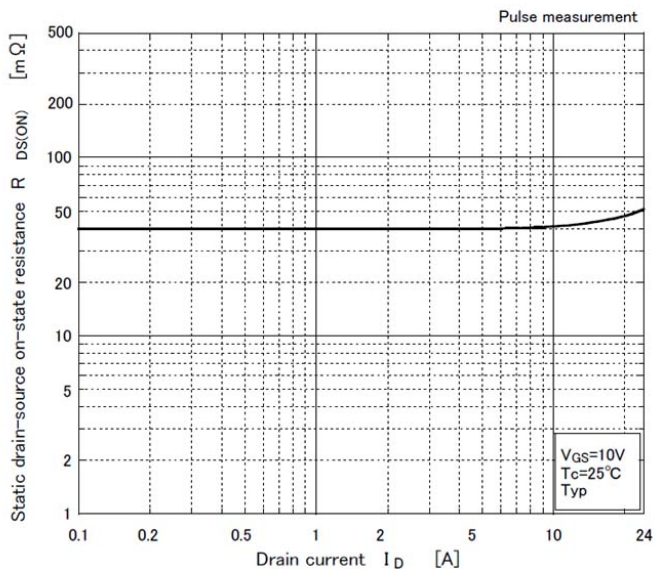
Typical output characteristics



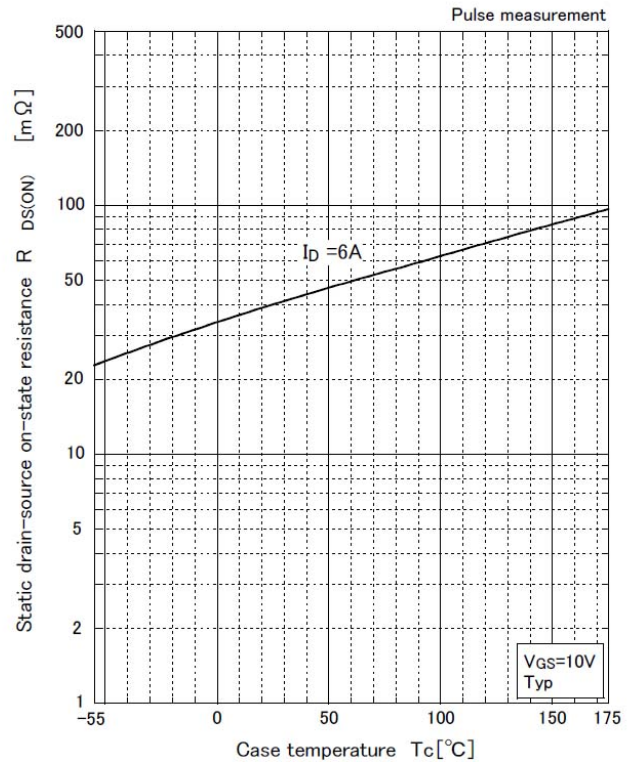
Transfer characteristics

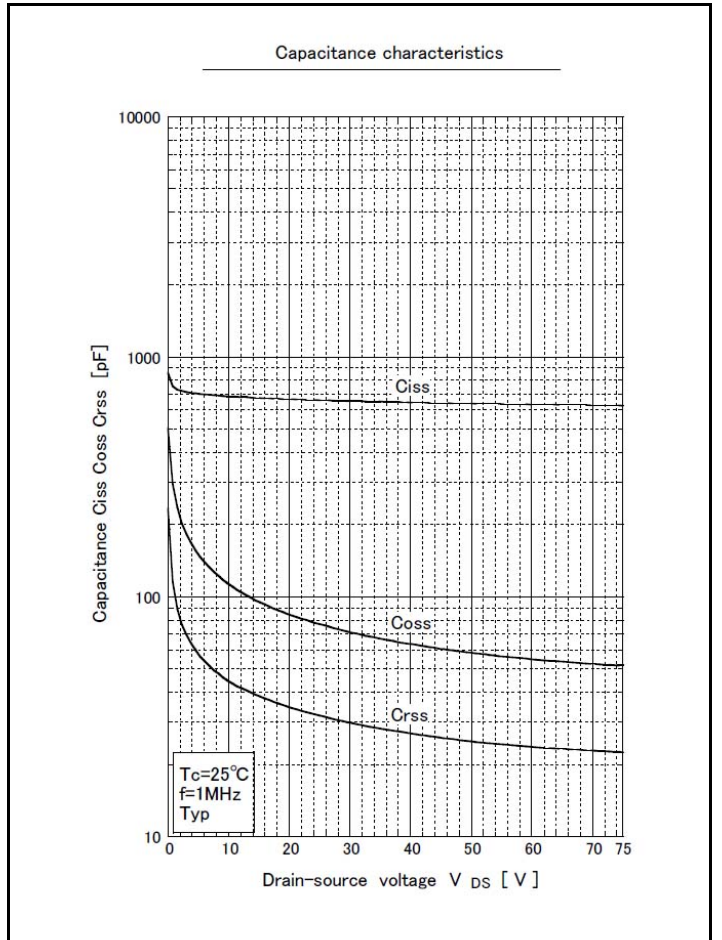
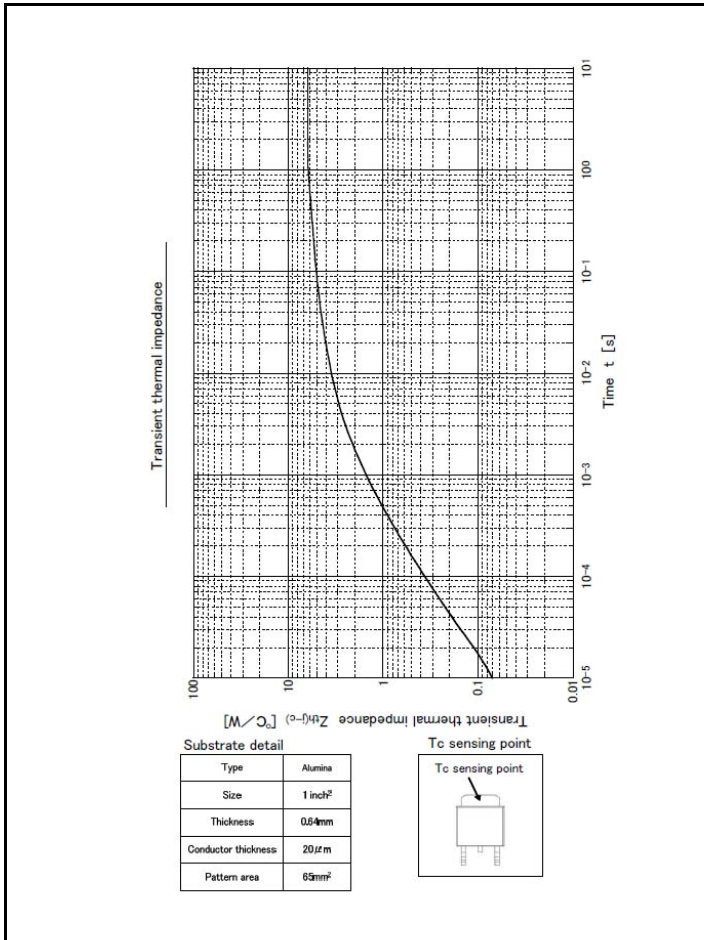
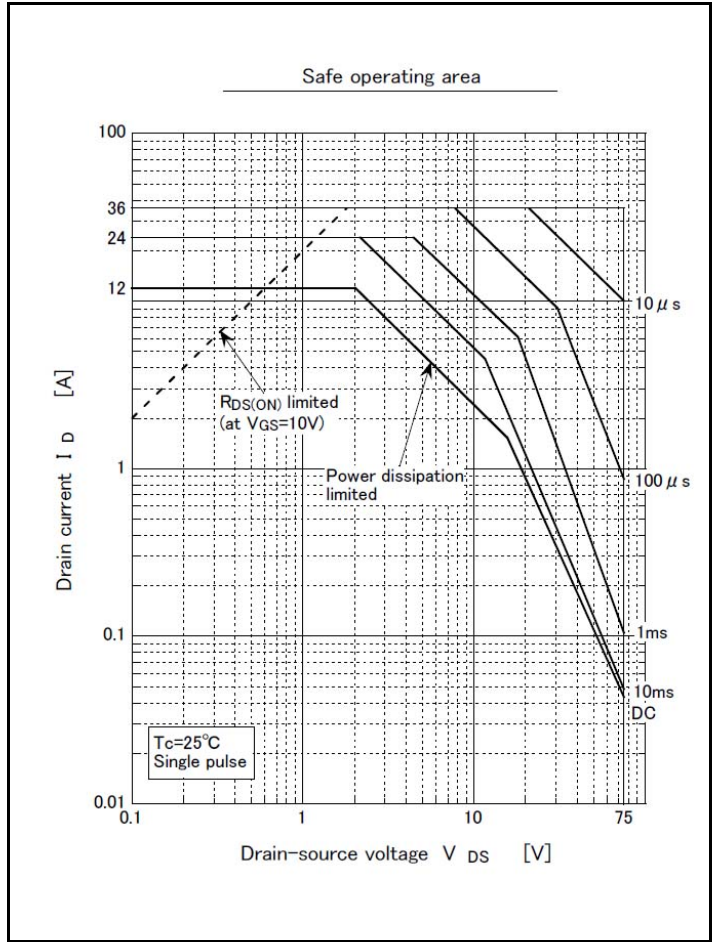
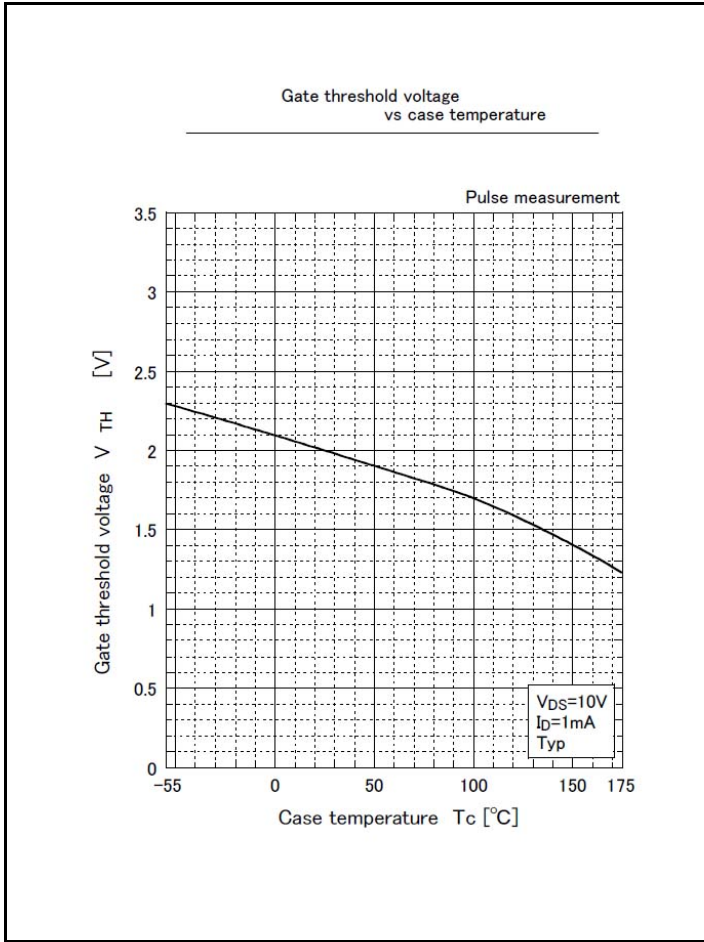


Static drain-source on-state resistance vs drain current

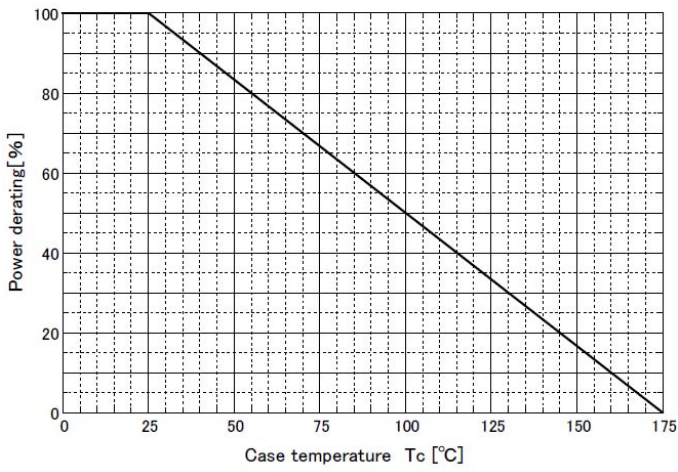


Static drain-source on-state resistance vs case temperature

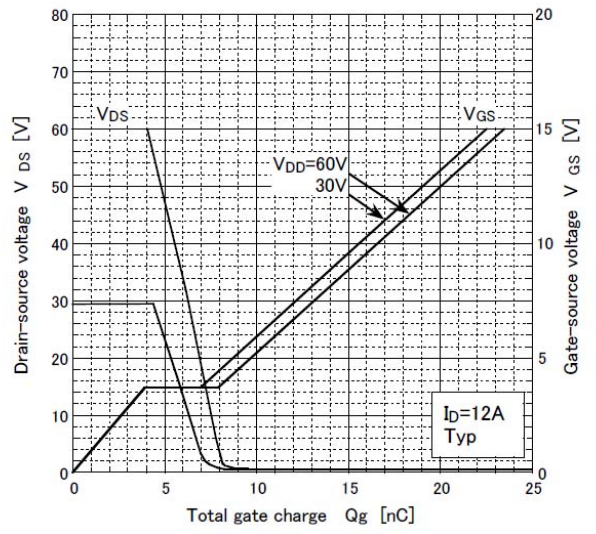




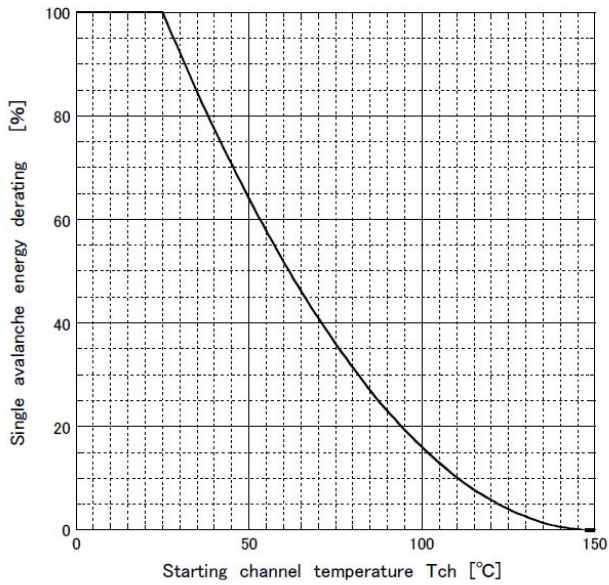
Power derating - case temperature



Gate charge characteristics

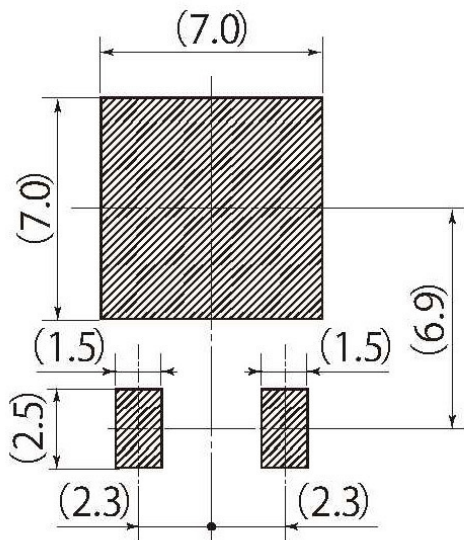
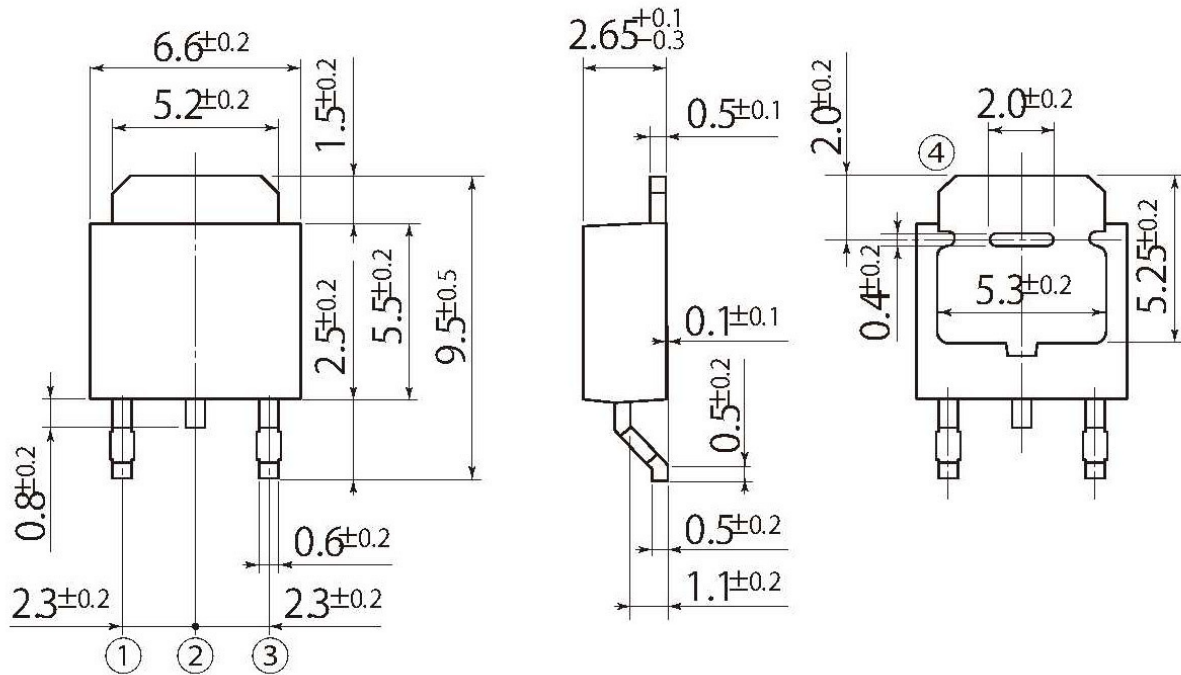


Single avalanche energy derating vs channel temperature



G3

JEDEC Code	TO-252AB similar
JEITA Code	SC-63
House Name	FE



Referential Soldering Pad

• Optimize soldering pad to the board design and soldering condition.

## Notes

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