ShinDengen

P12LF10SLKD

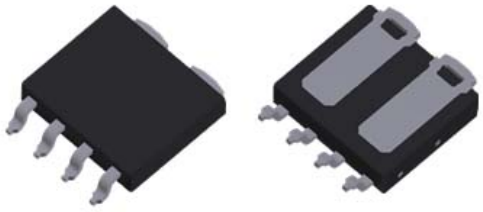
Power MOSFETs
100V, 12A, Dual N-channel

Feature

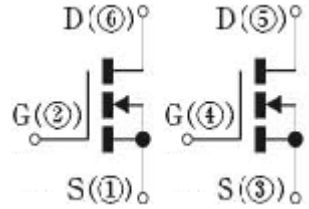
- N-channel
- Small SMD
- Dual type
- 4.5V Gate Drive
- Based on AEC-Q101
- Halogen free
- Pb free terminal
- RoHS:Yes

OUTLINE

Package (House Name): LF_Dual



Equivalent circuit



Absolute Maximum Ratings (unless otherwise specified : Tc=25℃)

Item	Symbol	Conditions	Ratings	Unit
Storage temperature	Tstg		-55 to 175	℃
Channel tempertature	Tch		-55 to 175	℃
Drain-source voltage	V_{DSS}		100	V
Gate-source voltage	V_{GSS}		±20	V
Continuous drain current(DC)	I_D		12	A
Continuous drain current(Peak)	I_{DP}	Pulse width 10μs, duty=1/100	36	A
Total power dissipation	P_T		50	W
Single avalanche current	I_{AS}	Starting Tch=25℃ Tch≦150℃	12	A
Single avalanche energy	E_{AS}	Starting Tch=25℃ Tch≦150℃	16	mJ

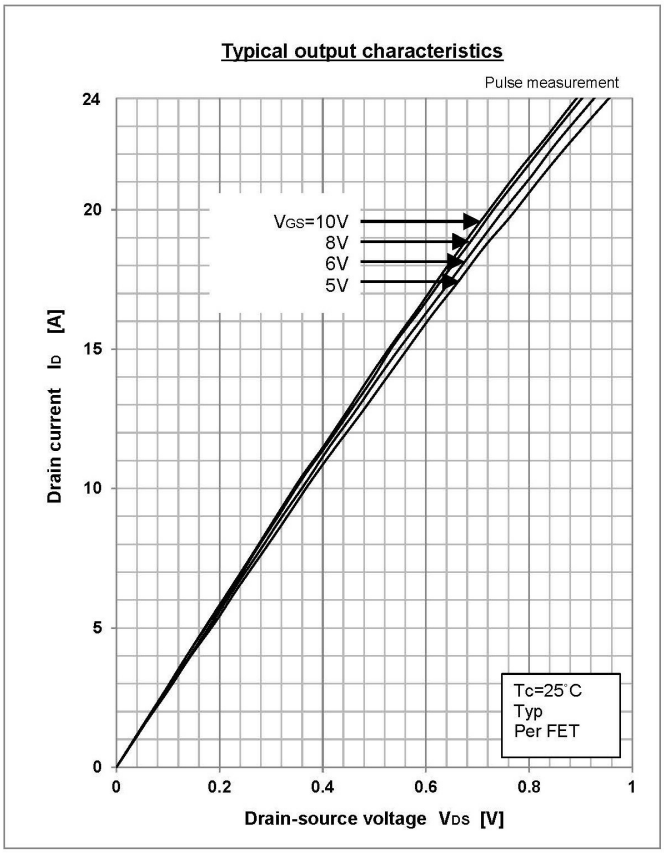
※ ：See the original Specifications

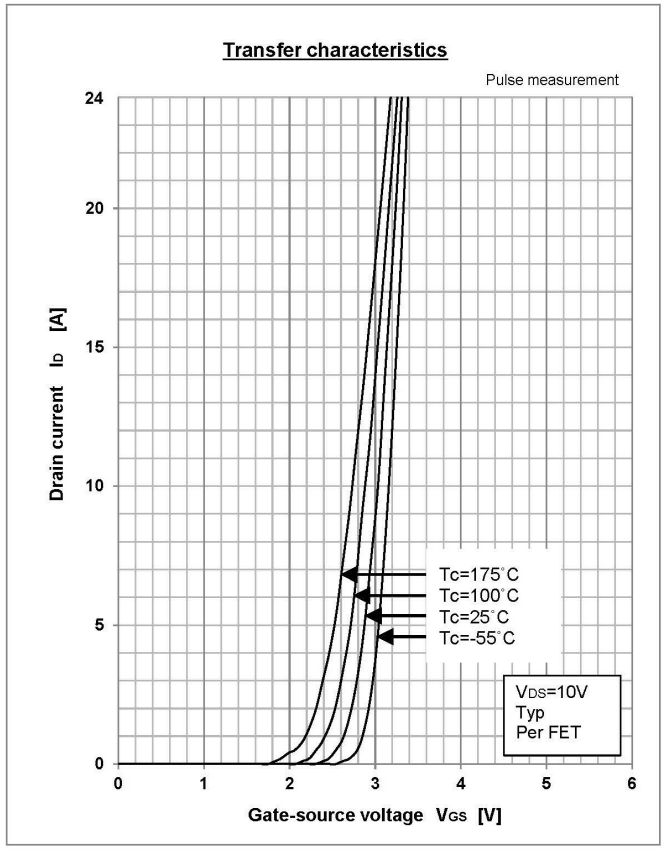
Electrical Characteristics (unless otherwise specified : Tc=25℃)

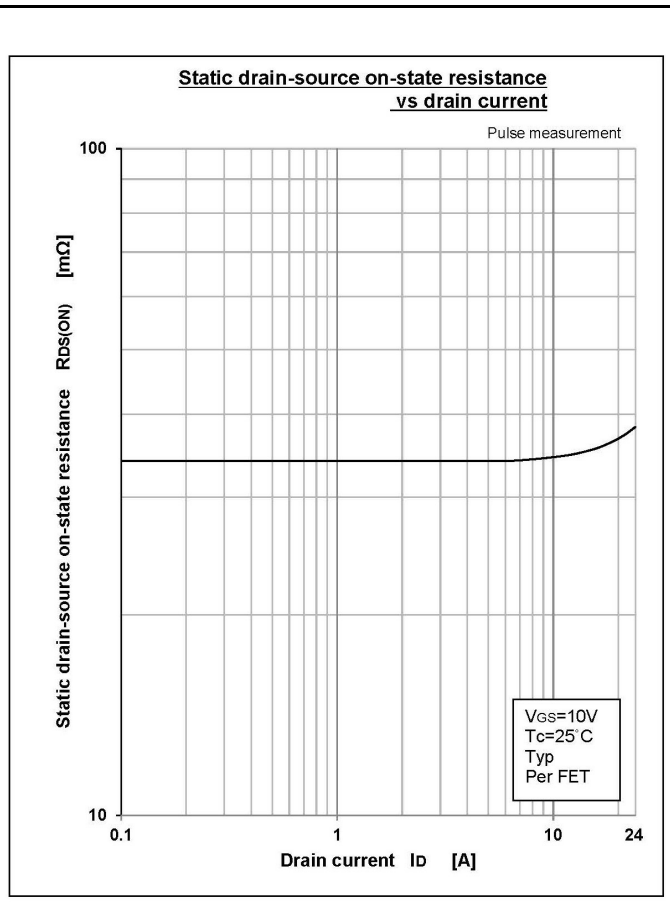
Item	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Drain-Source breakdown voltage	$V_{(BR)DSS}$	ID=1mA, VGS=0V	100			V
Zero gate voltage drain current	I_{DSS}	VDS=100V, VGS=0V			1	μA
Gate-source leakage current	I_{GSS}	VGS=±20V, VDS=0V			±0.1	μA
Forward transconductance	g_{fs}	ID=6A, VDS=10V	7			S
Static drain-source on-state resistance	$R_{DS(ON)}$	ID=6A, VGS=10V		0.034	0.042	Ω
Static drain-source on-state resistance	$R_{DS(ON)}$	ID=6A, VGS=4.5V		0.037	0.049	Ω
Gate threshold voltage	Vth	ID=1mA, VDS=10V	1.5	2	2.5	V
Source-drain diode forward voltage	V_{SD}	IS=12A, VGS=0V			1.5	V
Thermal resistance	Rth(j-c)	Junction to case			2.98	℃/W
Total gate charge	Qg	VDD=80V, VGS=10V, ID=12A		32		nC
Gate to source charge	Qgs	VDD=80V, VGS=10V, ID=12A		6.3		nC
Gate to drain charge	Qgd	VDD=80V, VGS=10V, ID=12A		8		nC
Input capacitance	Ciss	VDS=25V, VGS=0V, f=1MHz		1420		pF
Reverce transfer capacitnce	Crss	VDS=25V, VGS=0V, f=1MHz		53		pF
Output capacitance	Coss	VDS=25V, VGS=0V, f=1MHz		110		pF
Turn-on delay time	td(on)	ID=6A, RL=8.33Ω, VDD=50V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		8.5		ns
Rise time	tr	ID=6A, RL=8.33Ω, VDD=50V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		19		ns
Turn-off delay time	td(off)	ID=6A, RL=8.33Ω, VDD=50V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		24		ns
Fall time	tf	ID=6A, RL=8.33Ω, VDD=50V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		4.5		ns
Diode reverse recovery time	trr	IF=12A, VGS=0V, di/dt=100A/μs		52		ns
Diode reverse recovery charge	Qrr	IF=12A, VGS=0V, di/dt=100A/μs		90		nC

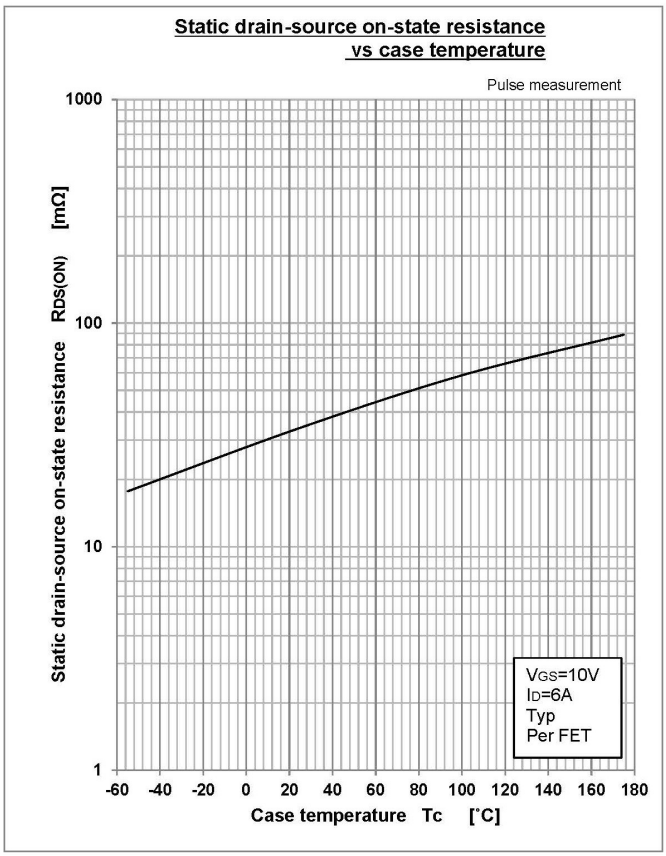
※ ：See the original Specifications

CHARACTERISTIC DIAGRAMS

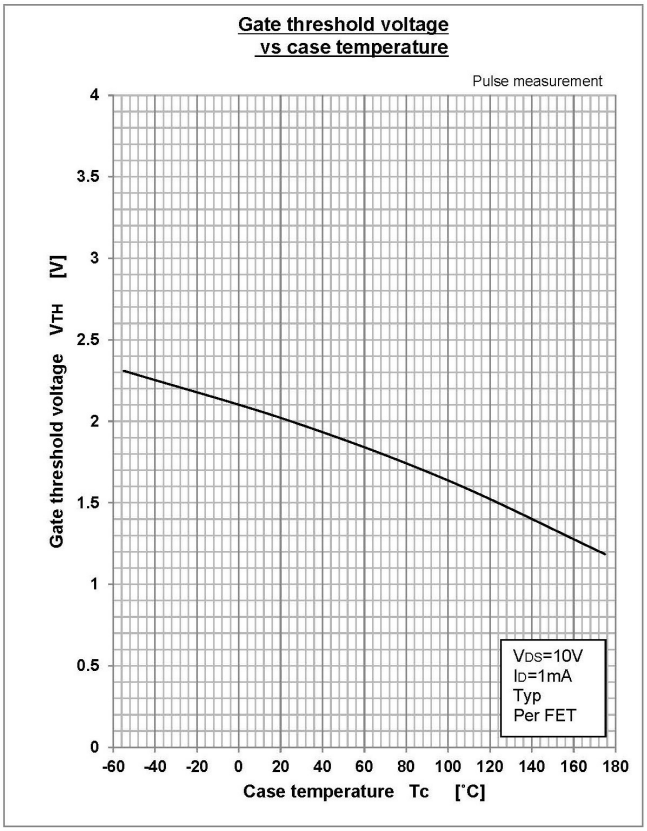




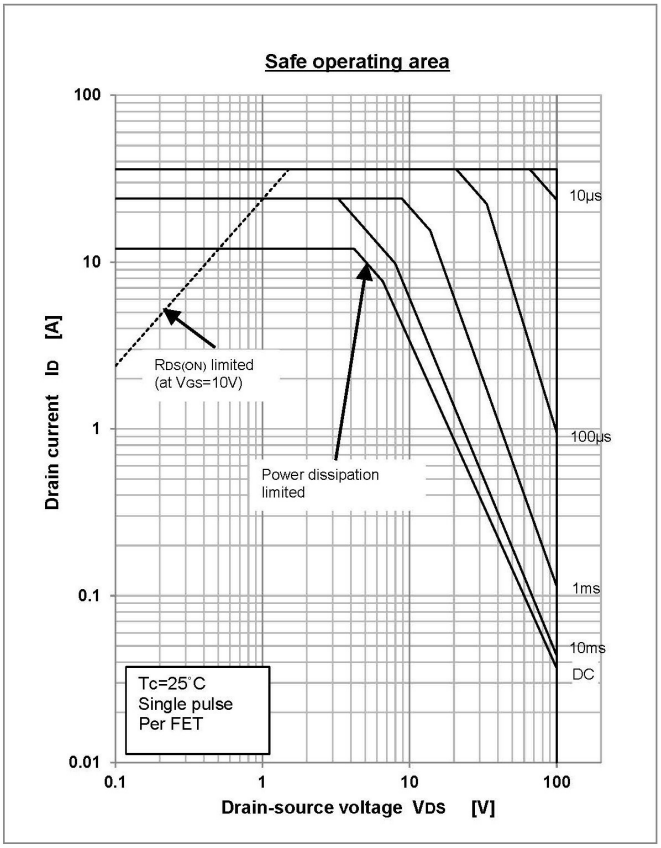


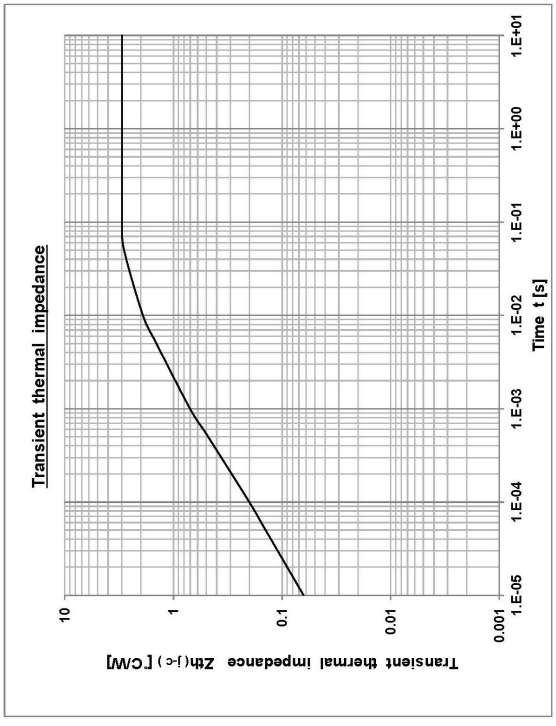


Gate threshold voltage vs case temperature

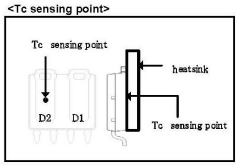


Safe operating area



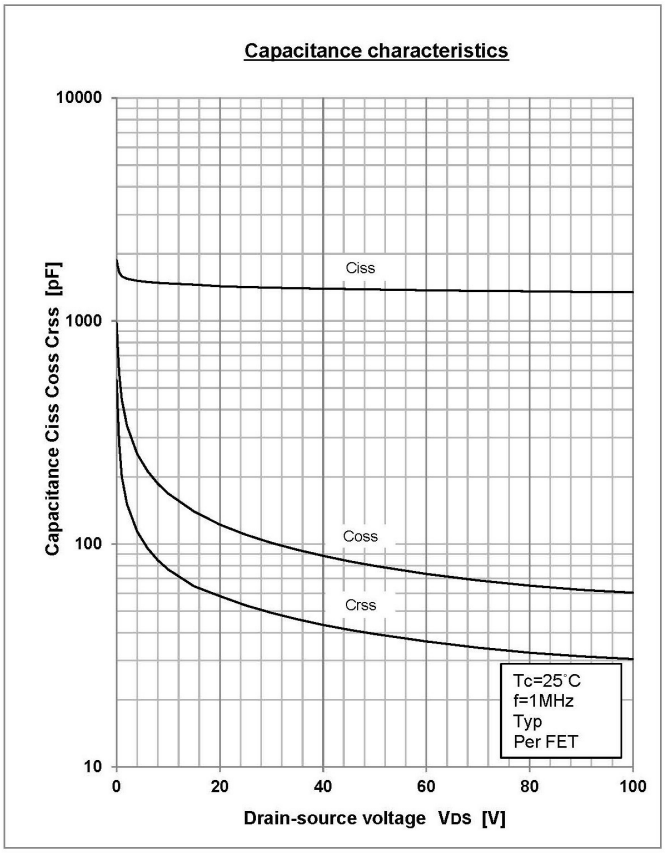


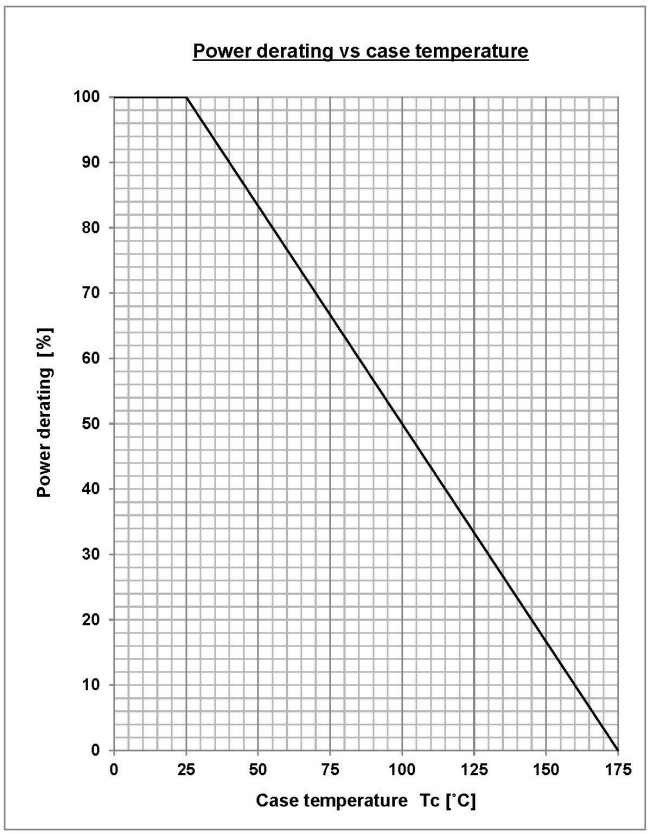
<Tc sensing point>

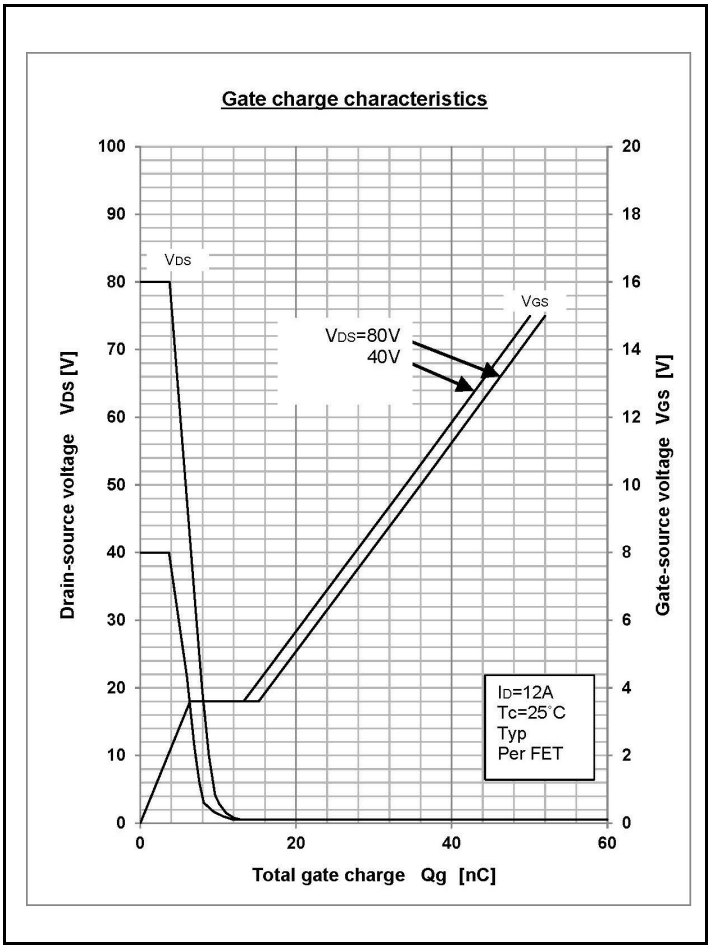


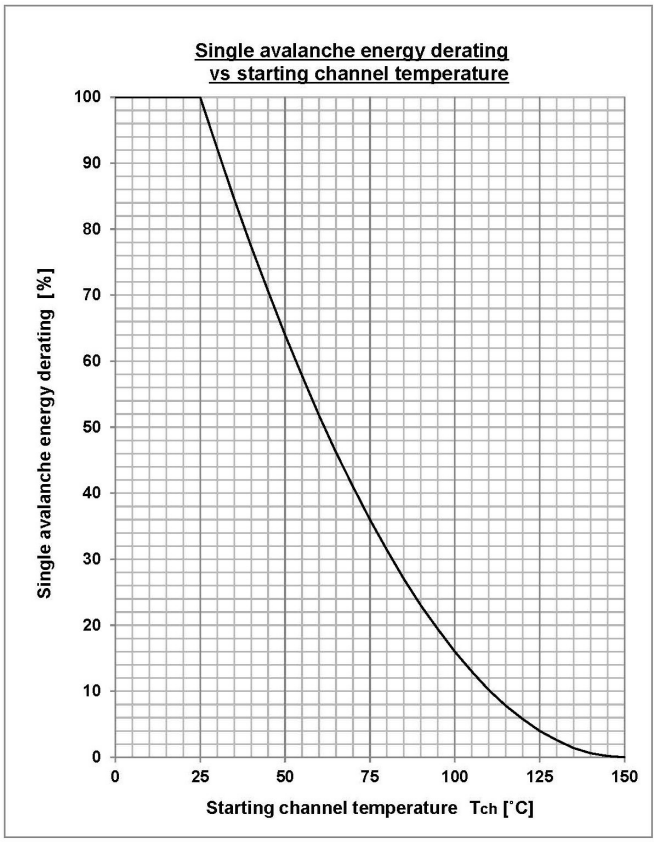
Specification No.

Capacitance characteristics




Power derating vs case temperature
Power derating [%]
Case temperature Tc [°C]
0
10
20
30
40
50
60
70
80
90
100
0
25
50
75
100
125
150
175


Gate charge characteristics
Drain-source voltage VDS [V]
Gate-source voltage VGS [V]
Total gate charge Qg [nC]
VDS
VGS
VDS=80V
40V
ID=12A
Tc=25°C
Typ
Per FET
0
10
20
30
40
50
60
70
80
90
100
0
2
4
6
8
10
12
14
16
18
20
0
20
40
60

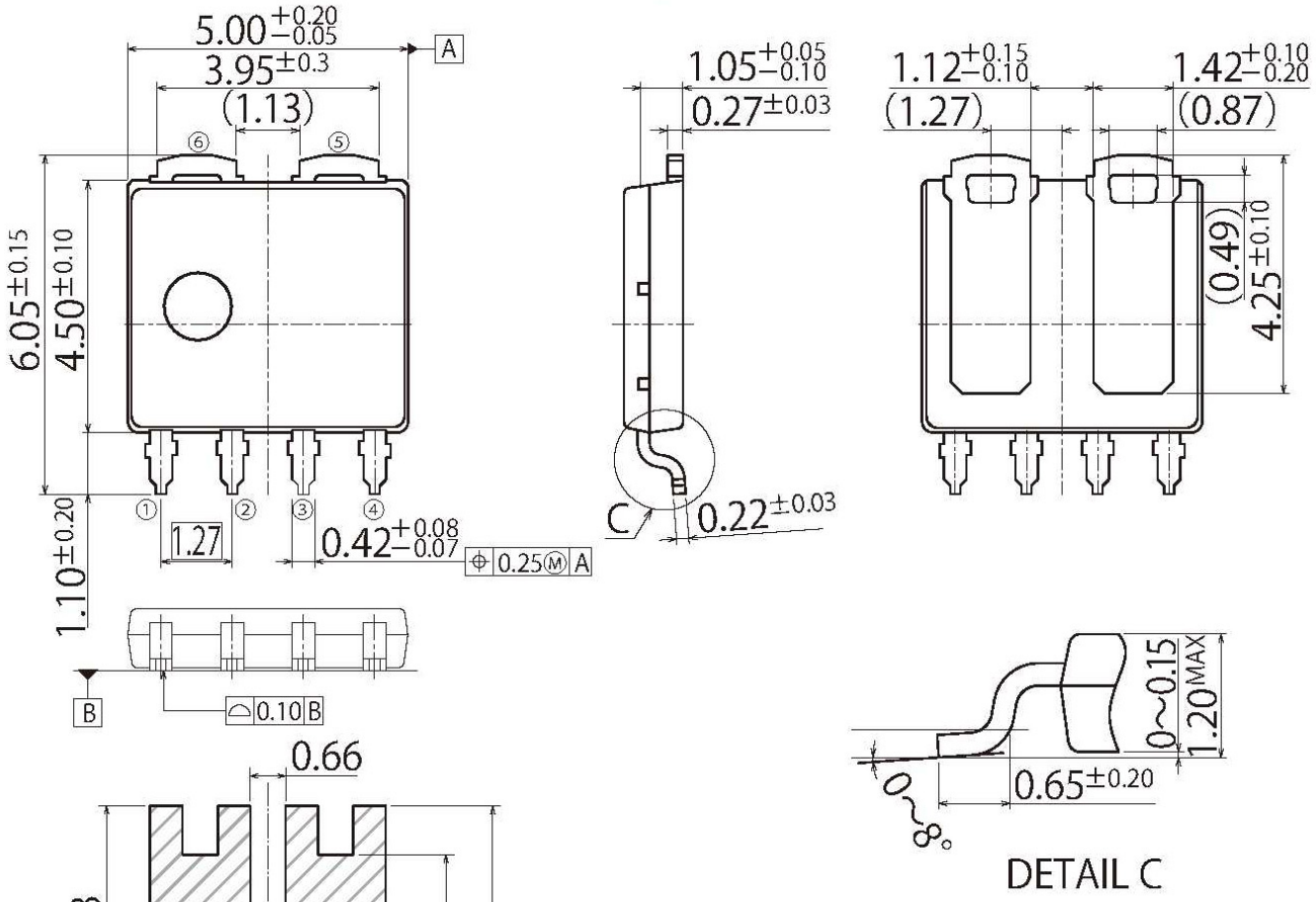

Single avalanche energy derating
vs starting channel temperature
Single avalanche energy derating [%]
Starting channel temperature Tch [°C]
0
10
20
30
40
50
60
70
80
90
100
0
25
50
75
100
125
150

Outline Dimensions

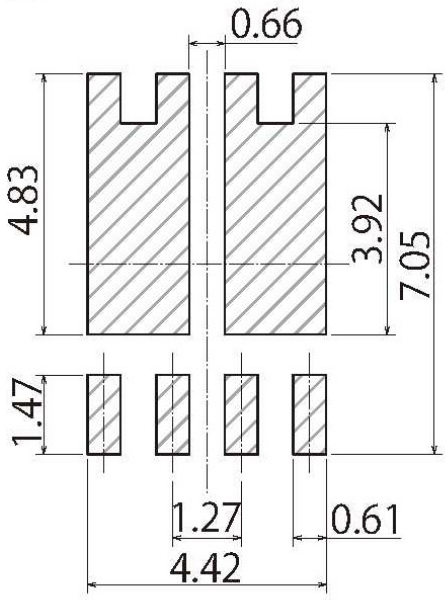
unit:mm

G8

JEDEC Code	–
JEITA Code	–
House Name	LF_Dual



DETAIL C



Referential Soldering Pad

Notes

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