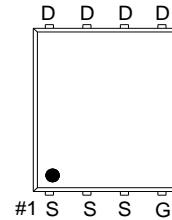
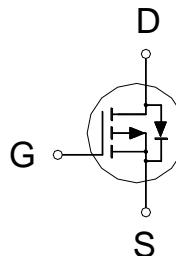


NIKO-SEM**P-Channel Logic Level Enhancement Mode
Field Effect Transistor****P1306EK**
PDFN 5x6P
Halogen-Free & Lead-Free**PRODUCT SUMMARY**

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
-60V	13.5mΩ	-43A

G. GATE
D. DRAIN
S. SOURCE100% UIS Tested
100% Rg Tested**ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ Unless Otherwise Noted)**

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	± 25	V
Continuous Drain Current	I_D	-43	A
		-27	
		-10	
		-8.3	
Pulsed Drain Current ¹	I_{DM}	-149	
Avalanche Current	I_{AS}	-52	
Avalanche Energy	E_{AS}	135	mJ
Power Dissipation ³	P_D	48	W
		19	
		2.7	
		1.7	
Operating Junction & Storage Temperature Range	T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient ²	$t \leq 10s$	$R_{\theta JA}$	45	75	°C / W
Junction-to-Ambient ²	Steady-State	$R_{\theta JA}$			
Junction-to-Case	Steady-State	$R_{\theta JC}$		2.6	

¹Pulse width limited by maximum junction temperature.²The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ C$. The value in any given application depends on the user's specific board design.³The Power dissipation is based on $R_{\theta JA}$ $t \leq 10s$ value.

NIKO-SEM**P-Channel Logic Level Enhancement Mode
Field Effect Transistor****P1306EK
PDFN 5x6P
Halogen-Free & Lead-Free****ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, Unless Otherwise Noted)**

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = -250\mu\text{A}$	-60			V
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}, I_D = -250\mu\text{A}$	-1.3	-1.8	-2.3	
Gate-Body Leakage	I_{GSS}	$V_{\text{DS}} = 0\text{V}, V_{\text{GS}} = \pm 25\text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = -60\text{V}, V_{\text{GS}} = 0\text{V}$			-1	
		$V_{\text{DS}} = -60\text{V}, V_{\text{GS}} = 0\text{V}, T_J = 55^\circ\text{C}$			-10	uA
Drain-Source On-State Resistance ¹	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}} = -10\text{V}, I_D = -20\text{A}$		11	13.5	
		$V_{\text{GS}} = -4.5\text{V}, I_D = -15\text{A}$		15	17.5	mΩ
Forward Transconductance ¹	g_{fs}	$V_{\text{DS}} = -5\text{V}, I_D = -20\text{A}$		55		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = -30\text{V}, f = 1\text{MHz}$		3963		pF
Output Capacitance	C_{oss}			368		
Reverse Transfer Capacitance	C_{rss}			266		
Gate Resistance	R_g	$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 0\text{V}, f = 1\text{MHz}$		2.9		Ω
Total Gate Charge ²	Q_g	$V_{\text{DS}} = -20\text{V}, V_{\text{GS}} = -10\text{V}, I_D = -20\text{A}$		84		nC
Gate-Source Charge ²	Q_{gs}			12		
Gate-Drain Charge ²	Q_{gd}			20.5		
Turn-On Delay Time ²	$t_{\text{d}(\text{on})}$	$V_{\text{DS}} = -20\text{V}, I_D \approx -20\text{A}, V_{\text{GS}} = -10\text{V}, R_{\text{GS}} = 6\Omega$		15		nS
Rise Time ²	t_r			69		
Turn-Off Delay Time ²	$t_{\text{d}(\text{off})}$			117		
Fall Time ²	t_f			112		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_J = 25^\circ\text{C}$)						
Continuous Current	I_S				-40	A
Forward Voltage ¹	V_{SD}	$I_F = -20\text{A}, V_{\text{GS}} = 0\text{V}$			-1.2	V
Reverse Recovery Time	t_{rr}	$I_F = -20\text{A}, dI_F/dt = 100 \text{ A} / \mu\text{s}$		20		nS
Reverse Recovery Charge	Q_{rr}			15.5		nC

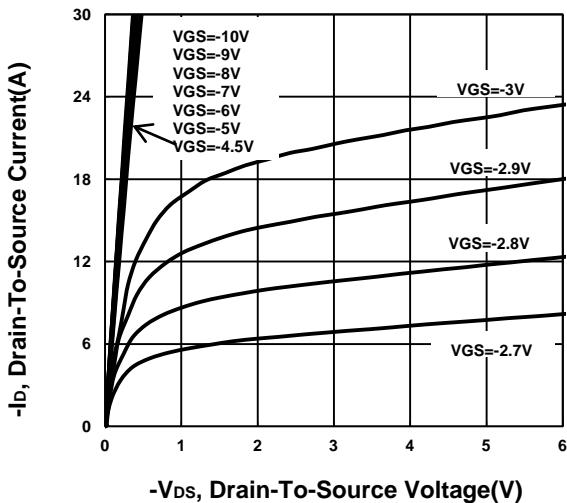
¹Pulse test : Pulse Width $\leq 300 \mu\text{sec}$, Duty Cycle $\leq 2\%$.²Independent of operating temperature.

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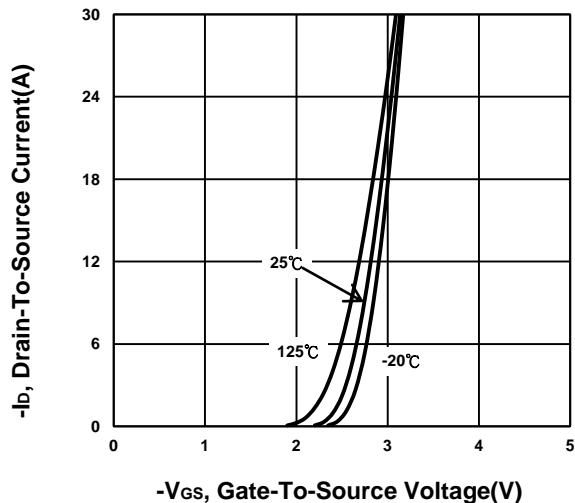
**P-Channel Logic Level Enhancement Mode
Field Effect Transistor**

P1306EK
PDFN 5x6P
Halogen-Free & Lead-Free

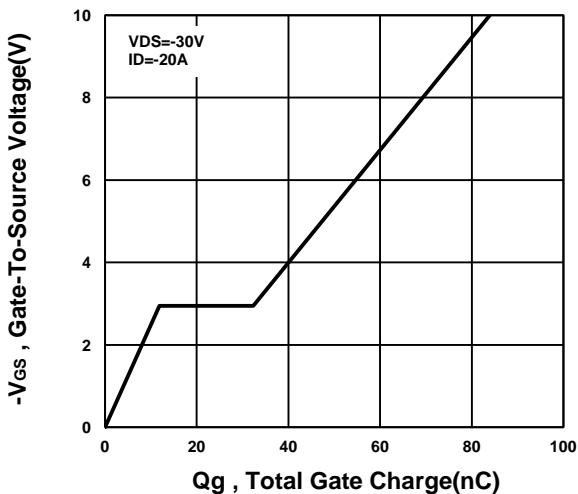
Output Characteristics



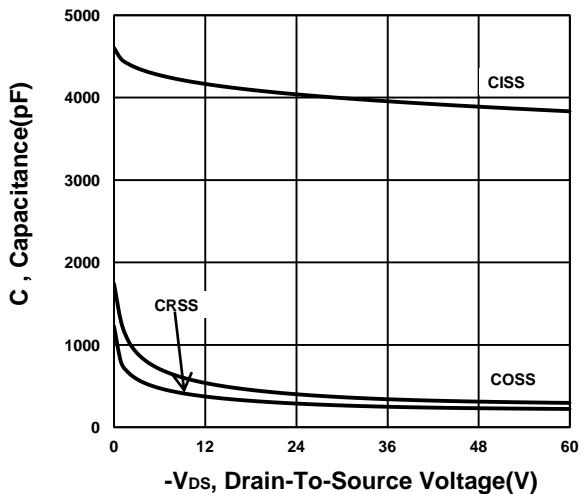
Transfer Characteristics



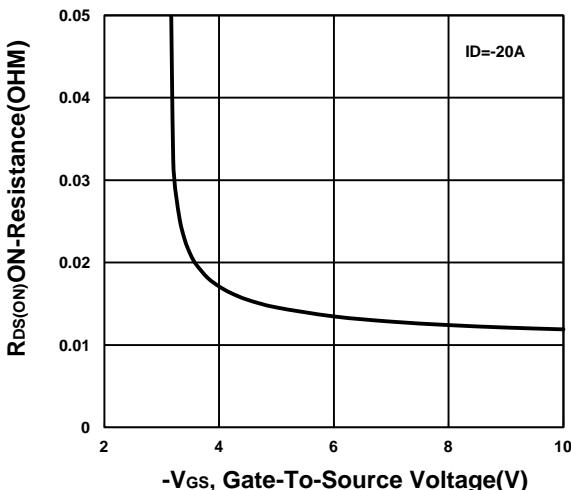
Gate charge Characteristics



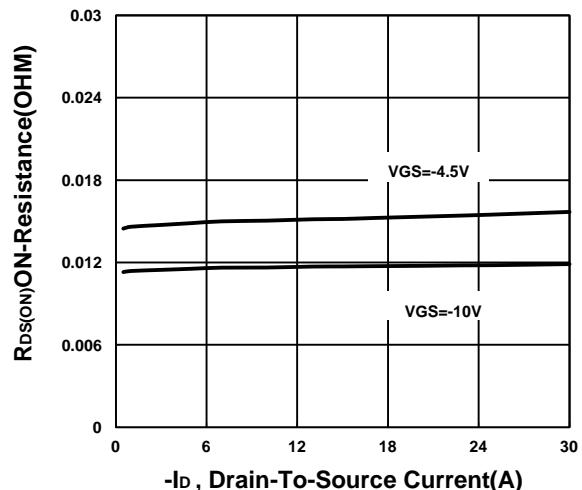
Capacitance Characteristic

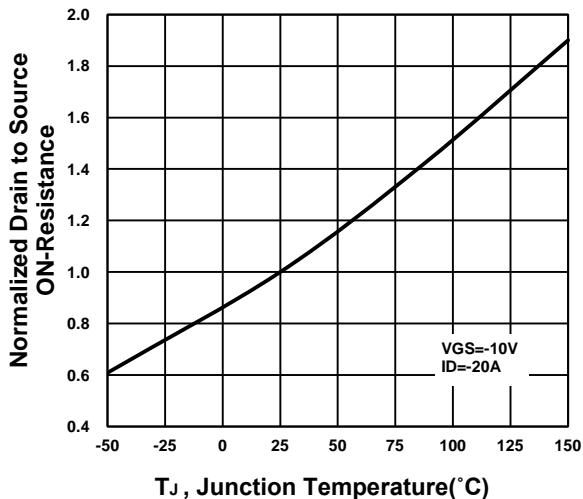
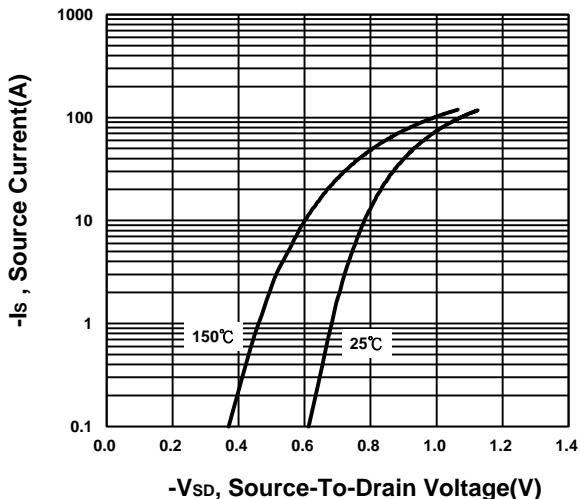
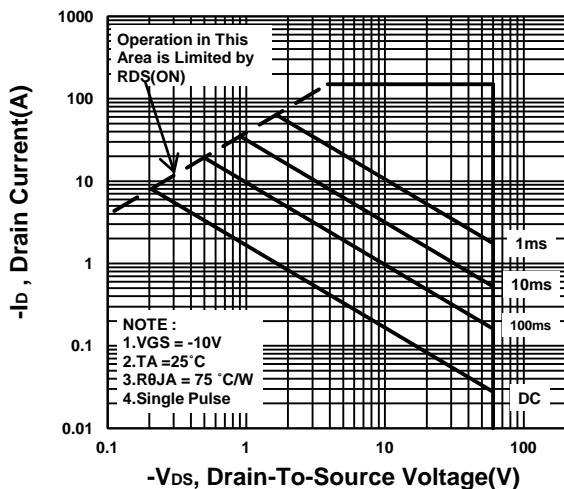
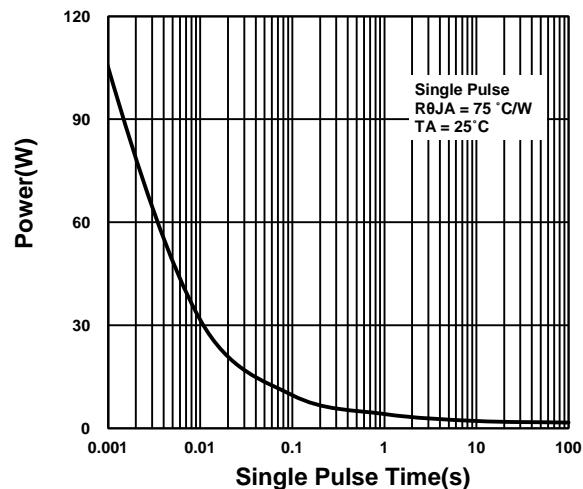
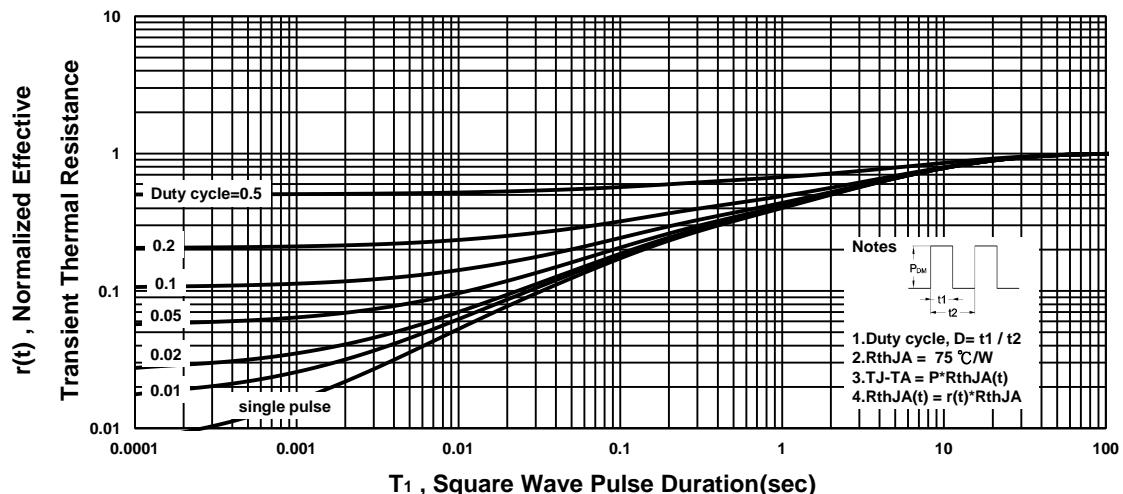


On-Resistance VS Gate-To-Source Voltage



On-Resistance VS Drain Current



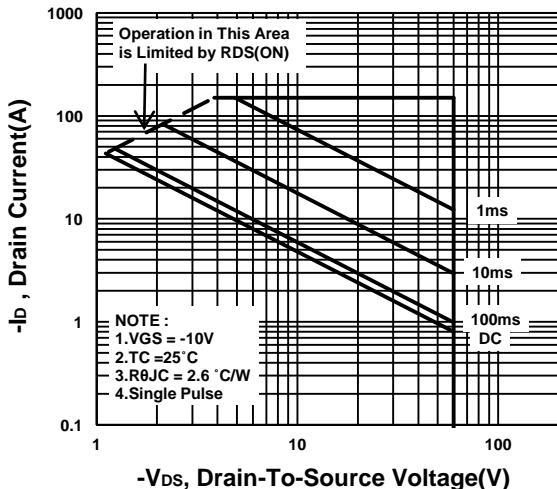
NIKO-SEM**P-Channel Logic Level Enhancement Mode
Field Effect Transistor****P1306EK
PDFN 5x6P
Halogen-Free & Lead-Free****On-Resistance VS Temperature****Source-Drain Diode Forward Voltage****Safe Operating Area****Single Pulse Maximum Power Dissipation****Transient Thermal Response Curve**

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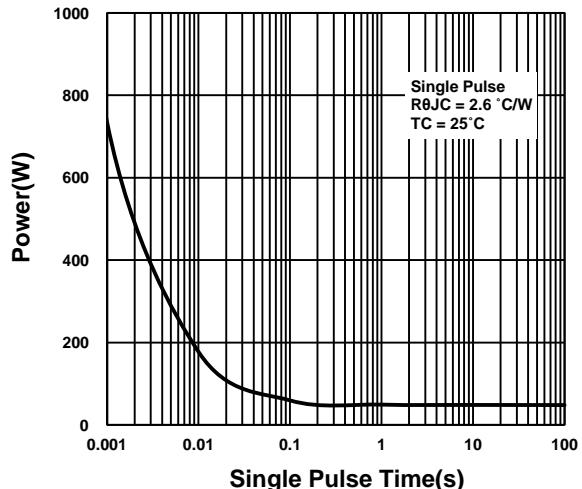
**P-Channel Logic Level Enhancement Mode
Field Effect Transistor**

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Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve

