Product Information

To:

Product Name: P140NWR1 R0

Document Issue Date: 2010/04/20

Note: 1. Please contact IVO Corp. before designing your product based on this product.
2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by IVO for any intellectual property claims or other problems that may result from application based on the module described herein.

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Revision	Date	Page	Old Description	New Description	Remark
00	2010/04/08	-	-	First issued	-
01	2010/04/20	6	Operation humidity max 80%	Operation humidity max 90%	
		8	Wx, Wy ±0.05	Wx, Wy ±0.03	

Contents

1.0 General Descriptions

1.1 Introduction

The P140NWR1 is a color active matrix thin film transistor (TFT) TN liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. It is composed of a TFT LCD panel, a timing controller, voltage reference, common voltage, column driver, and row driver circuit. This TFT LCD has a 14.0-inch diagonally measured active display area with resolution (1,366 horizontal by 768 vertical pixel array).

1.2 Features

- 14.0” TN TFT LCD Panel
- Supported (1,366x768 pixels) resolution
- Compatible with RoHS standard
- With Color Engine Function

1.3 Product Summary

Items	Specifications	Unit
Screen Diagonal	14.0	Inch
Active Area	309.399 (H) x 173.952 (V)	mm
Pixels H x V	1,366 x3(RGB) x 768	
Pixel Pitch	0.2265×0.2265	mm
Pixel Arrangement	R.G.B. Vertical Stripe	
Display Mode	Normally White (TN)	
Contrast Ratio	500 (Typ.)	
Response Time	8 (Typ.)	msec
Input Voltage	3.3 (Typ.)	V
Power Consumption	1.2 (Max.)	watt
Weight	173(Typ.)	g
Electrical Interface (Logic)	Single LVDS	
Support Color	262 K	
Optimum Viewing Direction	6 o’colok	
Surface Treatment	Glare+ HC	

1.4 Functional Block Diagram

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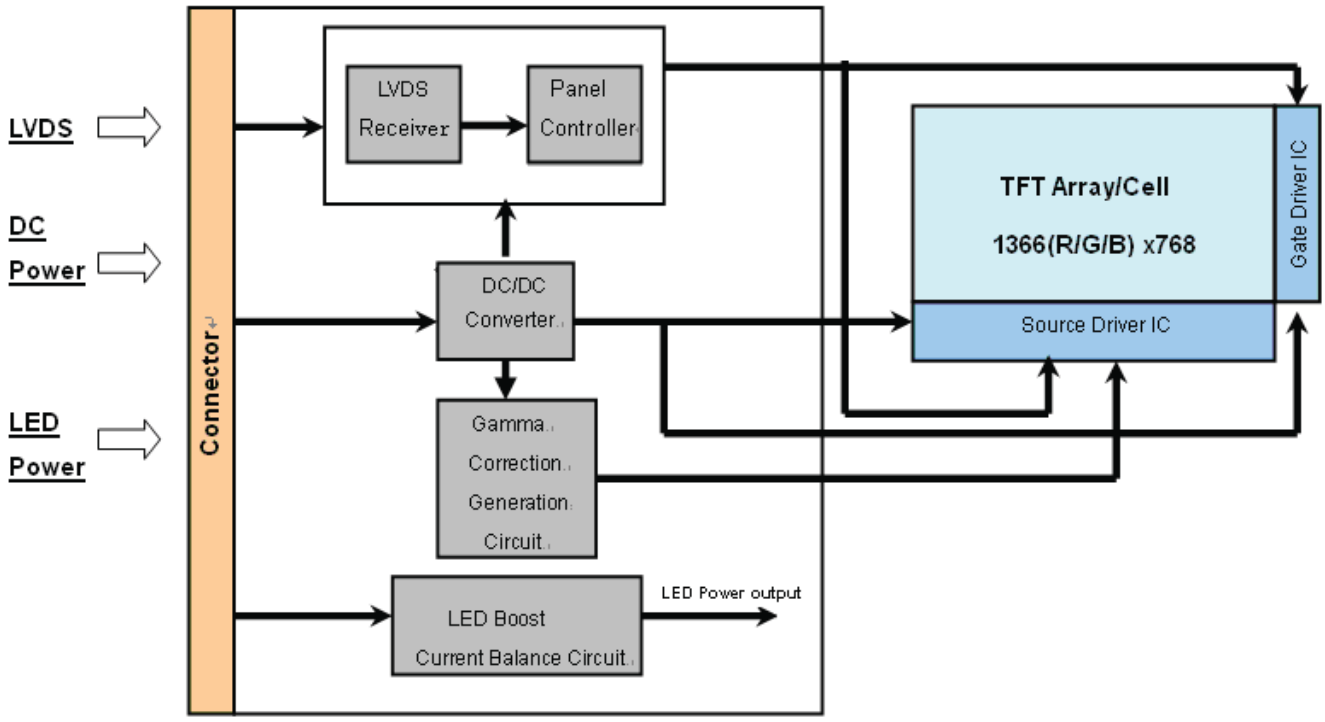
Figure 1 Shows the functional block diagram of the LCD module.

Figure 1 Block Diagram



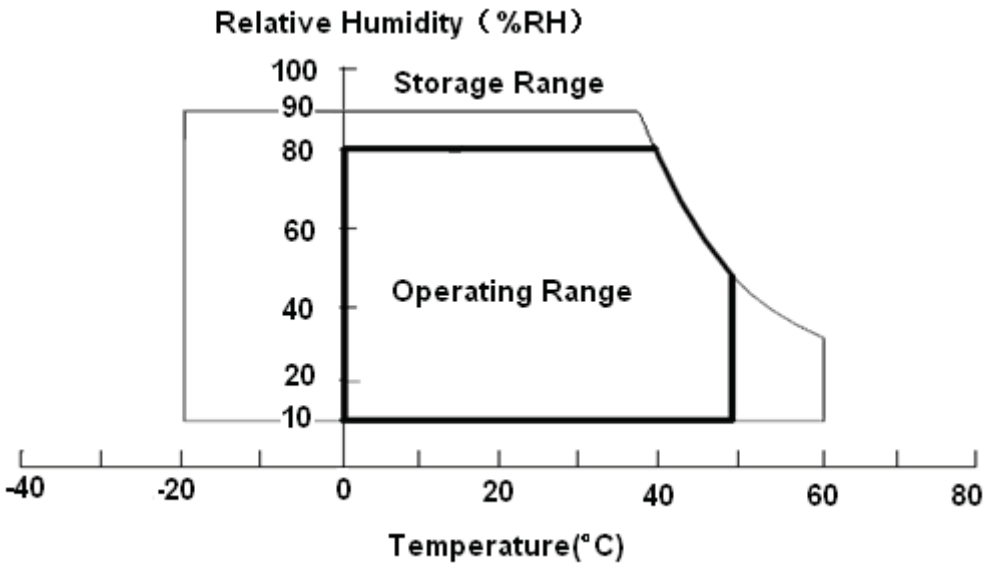
2.0 Absolute Maximum Ratings

Table 1

Item	Symbol	Min.	Max.	Unit	Conditions
Supply Voltage	VDD	-0.5	4.0	V	-
Supply V_LED Voltage	V_LED	6	21	V	
Input Signal	-	-0.5	2.6	V	LVDS signals
Operating Temperature	TOP	0	50	deg. C	(Note)
Operating Humidity	HOP	10	90	%RH	(Note)
Storage Temperature	TST	-20	60	deg. C	(Note)
Storage Humidity	HST	10	90	%RH	(Note)

Note (1) Maximum Wet-Bulb should be 39 degree C. No condensation.
(2) When you apply the LCD module for OA system. Please make sure to keep the temperature of LCD module is less than 60℃
(3) Storage /Operating temperature

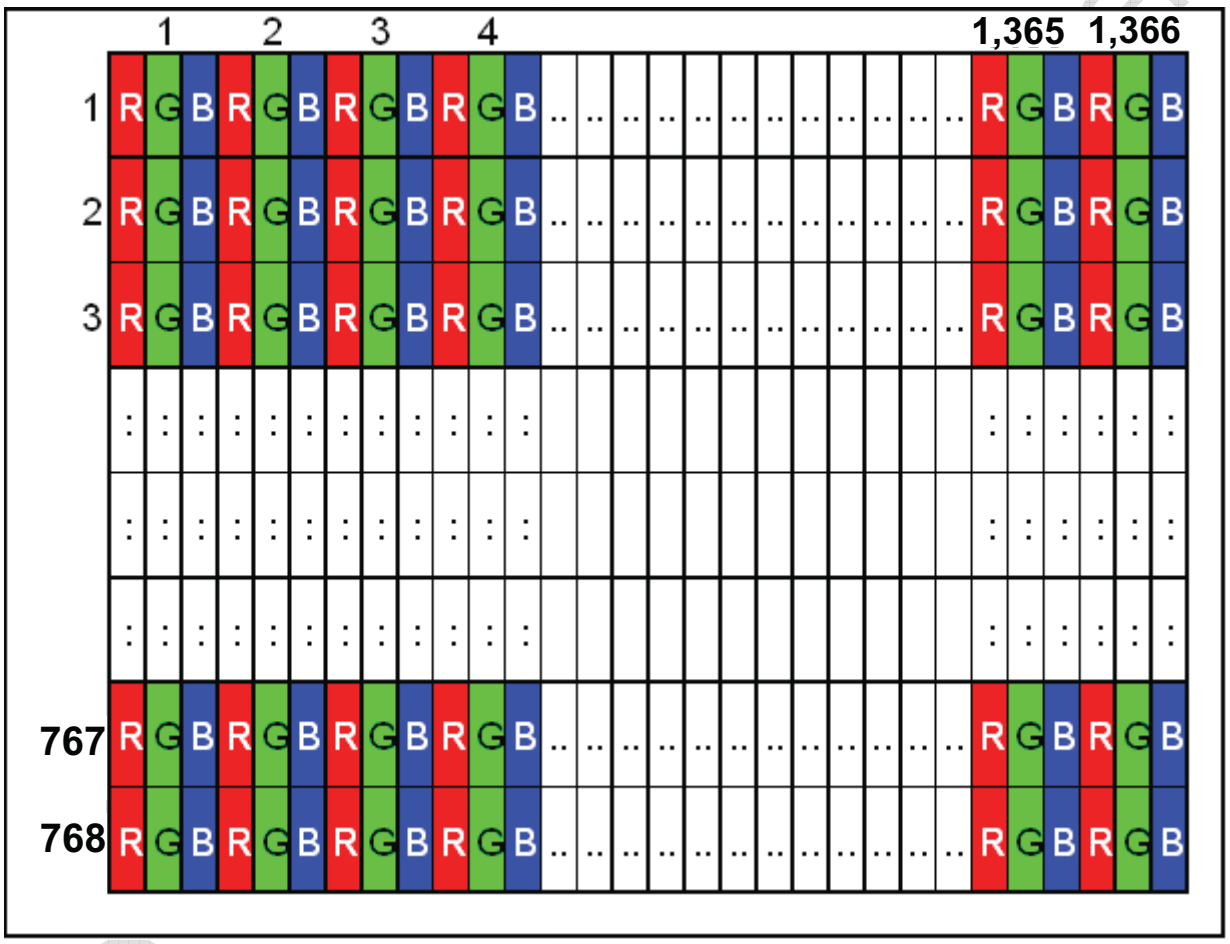
Figure 2 Absolute Ratings of Environment of the LCD module:



3.0 Pixel Format Image

Figure 3 shows the relationship of the input signals and LCD pixel format image.

Figure 3 Pixel Format



4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as following notes

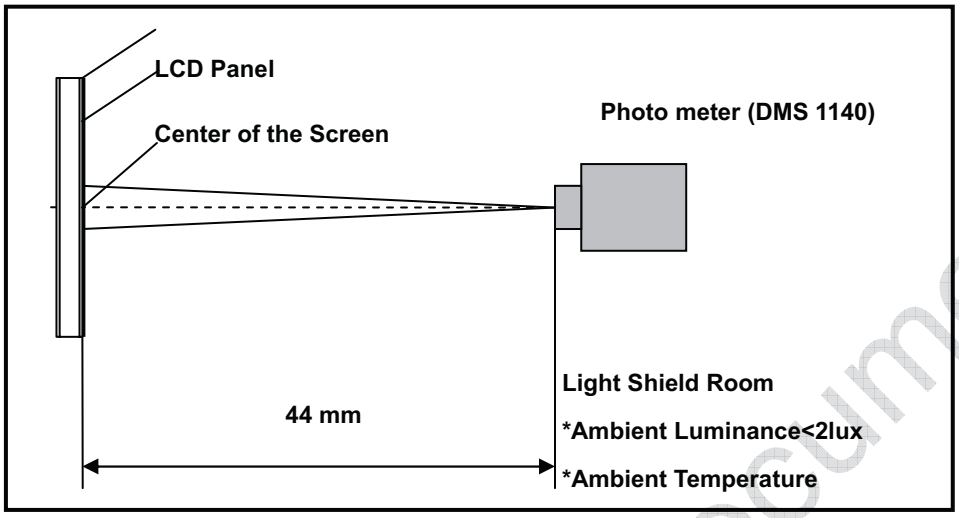
Table 2 Optical Characteristics

Item	Conditions		Specification			
			Min.	Typ.	Max.	Note
Viewing Angle [degrees] K=Contrast Ratio>10	Horizontal	Left	40	45	-	A, B,C,F,G
		Right	40	45	-	
	Vertical	Up	10	15	-	
		Down	30	35	-	
Contrast Ratio	Center		400	500		A, B,D,F,G
Response Time [ms]	Rising +Falling		-	8	16	A, B,E
Color Chromaticity (CIE1,931)	Red	x	Typ. -0.03	0.587	Typ. +0.03	A,B,F,G
	Red	y		0.349		A,B,F,G
	Green	x		0.337		A,B,F,G
	Green	y		0.565		A,B,F,G
	Blue	x		0.153		A,B,F,G
	Blue	y		0.110		A,B,F,G
	White	x	0.283	0.313	0.343	A,B,F,G
	White	y	0.299	0.329	0.359	A,B,F,G
Panel Transmittance (%)	-		5.7	6.2	-	F,G,H

Note: A. Measurement Setup:

The LCD module should be stabilized at given temperature for 15 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 15 minutes in a windless room.

Figure 4 Measurement Setup



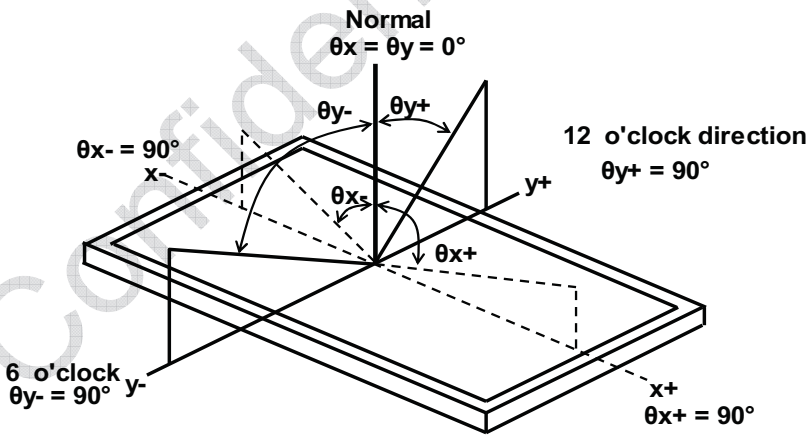
B. The LED input parameter setting as:

V_LED: 12V (±0.1V)

PWM_LED: duty 100 %

C. Definition of Viewing Angle

Figure 5 Definition of Viewing Angle



D. Definition Of Contrast Ratio (CR)

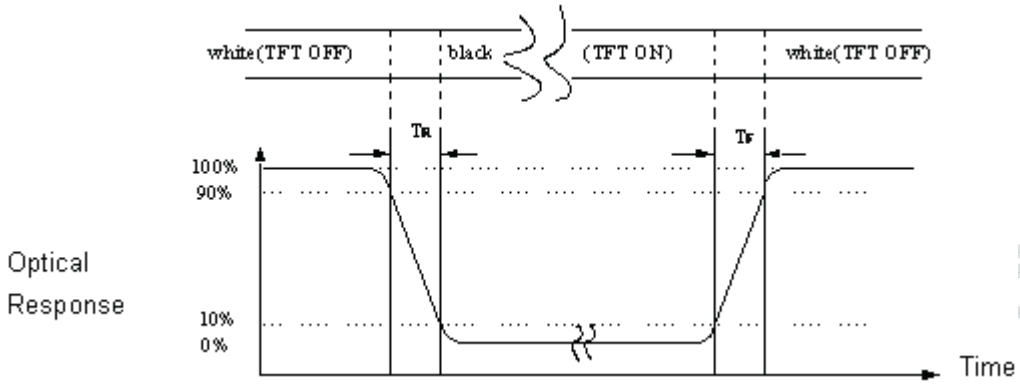
The contrast ratio can be calculated by the following expression

Contrast Ratio (CR) = L63 / L0

L63: Luminance of gray level 63, L0: Luminance of gray level 0

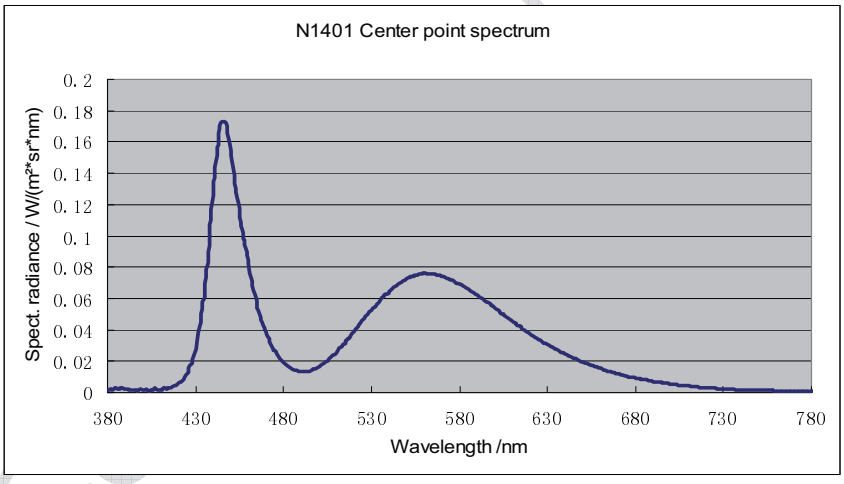
E. Definition Of Response Time (T_R, T_F)

Figure 6 Definition of Response Time



F. Light source is the BLU which is supplied by IVO.

G. Back light Spectrum (Reference)



H. Definition of Transmittance

Module is without signal input.

$$\text{Transmittance} = \frac{\text{Luminance of LCD module}}{\text{Luminance of backlight}} * 100\%$$

5.0 Backlight Characteristics(Reference)

Table 3 Parameter Guideline for LED Backlight

Symbol	Parameter		Min.	Typ.	Max.	Units	Condition
V_LED	LED Input		6	12	21	[V]	Ta=25[deg A] Note A
V_PWM_EN	PWM Signal Voltage	High	2.5	-	5.5	V	Ta=25[deg A]
		Low	-	-	0.5		
FPWM	Input PWM Frequency		100	-	1K	Hz	-
V_DBC_EN	DBC Voltage	High	1.5	-	3.6	V	Ta=25[deg A]
		Low	0	-	0.5		
V_CE_EN	Color Engine Voltage	High	1.5	-	3.6	V	Ta=25[deg A]
		Low	0	-	0.5		
V_LED_EN	LED Enable Voltage	High	2.5	-	5.5	V	Ta=25[deg A]
		Low	-	-	0.5		
PWM_LED	Duty Ratio		5	-	100	%	-

Note A: Strong propose to set LED Input Voltage 12V, it would be best power efficiency.

6.0 Electrical Characteristics

6.1 Interface Connector

6.1.1 Interface Connector

Table 4 Connector Name / Designation

Manufacturer	UJU(or equivalent)
Type / Part Number	IS050-L40B-C10
Mating Receptacle/Part Number	IPEX 20453-040T-11

Table 5 Signal Pin Assignment

Pin #	Signal Name	Description	Remarks
1	NC	Not connected(Reserve)	-
2	VDD	Power supply 3.3V(typical)	-
3	VDD	Power supply 3.3V(typical)	-
4	VDD_EDID	Power supply for EDID	-
5	NC	Not connected(Reserve)	-
6	SCL	EDID clock	-
7	SDA	EDID data	-
8	RX_0-	LVDS differential data input	-
9	RX_0+	LVDS differential data input	-
10	GND	Ground	-
11	RX_1-	LVDS differential data input	-
12	RX_1+	LVDS differential data input	-
13	GND	Ground	-
14	RX_2-	LVDS differential data input	-
15	RX_2+	LVDS differential data input	-
16	GND	Ground	-
17	RX_CLK-	LVDS differential clock input	-
18	RX_CLK+	LVDS differential clock input	-
19	V_CE_EN	Color Engine EN(High Enable)	-
20	NC	Not connected(Reserve)	-
21	NC	Not connected(Reserve)	-
22	GND	GND	-
23	NC	Not connected(Reserve)	-
24	NC	Not connected(Reserve)	-

25	GND	GND	-
26	NC	Not connected(Reserve)	-
27	NC	Not connected(Reserve)	-
28	GND	GND	-
29	NC	Not connected(Reserve)	-
30	NC	Not connected(Reserve)	-
31	V_LED_GND	LED Ground	-
32	V_LED_GND	LED Ground	-
33	V_LED_GND	LED Ground	-
34	NC	Not connected(Reserve)	-
35	V_PWM _EN	System PWM Signal Input	-
36	V_LED_EN	LED enable pin	-
37	V_DBC_EN	Dynamic Backlight Control(High	-
38	V_LED	LED Power Supply	-
39	V_LED	LED Power Supply	-
40	V_LED	LED Power Supply	-

Note A: All input signals shall be low or Hi-Z state when VDD is off.

6.1.2 LED Driving Specification

Table 6 Connector Name / Designation

Manufacturer	UJU (or equivalent)
Type / Part Number	PF050-009B-C11-S or compatible
Mating Receptacle/Part Number	Compatible

Table 7 Pin Assignment

Pin #	Signal Name Description
1	LED power bus (LED Anode)
2	LED power bus (LED Anode)
3	NC
4	LCD cathode
5	LCD cathode
6	LCD cathode
7	LCD cathode
8	LCD cathode
9	LCD cathode

6.2 LVDS Receiver

6.2.1 Signal Electrical Characteristics For LVDS Receiver

The built-in LVDS receiver is compatible with (ANSI/TIA/TIA-644) standard.

Table 8 LVDS Receiver Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Differential Input High Threshold	Vth	-	-	+100	mV	Vcm=+1.2V
Differential Input Low Threshold	Vtl	-100	-	-	mV	Vcm=+1.2V
Magnitude Differential Input Voltage	|Vid|	100	-	600	mV	-
Common Mode Voltage	Vcm	|Vid|/2+0.6	1.2	1.8-|Vid|/2	V	-
Common Mode Voltage Offset	ΔVcm	-	-	50	mV	Vcm=+1.2V

Note:

A. Input signals shall be low or Hi-Z state when VDD is off.

B. All electrical characteristics for LVDS signal are defined and shall be measured at the interface connector of LCD.

Figure 8 Voltage Definitions

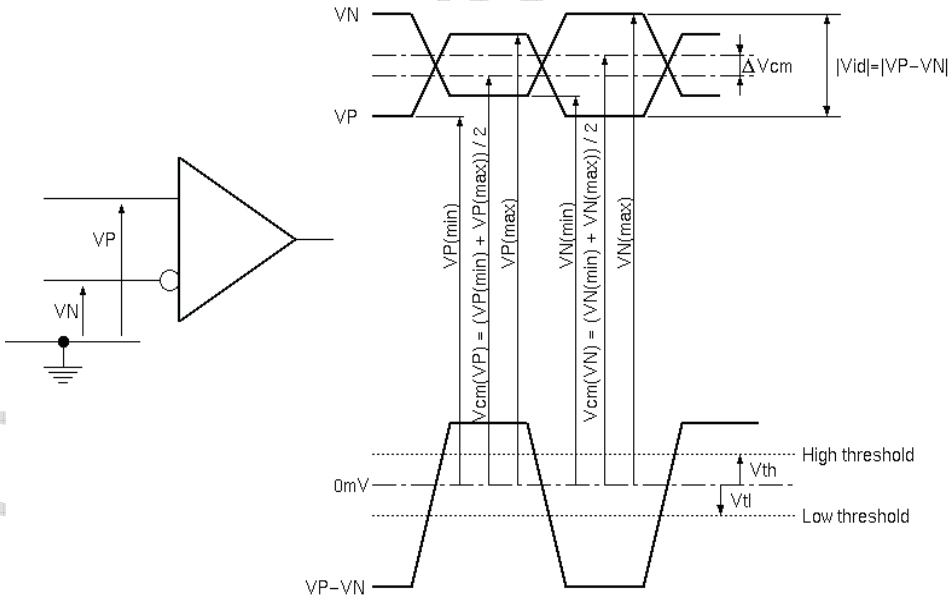


Figure 9 Measurement System

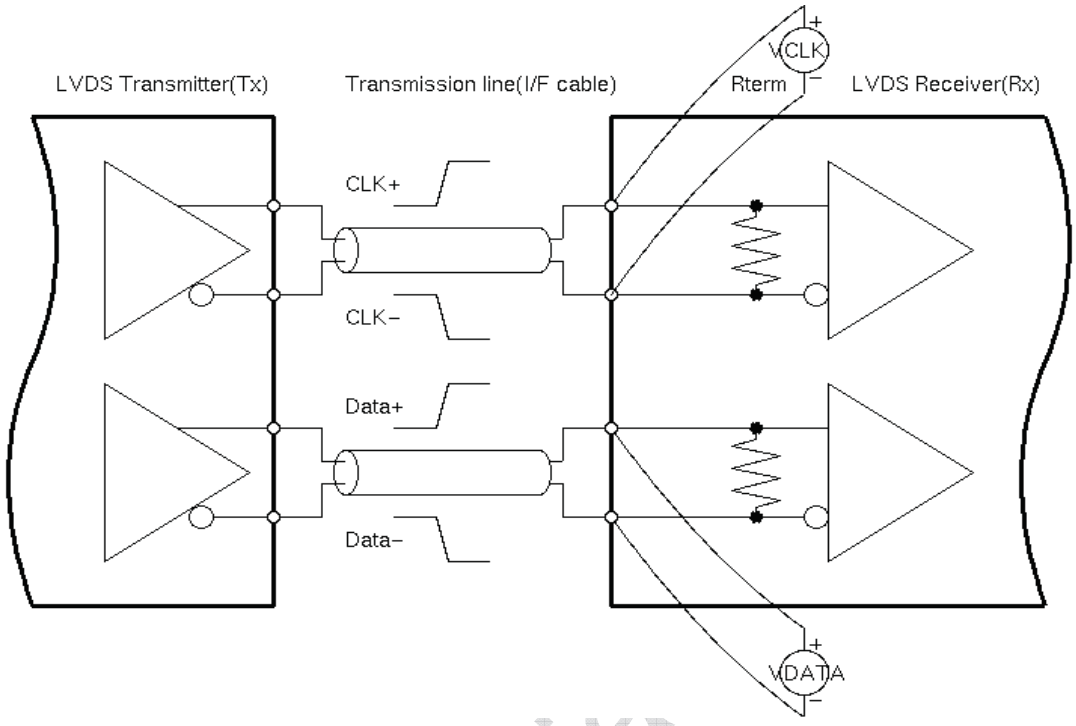
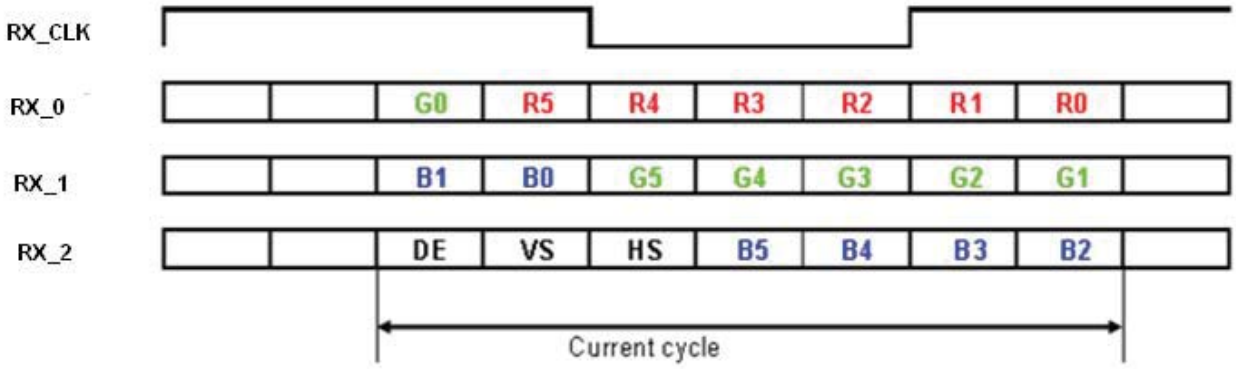


Figure 10 Data Mapping

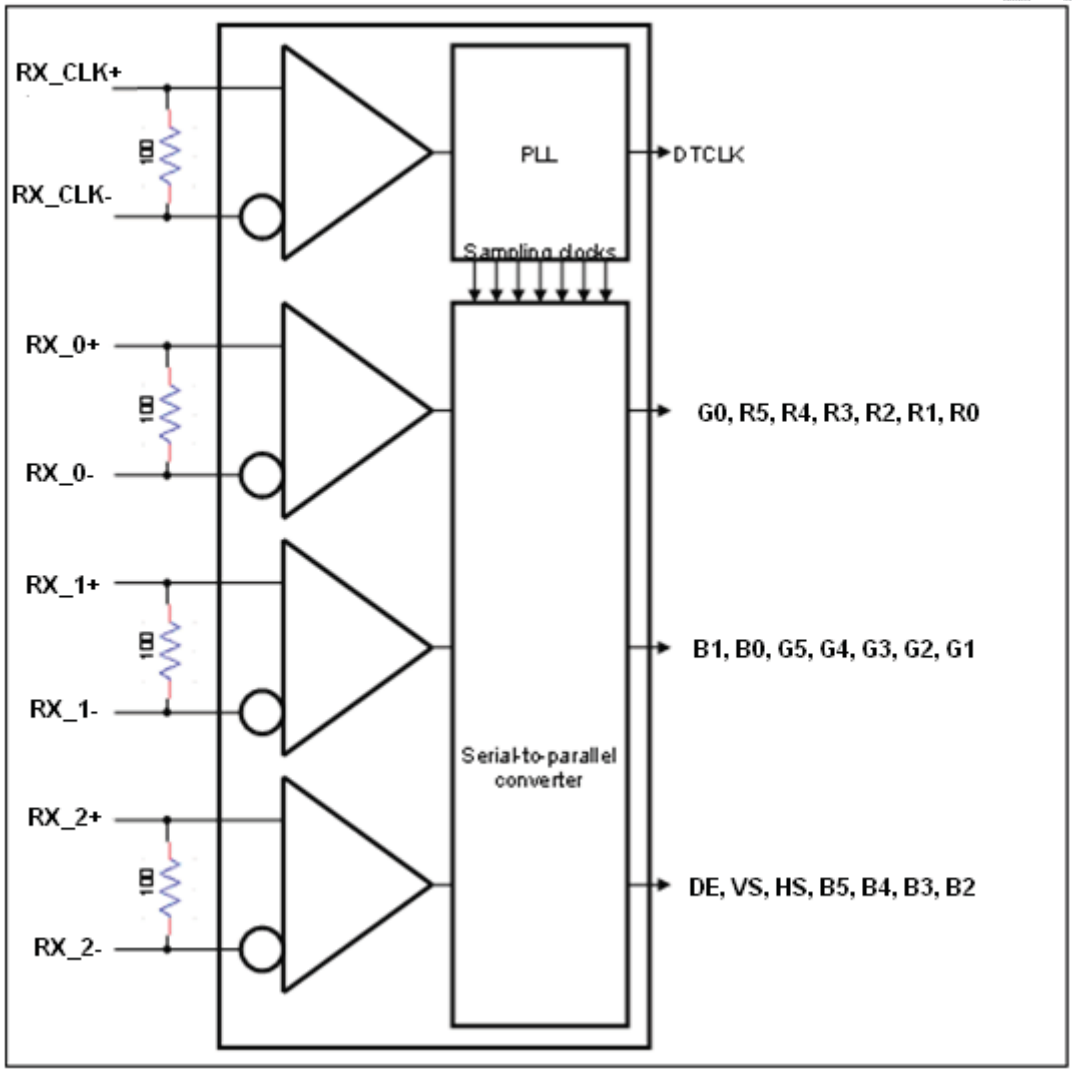


6.2.2 LVDS Receiver Internal Circuit

Figure 11 LVDS Receiver Internal Circuit

Shows the internal block diagram of the LVDS receiver. This LCD module equips termination resistors for LVDS link.

Figure 11 LVDS Receiver Internal Circuit



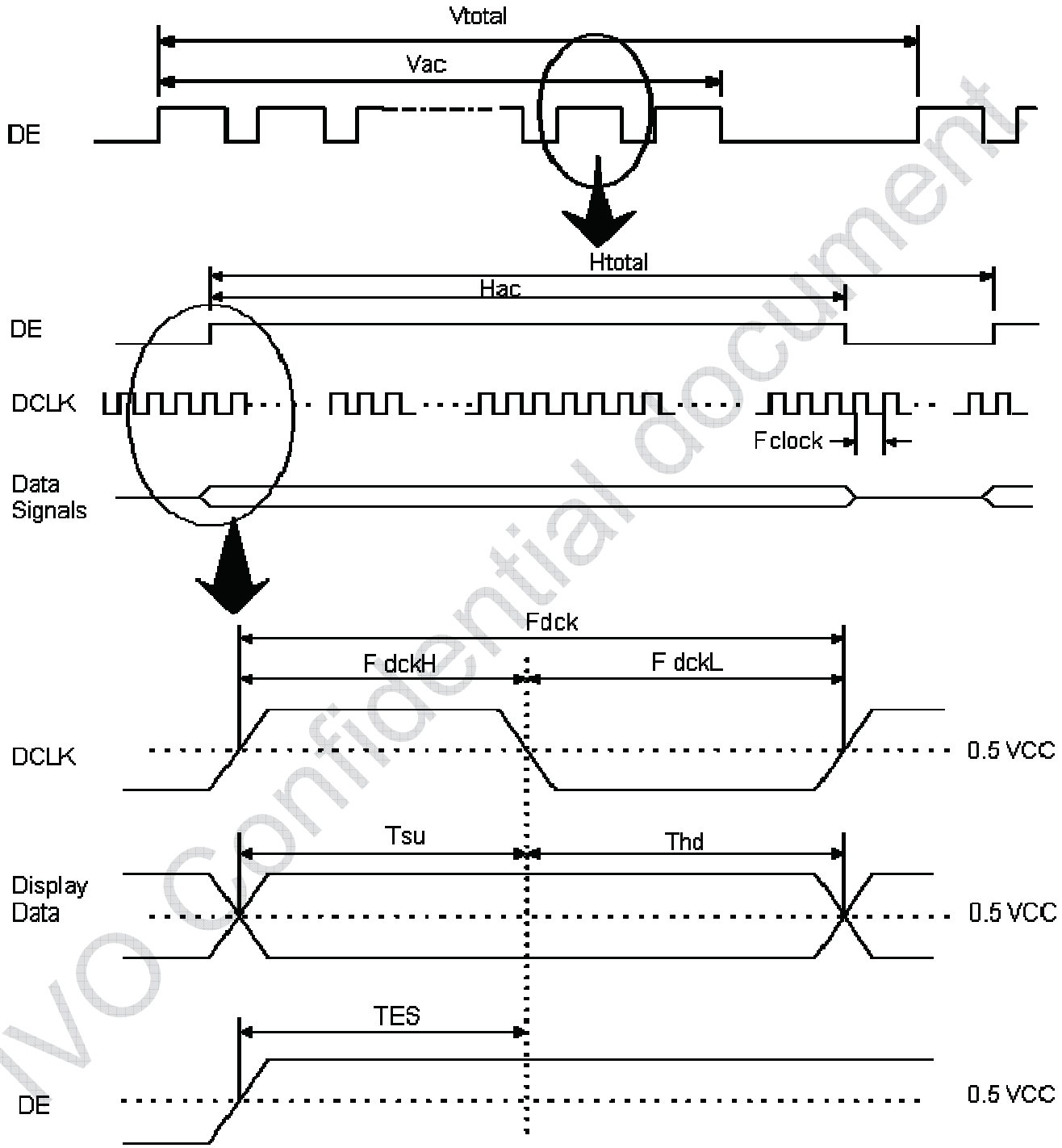
7.0 Interface Timings

7.1 Timing Characteristics

Table 9 Interface Timings

Parameter	Symbol	Unit	Min.	Typ.	Max.
LVDS Clock Frequency(single)	Fdck	MHz	65	75.4	85
H Total Time	Htotal	Clocks	1,506	1,560	1,600
H Active Time	Hac	Clocks	1,366	1,366	1,366
V Total Time	Vtotal	Lines	780	806	816
V Active Time	Vac	Lines	768	768	768
Frame Rate	Vsync	Hz	55	60	65

Figure 12 Timing Characteristics



Note: TES is data enable signal setup time.

8.0 Power Consumption

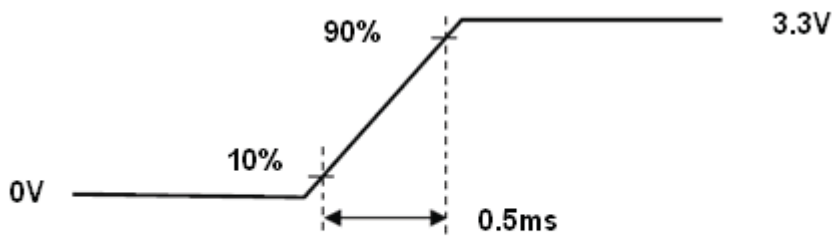
Input power specifications are as follows.

Table 10 Power Consumption

Symbol	Parameter	Min.	Typ.	Max.	Units	Condition
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[V]	-
IDD	VDD Current	-	0.34	-	[A]	Black Pattern, 60Hz
PDD	VDD Power	-	-	1.2	[W]	Black Pattern, 60Hz
Irush	Rush Current	-	-	2.0	[A]	Note 1
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	200	[mV]p-p	Note 2

Note 1.Measure Condition

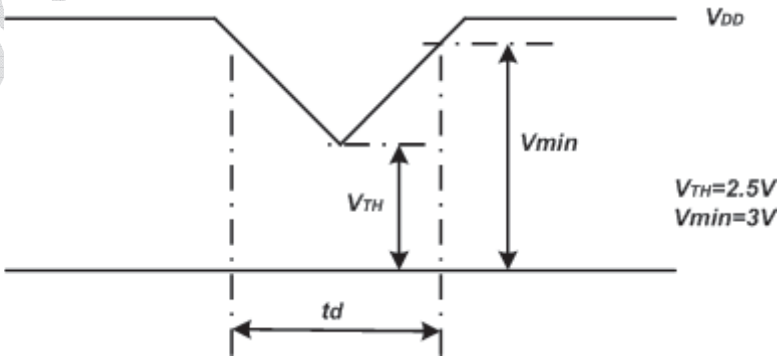
Figure 13 VDD rising time



VDD rising time

2. VDD Power Dip Condition

Figure 14 VDD Power Dip



If $V_{TH} < V_{DD} \leq Vmin$，then $t_d \leq 10ms$；when the voltage return to normal our panel must revive automatically.

9.0 Power ON/OFF Sequence

VDD power on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.

Figure 15 Power Sequence

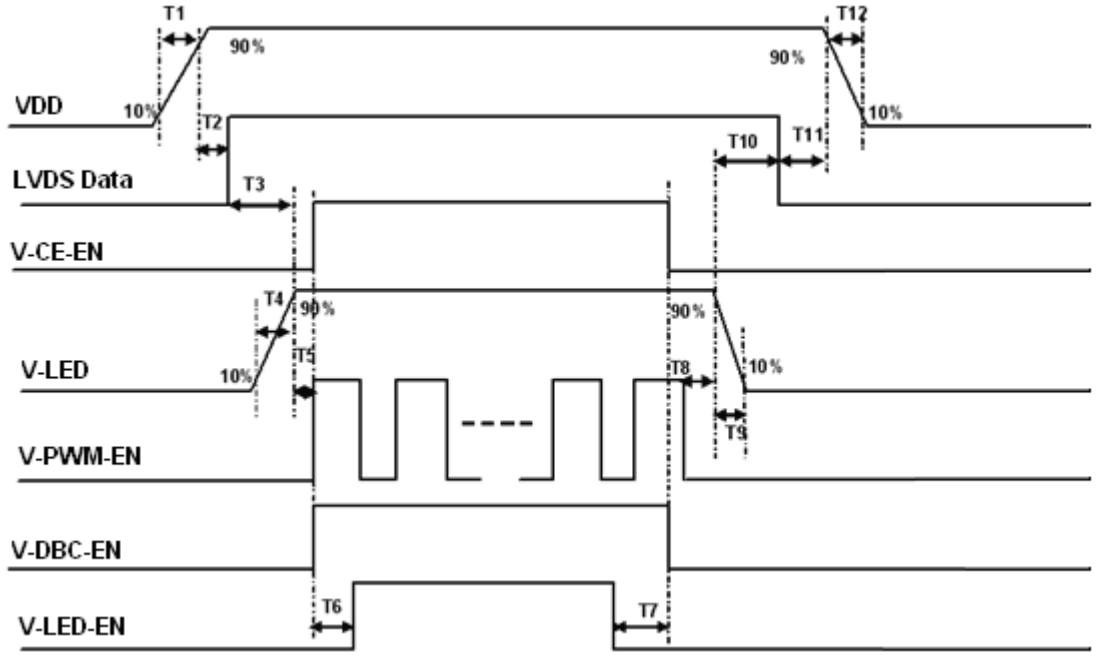


Table 11 Power Sequencing Requirements

Parameter	Unit	min	typ	max
T1	ms	0.5	-	10
T2	ms	30	40	90
T3	ms	200	-	-
T4	ms	0.5	-	10
T5	ms	10	-	-
T6	ms	10	-	-
T7	ms	0	-	-
T8	ms	10	-	-
T9	ms	-	10	30
T10	ms	200	-	-
T11	ms	0	-	50
T12	ms	-	10	30

10.0 Mechanical Characteristics Connector

Figure 16 Reference Outline Drawing (Front Side)

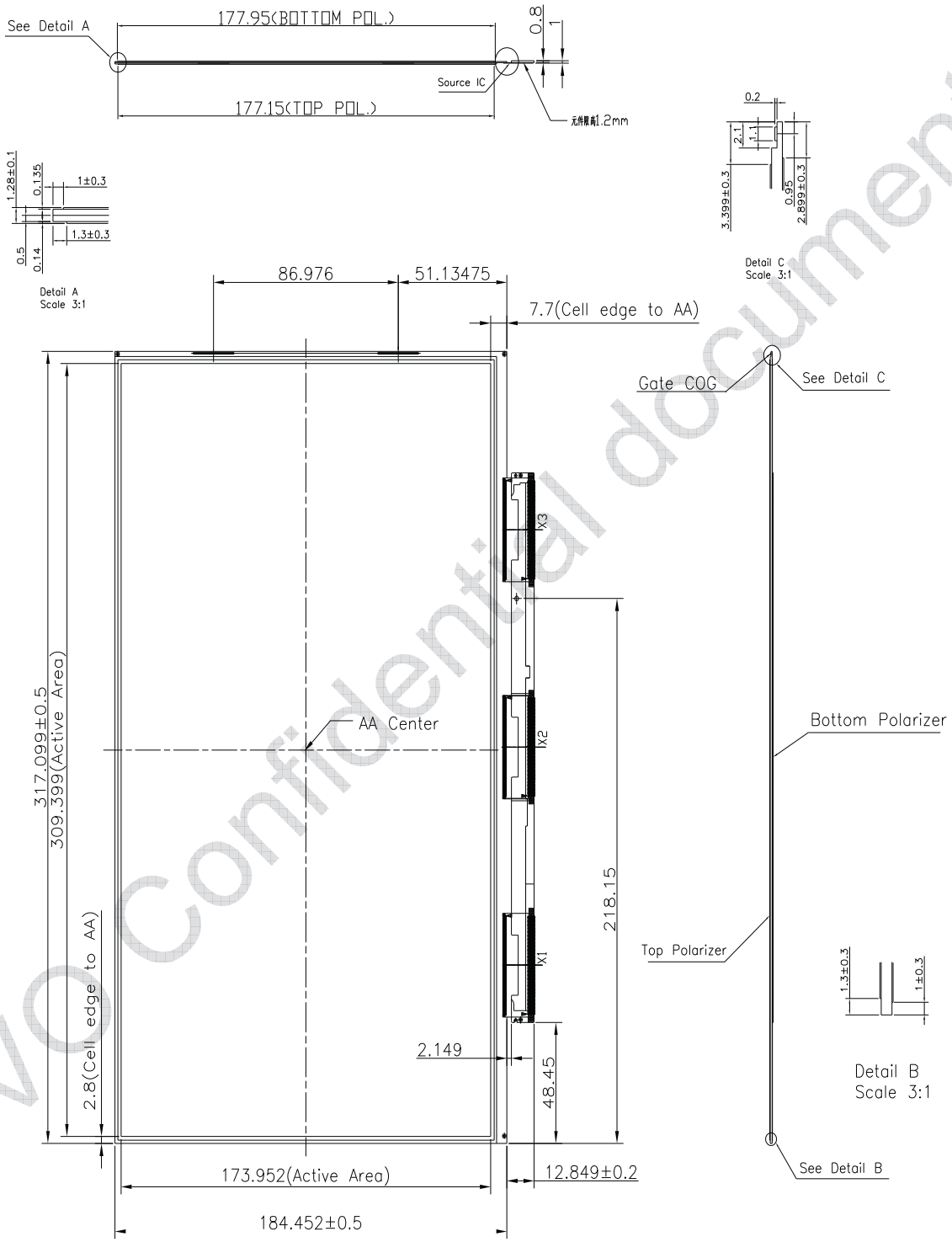
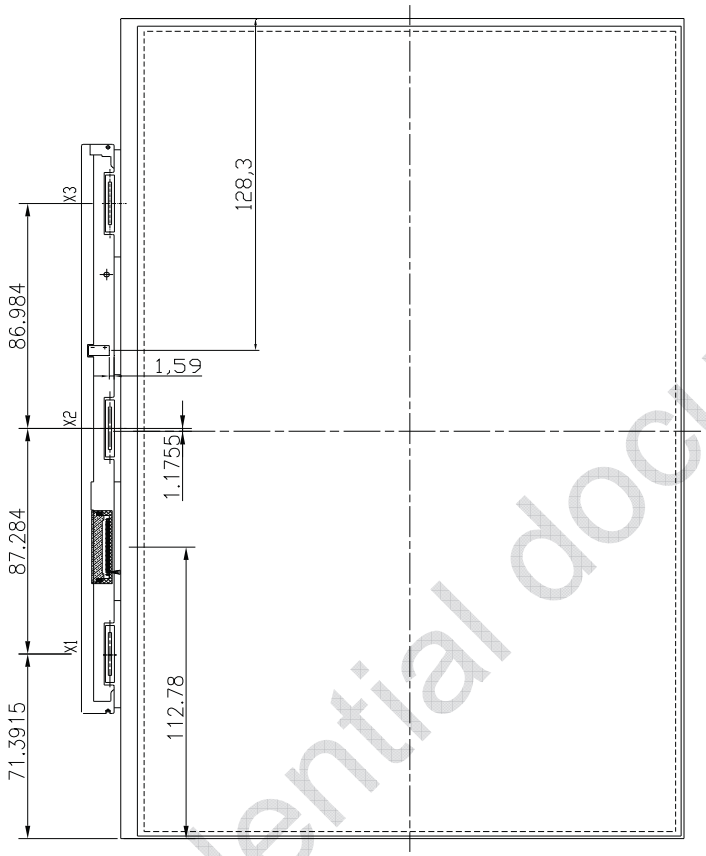


Figure 17 Reference Outline Drawing (Back Side)

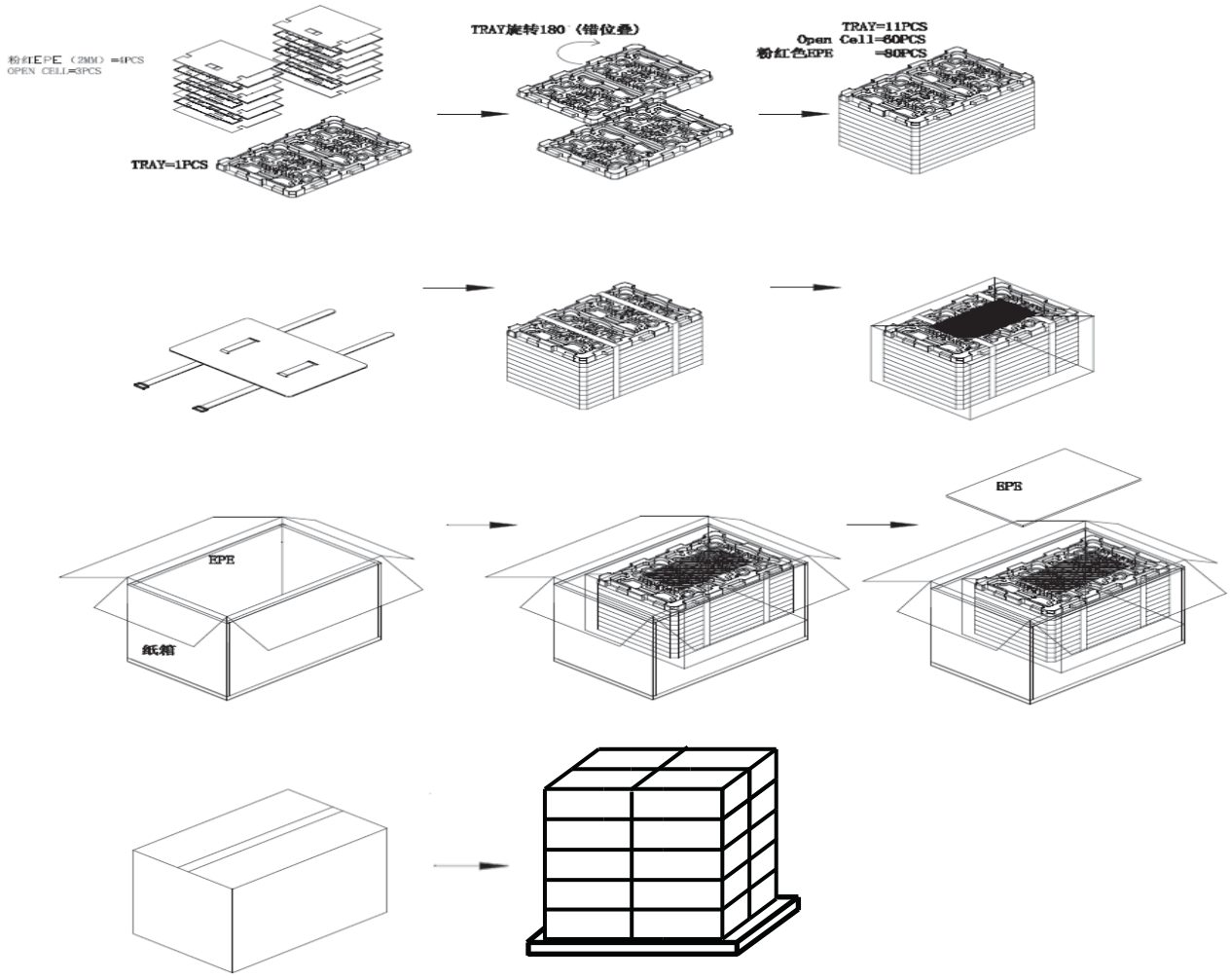


10.1 Dimension Specifications

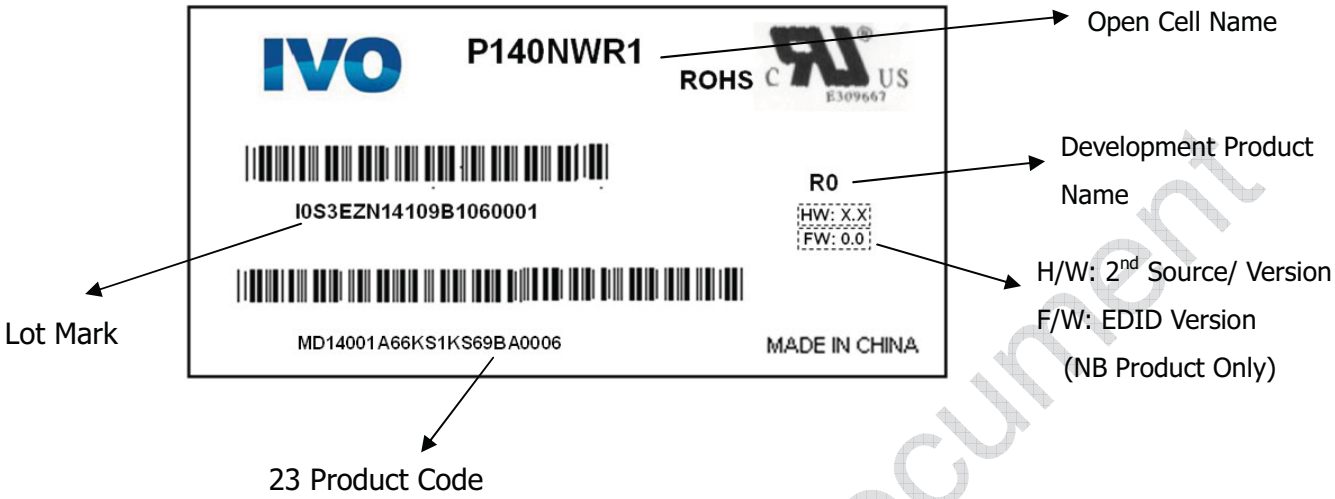
Table 6 Open Cell Dimension Specifications

Width [mm]		197.3±0.5
Height [mm]		317.1±0.5
Thickness	Glass(Cell)	1.28±0.2
	PCB	0.8±0.1
	Component	1.2（Max）
Weight [g]		173(Typ.)

11.0 Package Specification



12.0 Lot Mark



12.1 Lot Mark

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

code 1,2,4,5,6,7,8,9,10,11,16: IVO internal flow control code.
code 3: Production location.
code 12: Production year.
code 13: Production month.
code 14,15: Production date.
Code 17,18,19,20: Serial number.

Note (1) Production Year

Year	2,006	2,007	2,008	2,009	2,010	2,011	2,012	2,013	2,014	2,015
Mark	6	7	8	9	A	B	C	D	E	F

Note (2) Production Month

Month	Jan.	Feb.	Mar.	Apr.	May.	Jun.	Jul.	Aug.	Sep.	Oct	Nov.	Dec.
Mark	1	2	3	4	5	6	7	8	9	A	B	C

12.2 23 Product Barcode

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

code 1,2: MD mindtech display.
code 3,4,5,6,7: IVO internal module name.
code 8,9,10,13,16: IVO internal flow control code.
code 11,12: Cell location Suzhou defined as “SZ”.
code 14 ,15: Module line kunshan defined as” KS”.
code 17,18,19 : Year, Month, Day Refer to Note(1) and Note(2) of Lot Mark.
code 20~23 : Serial Number.

13.0 General Precaution

13.1 Use Restriction

This product is not authorized for use in life supporting systems, aircraft navigation control systems, military systems and any other application where performance failure could be life-threatening or otherwise catastrophic.

13.2 Disassembling or Modification

Do not disassemble or modify the module. It may damage sensitive parts inside LCD module, and may cause scratches or dust on the display. MTD does not warrant the module, if customers disassemble or modify the module.

13.3 Breakage of LCD Panel

12.3.1 If LCD panel is broken and liquid crystal spills out, do not ingest or inhale liquid Crystal, and do not contact liquid crystal with skin.
12.3.2 If liquid crystal contacts mouth or eyes, rinse out with water immediately.
12.3.3 If liquid crystal contacts skin or cloths, wash it off immediately with alcohol and Rinse thoroughly with water.
12.3.4 Handle carefully with chips of glass that may cause injury, when the glass is

13.4 Absolute Maximum Ratings and Power Protection Circuit

12.3.1 Do not exceed the absolute maximum rating values, such as the supply voltage variation, input voltage variation, variation in parts’ parameters, environmental temperature; etc otherwise LCD module may be damaged.
12.3.2 Please do not leave LCD module in the environment of high humidity and high temperature for a long time.
12.3.3 It’s recommended employing protection circuit for power supply.

13.5 Operation

12.3.1 Do not touch, push or rub the polarizer with anything harder than HB pencil lead. Use fingerstalls of soft gloves in order to keep clean display quality, when Persons handle the LCD module for incoming inspection or assembly.
12.3.2 When the surface is dusty, please wipe gently with absorbent cotton or other soft Material
12.3.3 Wipe off saliva or water drops as soon as possible. If saliva or water drops Contact with polarizer for a long time, they may causes deformation or color Fading

12.3.4 When cleaning the adhesives, please use absorbent cotton wetted with a little Petroleum benzene or other adequate solvent

13.6 Static Electricity

12.3.1 Protection film must remove very slowly from the surface of LCD module to Prevent from electrostatic occurrence.

12.3.2 Because LCD module uses CMOS-IC on circuit board and TFT-LCD panel, it is Very weak to electrostatic discharge, Please be careful with electrostatic Discharge

12.3.3 Persons who handle the module should be grounded through adequate methods.

13.7 Strong Light Exposure

The module shall not be exposed under strong light such as direct sunlight. Otherwise, Display characteristics may be changed.

13.8 Disposal

When disposing LCD module, obey the local environmental regulations.