ShinDengen

P15LF6QTKD

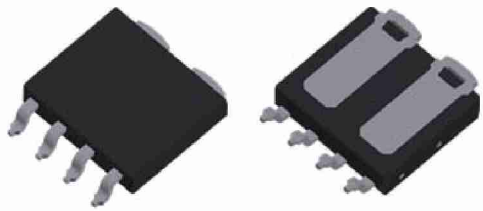
Power MOSFETs
60V, 15A, Dual N-channel

Feature

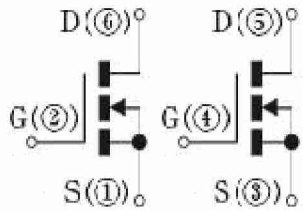
- N-channel
- Small SMD
- Dual type
- 4.5V Gate Drive
- Low Capacitance
- Based on AEC-Q101
- Halogen free
- Pb free terminal
- RoHS:Yes

OUTLINE

Package (House Name): LF_Dual



Equivalent circuit



Absolute Maximum Ratings (unless otherwise specified : Tc=25°C, per FET)

Item	Symbol	Conditions	Ratings	Unit
Storage temperature	Tstg		-55 to 175	°C
Channel tempertature	Tch		-55 to 175	°C
Drain-source voltage	V_{DSS}		60	V
Gate-source voltage	V_{GSS}		±20	V
Continuous drain current(DC)	I_D		15	A
Continuous drain current(Peak)	I_{DP}	Pulse width 10μs, duty=1/100	45	A
Continuous source current(DC)	Is		15	A
Total power dissipation	P_T	With heatsink	35	W
Total power dissipation	P_T	※	2.5	W
Total power dissipation	P_T	※	1.5	W
Single avalanche current	I_{AS}	Starting Tch=25°C Tch≦150°C	11	A
Single avalanche energy	E_{AS}	Starting Tch=25°C Tch≦150°C	13	mJ

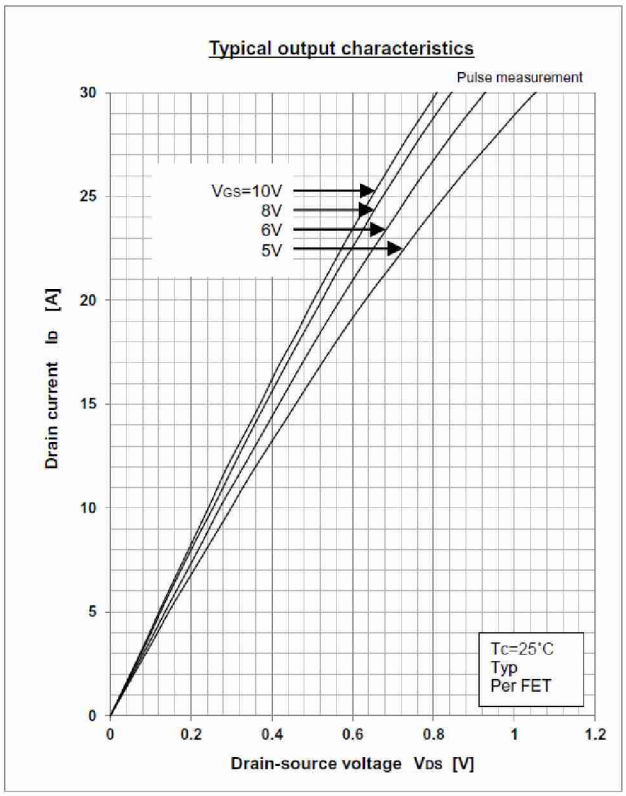
※ :See the original Specifications

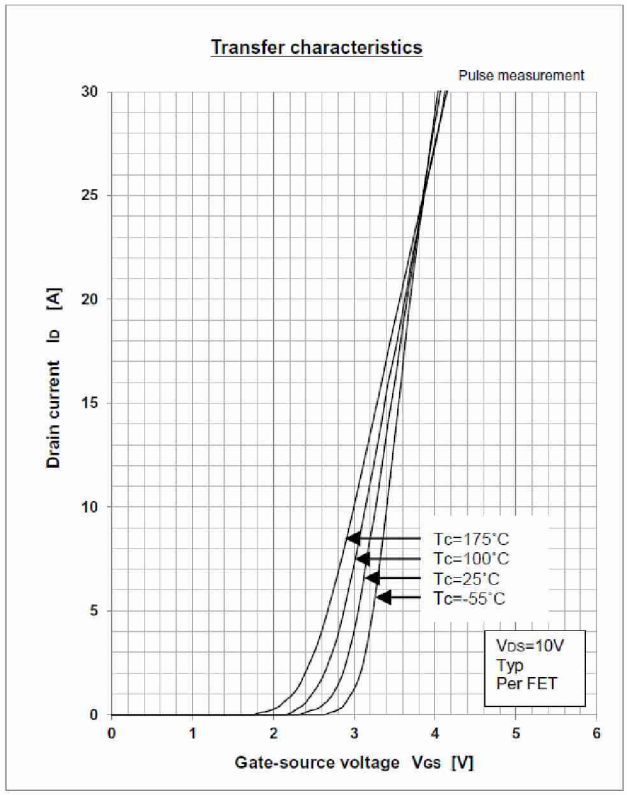
Electrical Characteristics (unless otherwise specified : Tc=25°C, per FET)

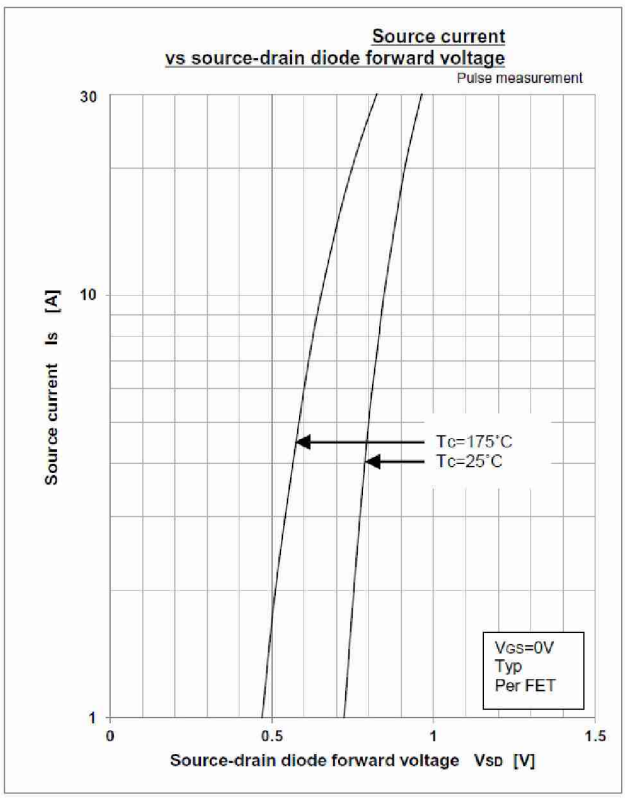
Item	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Drain-Source breakdown voltage	$V_{(BR)DSS}$	ID=1mA, VGS=0V	60			V
Zero gate voltage drain current	I_{DSS}	VDS=60V, VGS=0V			1	μA
Gate-source leakage current	I_{GSS}	VGS=±20V, VDS=0V			±0.1	μA
Forward transconductance	g_{fs}	ID=7.5A, VDS=10V	4			S
Static drain-source on-state resistance	$R_{DS(ON)}$	ID=7.5A, VGS=10V		0.024	0.03	Ω
Static drain-source on-state resistance	$R_{DS(ON)}$	ID=7.5A, VGS=4.5V		0.032	0.043	Ω
Gate threshold voltage	Vth	ID=1mA, VDS=10V	1.5	2	2.5	V
Source-drain diode forward voltage	V_{SD}	IS=15A, VGS=0V			1.2	V
Thermal resistance	Rth(j-c)	Junction to case, with heatsink			4.25	°C/W
Thermal resistance	Rth(j-a)	Junction to ambient ※			60	°C/W
Thermal resistance	Rth(j-a)	Junction to ambient ※			100	°C/W
Total gate charge	Qg	VDD=48V, VGS=10V, ID=15A		15		nC
Gate to source charge	Qgs	VDD=48V, VGS=10V, ID=15A		4.1		nC
Gate to drain charge	Qgd	VDD=48V, VGS=10V, ID=15A		3.9		nC
Input capacitance	Ciss	VDS=25V, VGS=0V, f=1MHz		632		pF
Reverce transfer capacitnce	Crss	VDS=25V, VGS=0V, f=1MHz		38		pF
Output capacitance	Coss	VDS=25V, VGS=0V, f=1MHz		86		pF
Turn-on delay time	td(on)	ID=7.5A, RL=4.00Ω, VDD=30V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		3.5		ns
Rise time	tr	ID=7.5A, RL=4.00Ω, VDD=30V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		9.5		ns
Turn-off delay time	td(off)	ID=7.5A, RL=4.00Ω, VDD=30V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		12		ns
Fall time	tf	ID=7.5A, RL=4.00Ω, VDD=30V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		4		ns
Diode reverse recovery time	trr	IF=15A, VGS=0V, di/dt=100A/μs		35		ns
Diode reverse recovery charge	Qrr	IF=15A, VGS=0V, di/dt=100A/μs		32		nC

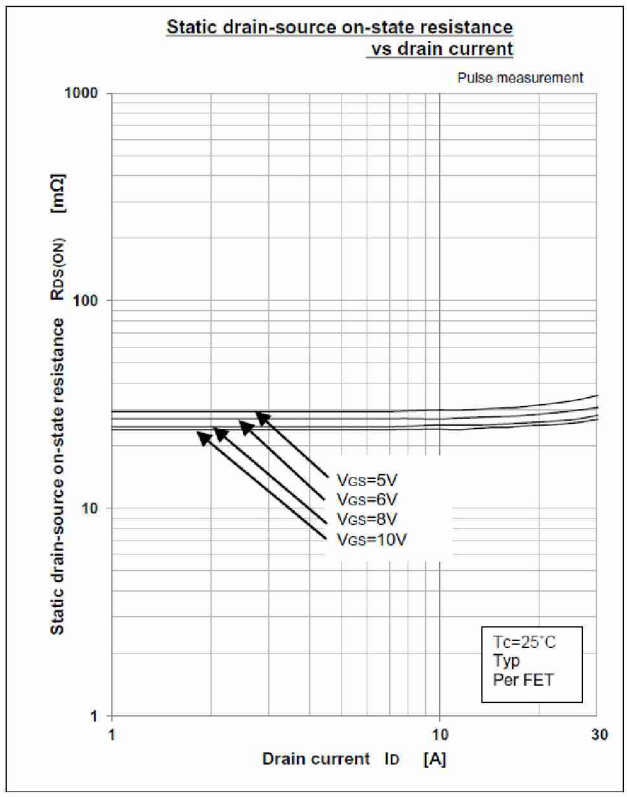
※ :See the original Specifications

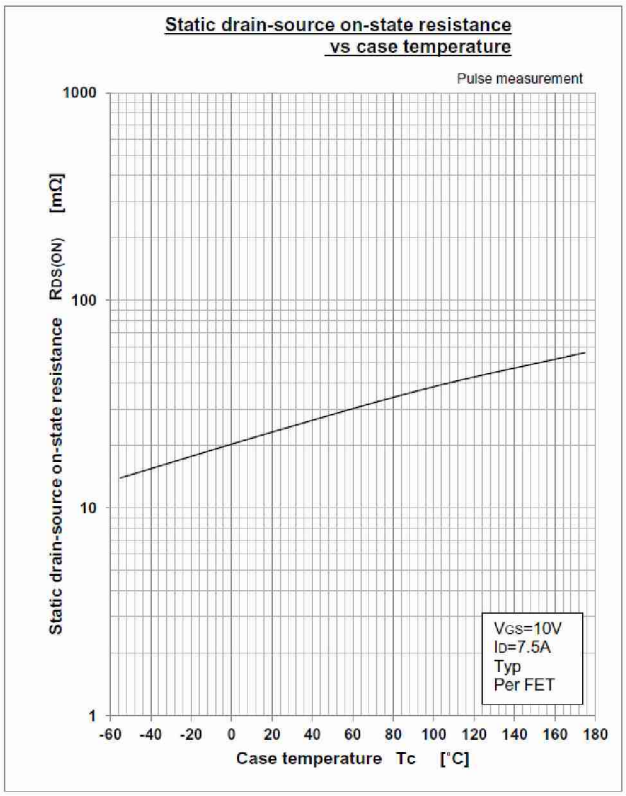
CHARACTERISTIC DIAGRAMS

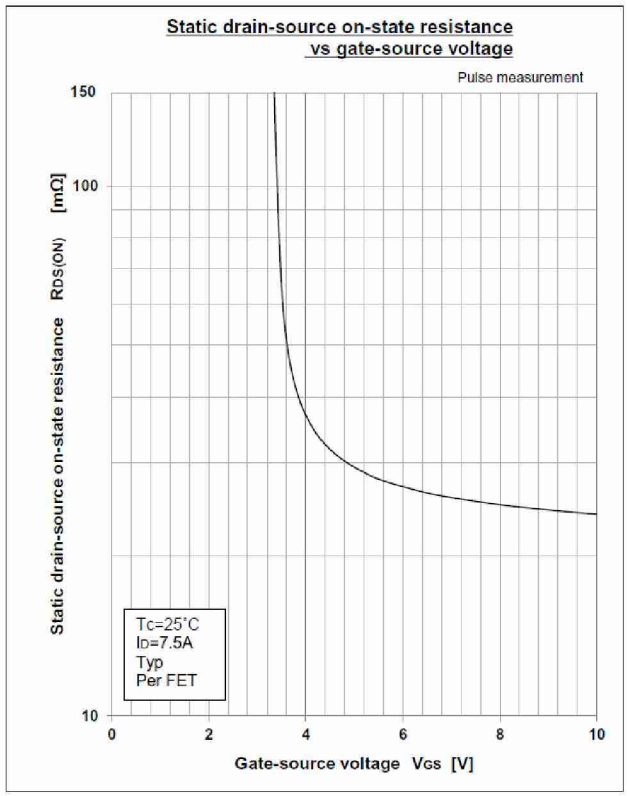


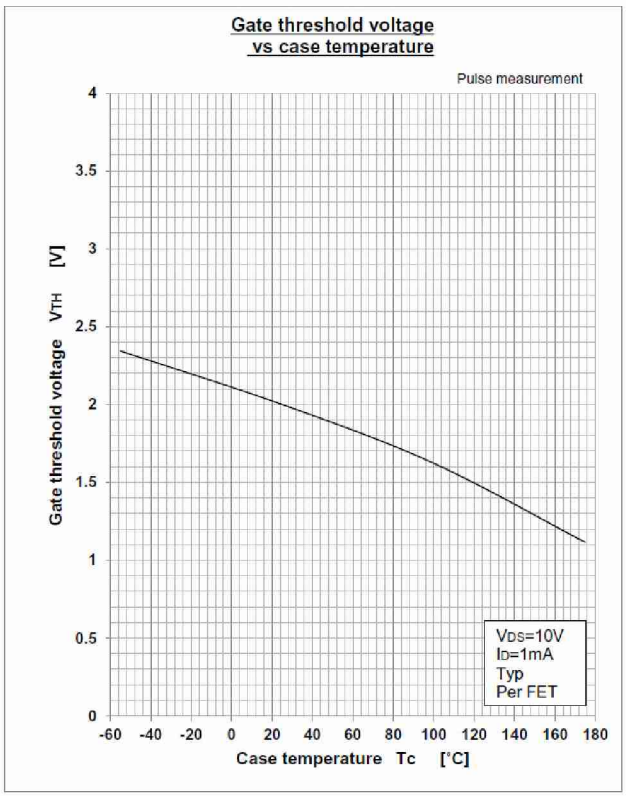


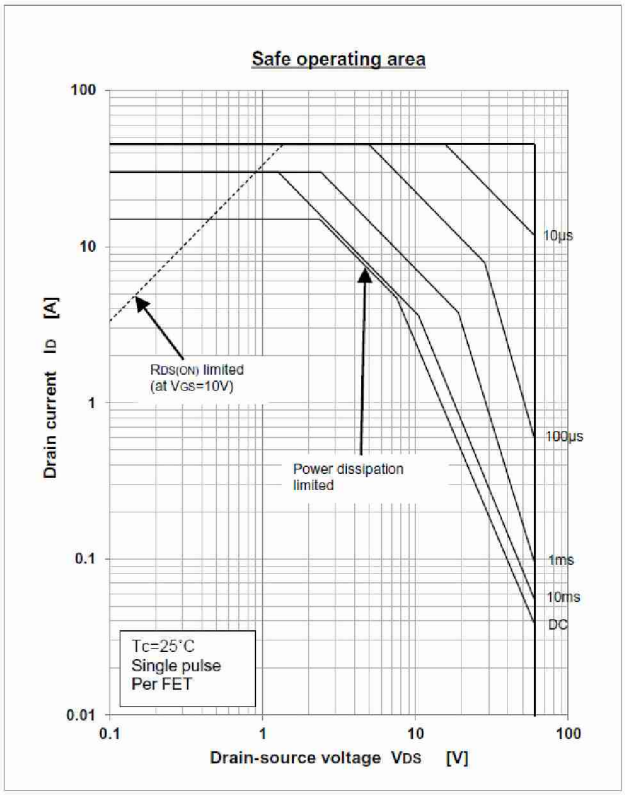


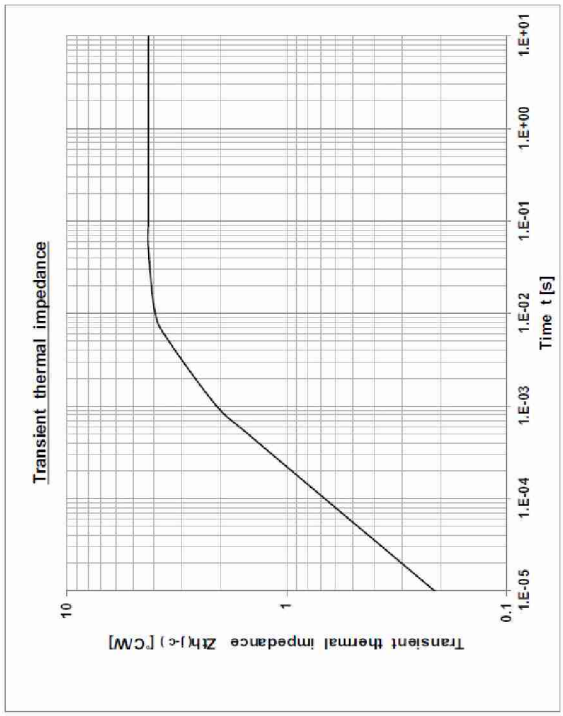



Static drain-source on-state resistance
vs case temperature
Pulse measurement
Static drain-source on-state resistance RDS(ON) [mΩ]
1000
100
10
1
-60 -40 -20 0 20 40 60 80 100 120 140 160 180
Case temperature Tc [°C]
VGS=10V
ID=7.5A
Typ
Per FET

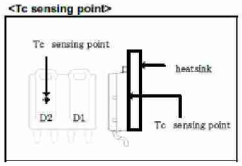

Static drain-source on-state resistance
vs gate-source voltage
Pulse measurement
Static drain-source on-state resistance RDS(ON) [mΩ]
150
100
10
0 2 4 6 8 10
Gate-source voltage VGS [V]
Tc=25°C
ID=7.5A
Typ
Per FET

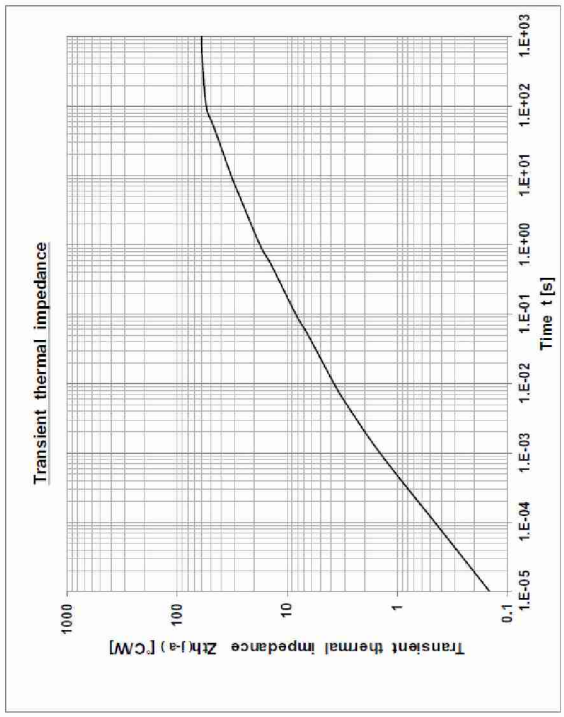

Gate threshold voltage
vs case temperature
Pulse measurement
Gate threshold voltage VTH [V]
4
3.5
3
2.5
2
1.5
1
0.5
0
-60 -40 -20 0 20 40 60 80 100 120 140 160 180
Case temperature Tc [°C]
VDS=10V
ID=1mA
Typ
Per FET


Safe operating area
Drain current ID [A]
100
10
1
0.1
0.01
0.1 1 10 100
Drain-source voltage VDS [V]
10μs
100μs
1ms
10ms
DC
RDS(ON) limited
(at VGS=10V)
Power dissipation
limited
Tc=25°C
Single pulse
Per FET



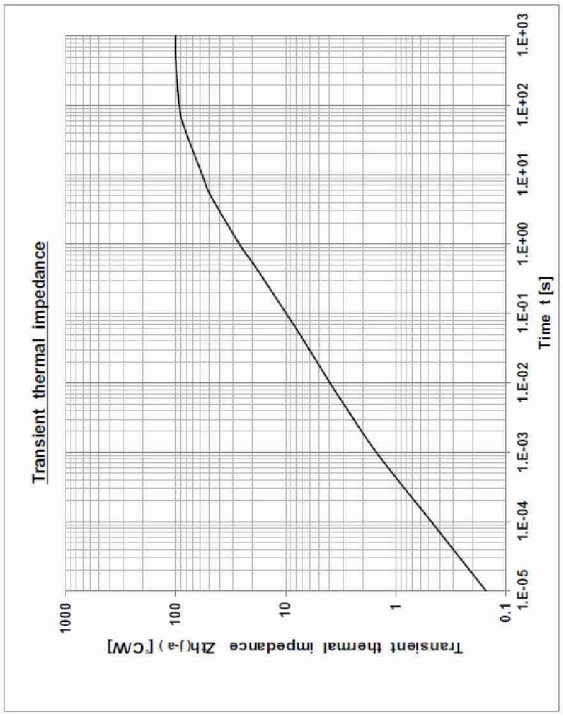
<Tc sensing point>





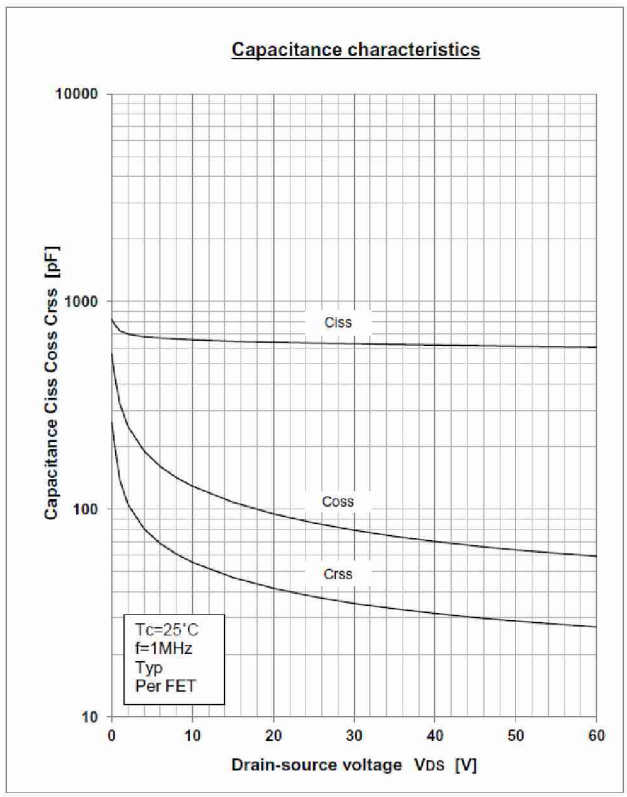
<Substrate detail>

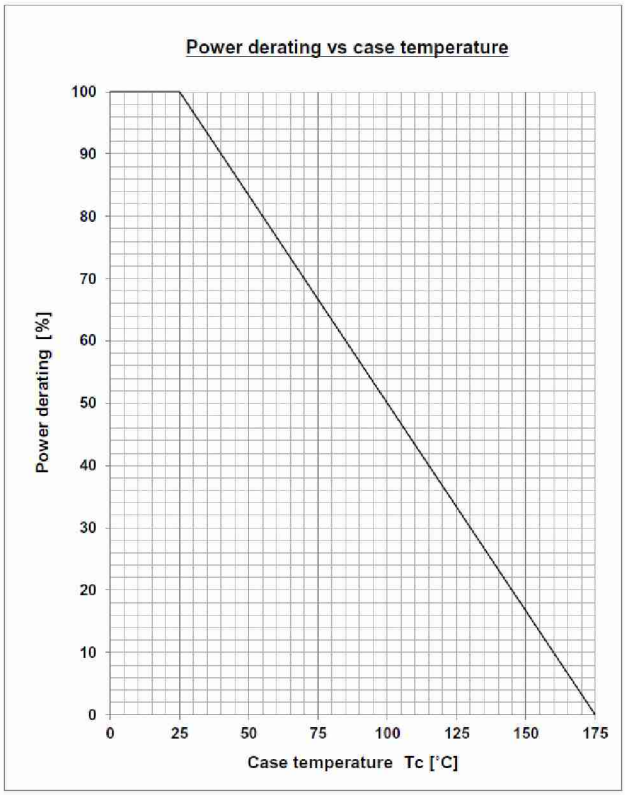
Type	Glass-epoxy
Size	1 inch^2
Thickness	1.6 mm
Conductor thickness	70 µm
Pattern area	629.42 mm^2

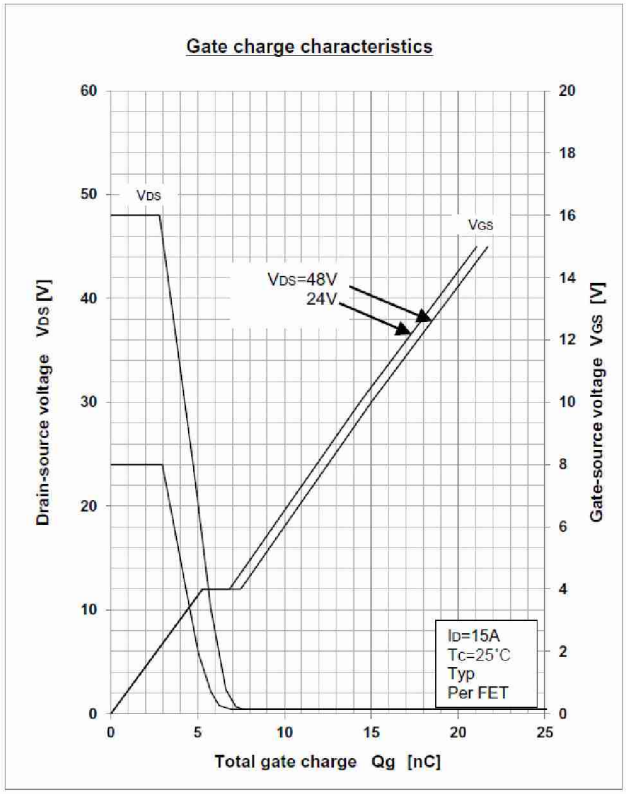


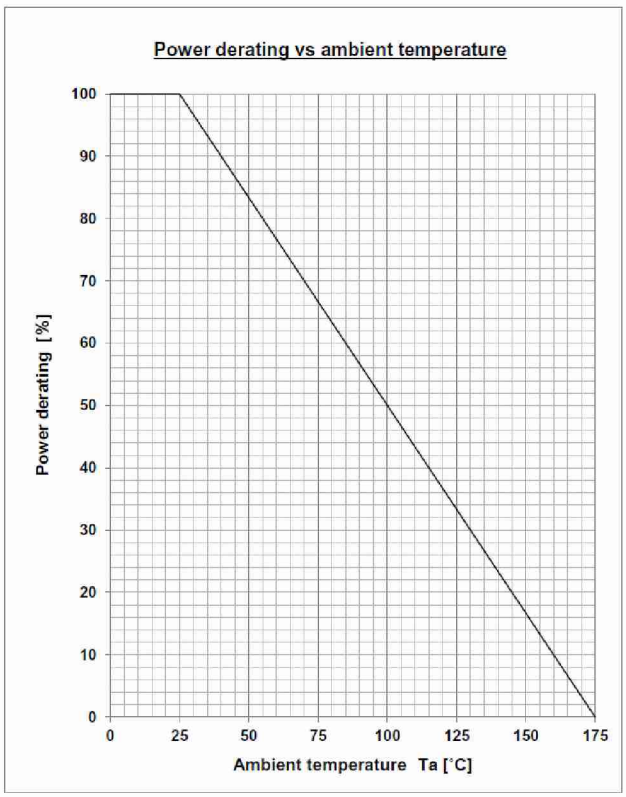
<Substrate detail>

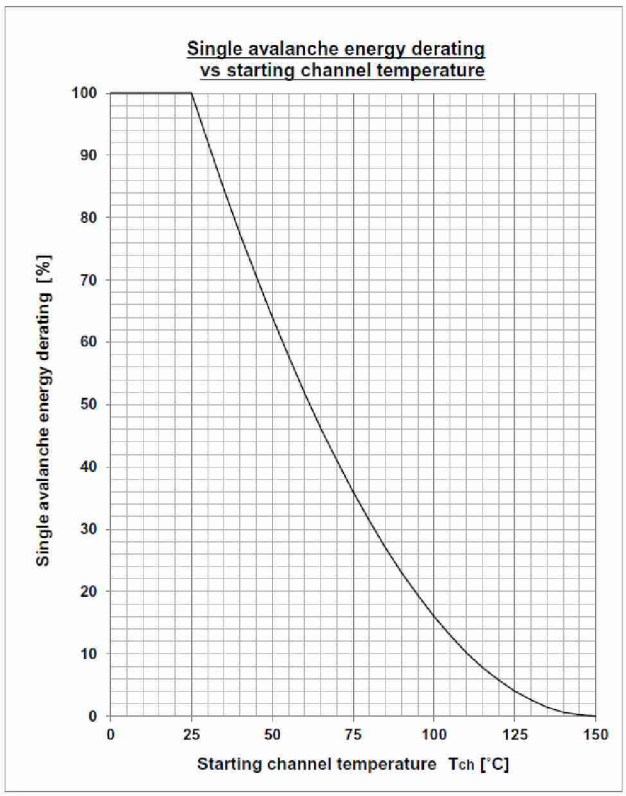
Type	Glass-epoxy
Size	1 inch^2
Thickness	1.6 mm
Conductor thickness	70 µm
Pattern area	91.34 mm^2




Power derating vs case temperature
Power derating [%]
Case temperature Tc [°C]
0
10
20
30
40
50
60
70
80
90
100
0
25
50
75
100
125
150
175


Gate charge characteristics
Drain-source voltage VDS [V]
Gate-source voltage VGS [V]
Total gate charge Qg [nC]
VDS
VGS
VDS=48V
24V
ID=15A
Tc=25°C
Typ
Per FET
0
10
20
30
40
50
60
0
2
4
6
8
10
12
14
16
18
20
0
5
10
15
20
25


Power derating vs ambient temperature
Power derating [%]
Ambient temperature Ta [°C]
0
10
20
30
40
50
60
70
80
90
100
0
25
50
75
100
125
150
175

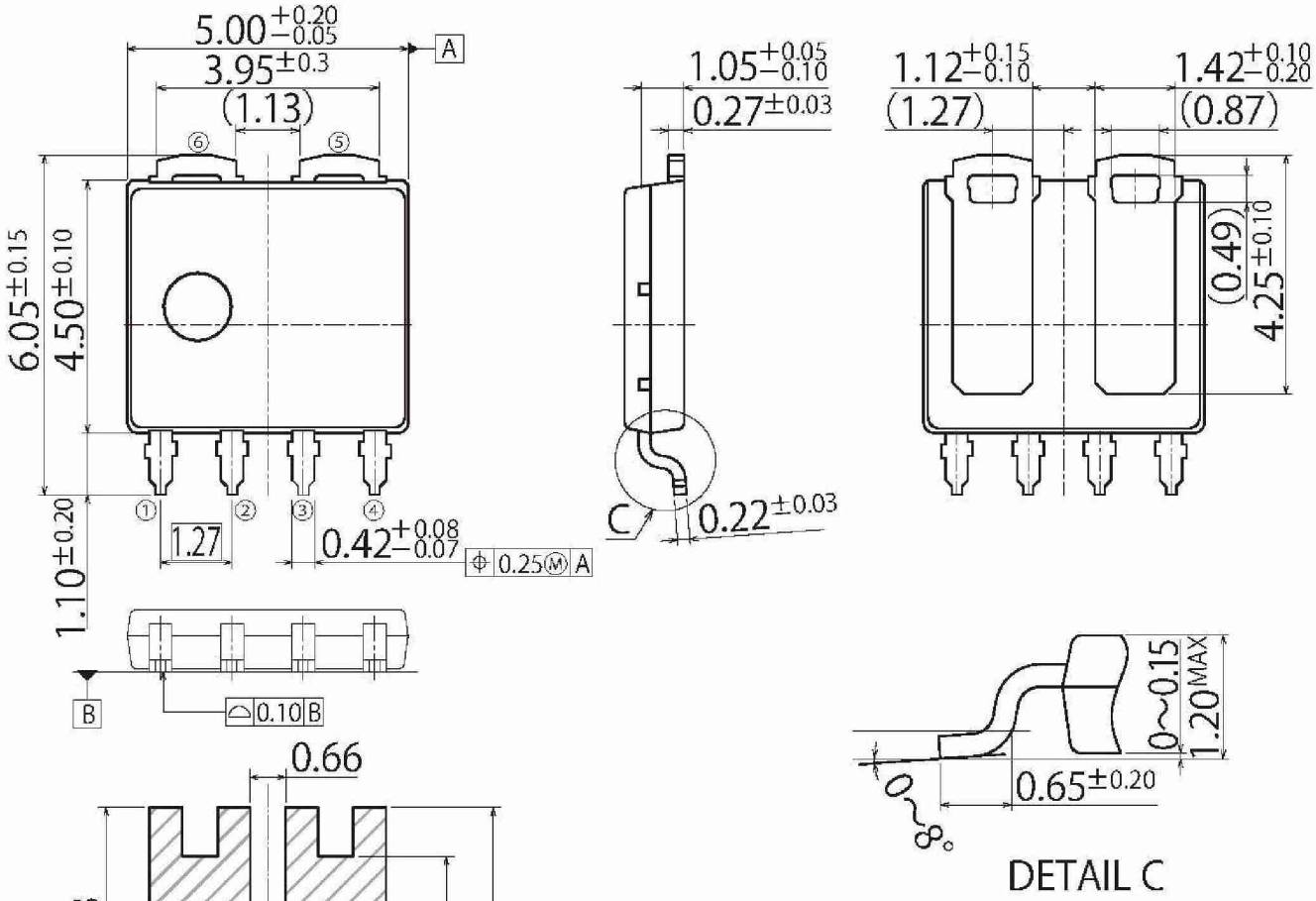

Single avalanche energy derating
vs starting channel temperature
Single avalanche energy derating [%]
Starting channel temperature Tch [°C]
0
10
20
30
40
50
60
70
80
90
100
0
25
50
75
100
125
150

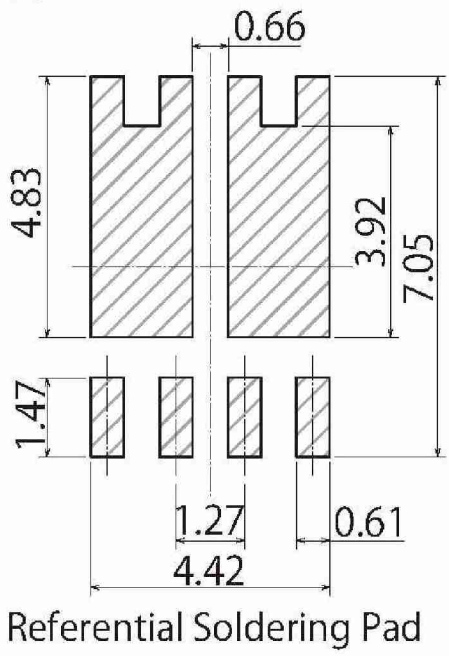
Outline Dimensions

unit:mm

G8

JEDEC Code	–
JEITA Code	–
House Name	LF_Dual





Referential Soldering Pad

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