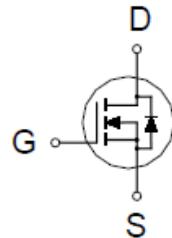
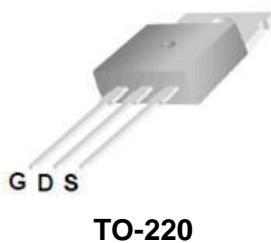


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N-Channel Enhancement Mode MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
110V	16mΩ @ $V_{GS} = 10V$	51A



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ²	I_D	51	A
		32	
Pulsed Drain Current ^{1,2}	I_{DM}	150	
Avalanche Current	I_{AS}	12	
Avalanche Energy	E_{AS}	72	mJ
Power Dissipation	P_D	96	W
		38	
Operating Junction & Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta JC}$	1.3	62.5	°C / W
Junction-to-Ambient	$R_{\theta JA}$			

¹Pulse width limited by maximum junction temperature.

²Limited only by maximum temperature allowed.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, Unless Otherwise Noted)

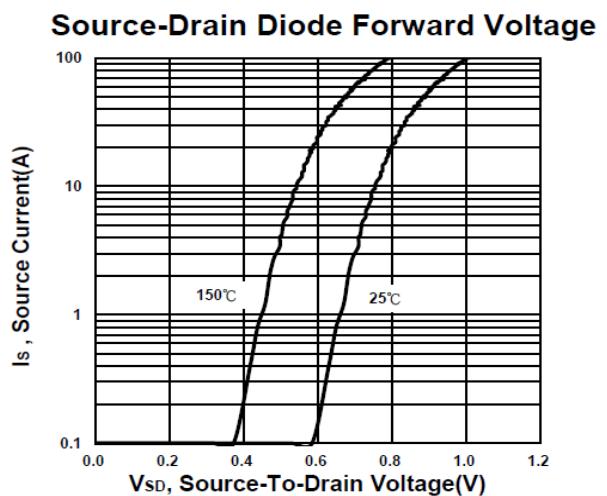
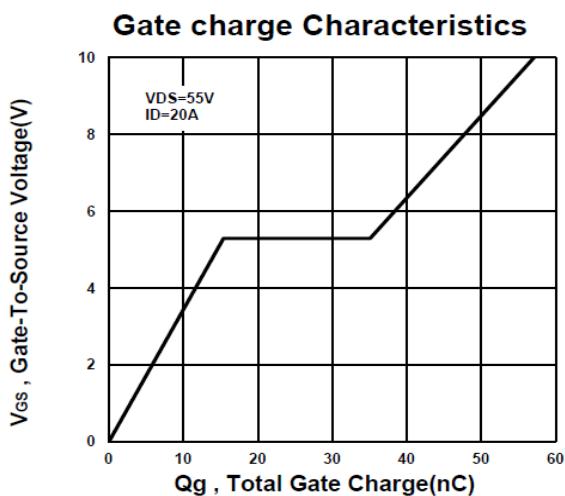
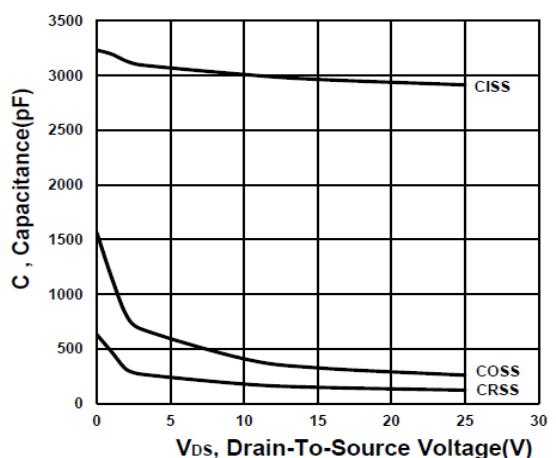
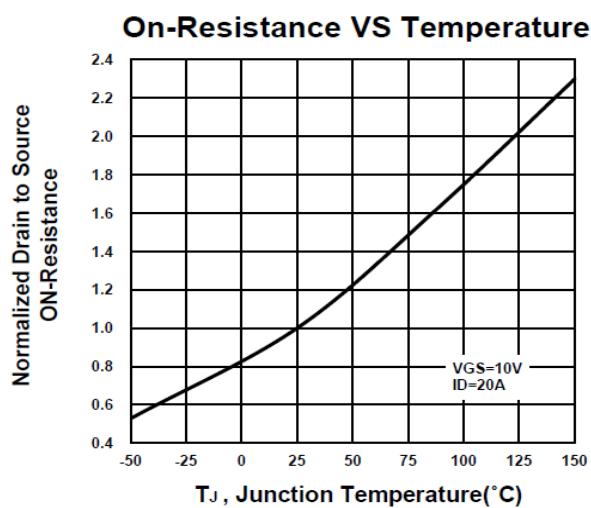
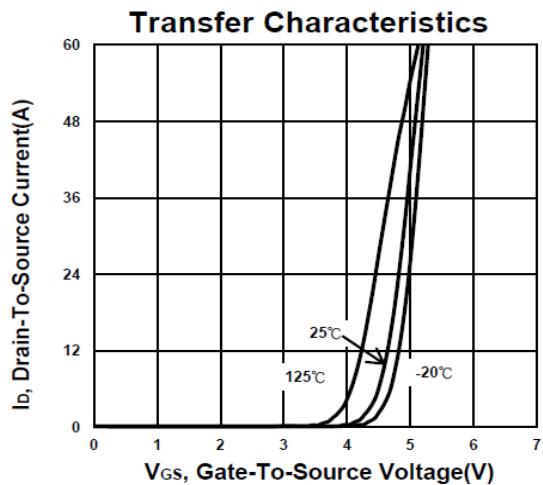
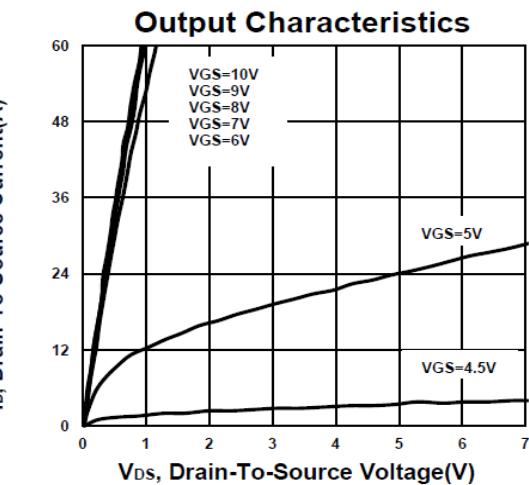
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$	110			V
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}, I_D = 250\mu\text{A}$	2	3.2	4	
Gate-Body Leakage	I_{GSS}	$V_{\text{DS}} = 0\text{V}, V_{\text{GS}} = \pm 20\text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = 88\text{V}, V_{\text{GS}} = 0\text{V}$			1	μA
		$V_{\text{DS}} = 80\text{V}, V_{\text{GS}} = 0\text{V}, T_J = 125^\circ\text{C}$			10	
Drain-Source On-State Resistance ¹	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}} = 7\text{V}, I_D = 15\text{A}$		14	21	$\text{m}\Omega$
		$V_{\text{GS}} = 10\text{V}, I_D = 20\text{A}$		13	16	
Forward Transconductance ¹	g_{fs}	$V_{\text{DS}} = 10\text{V}, I_D = 20\text{A}$		80		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 25\text{V}, f = 1\text{MHz}$		3009		pF
Output Capacitance	C_{oss}			258		
Reverse Transfer Capacitance	C_{rss}			152		
Gate Resistance	R_g	$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 0\text{V}, f = 1\text{MHz}$		0.81		Ω
Total Gate Charge ²	Q_g	$V_{\text{DS}} = 55\text{V}, V_{\text{GS}} = 10\text{V}, I_D = 20\text{A}$		57		nC
Gate-Source Charge ²	Q_{gs}			15.8		
Gate-Drain Charge ²	Q_{gd}			20		
Turn-On Delay Time ²	$t_{d(\text{on})}$	$V_{\text{DD}} = 55\text{V}, I_D \approx 20\text{A}, V_{\text{GS}} = 10\text{V}, R_{\text{GEN}} = 6\Omega$		47		nS
Rise Time ²	t_r			88		
Turn-Off Delay Time ²	$t_{d(\text{off})}$			86		
Fall Time ²	t_f			83		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_J = 25^\circ\text{C}$)						
Continuous Current	I_S				51	A
Forward Voltage ¹	V_{SD}	$I_F = 20\text{A}, V_{\text{GS}} = 0\text{V}$			1.2	V
Reverse Recovery Time	t_{rr}	$I_F = 20\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$		37		nS
Reverse Recovery Charge	Q_{rr}			50		nC

¹Pulse test : Pulse Width $\leq 300\ \mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

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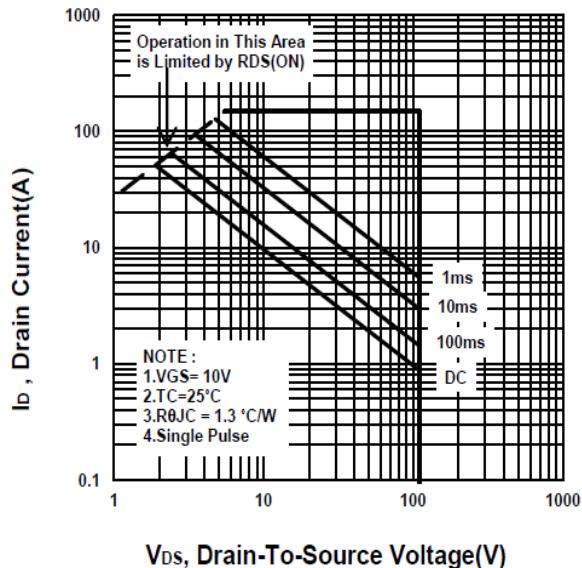
N-Channel Enhancement Mode MOSFET



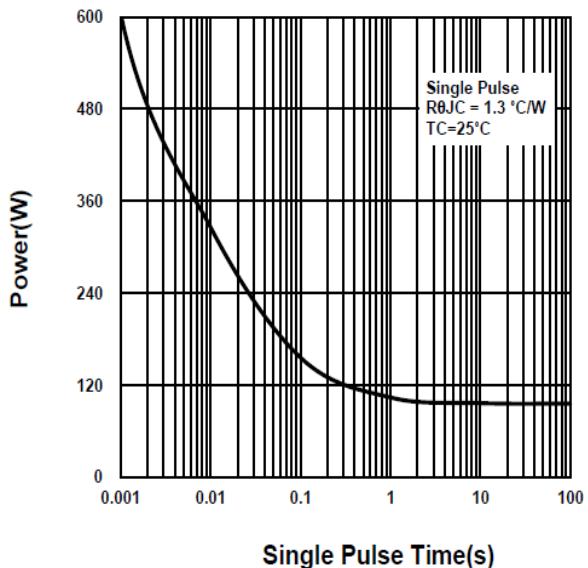
P1610AT

N-Channel Enhancement Mode MOSFET

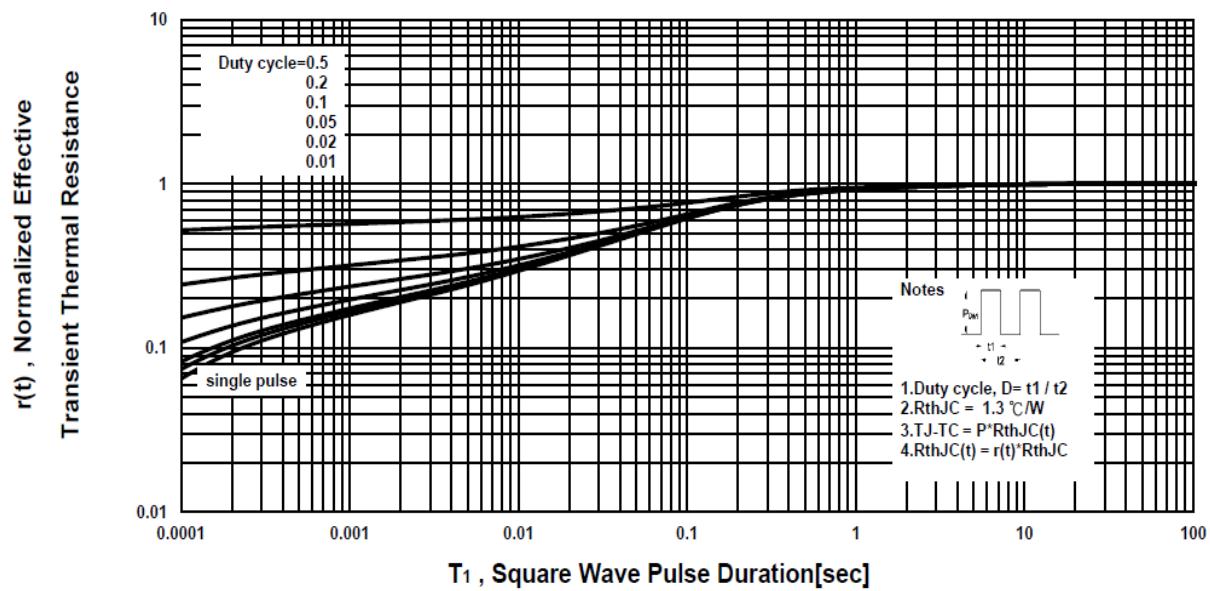
Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve



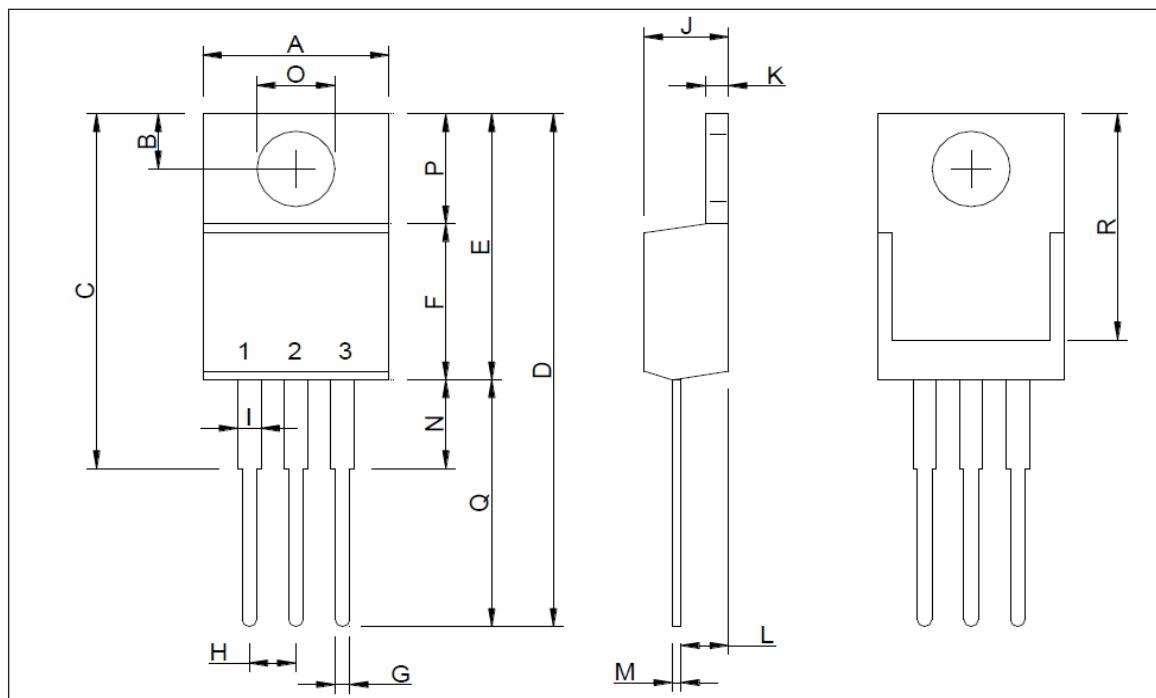
P1610AT

N-Channel Enhancement Mode MOSFET

Package Dimension

TO-220 (3-Lead) MECHANICAL DATA

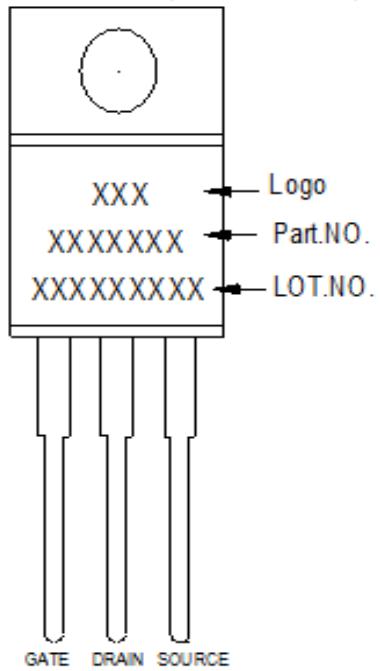
Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	9.65		11.5	J	3.55		4.83
B		2.54		K	1.11		1.45
C	18.1		22.86	L	1.89		3.09
D	26.9		31.24	M	0.34		0.61
E	14.32		16.51	N	2.6		4.06
F	8.38		9.3	O		3.7	
G	0.38		1.02	P	5.84		6.85
H	2.04	2.54	3.04	Q	12.5		14.73
I	1.14		1.8	R	11.3		13.31



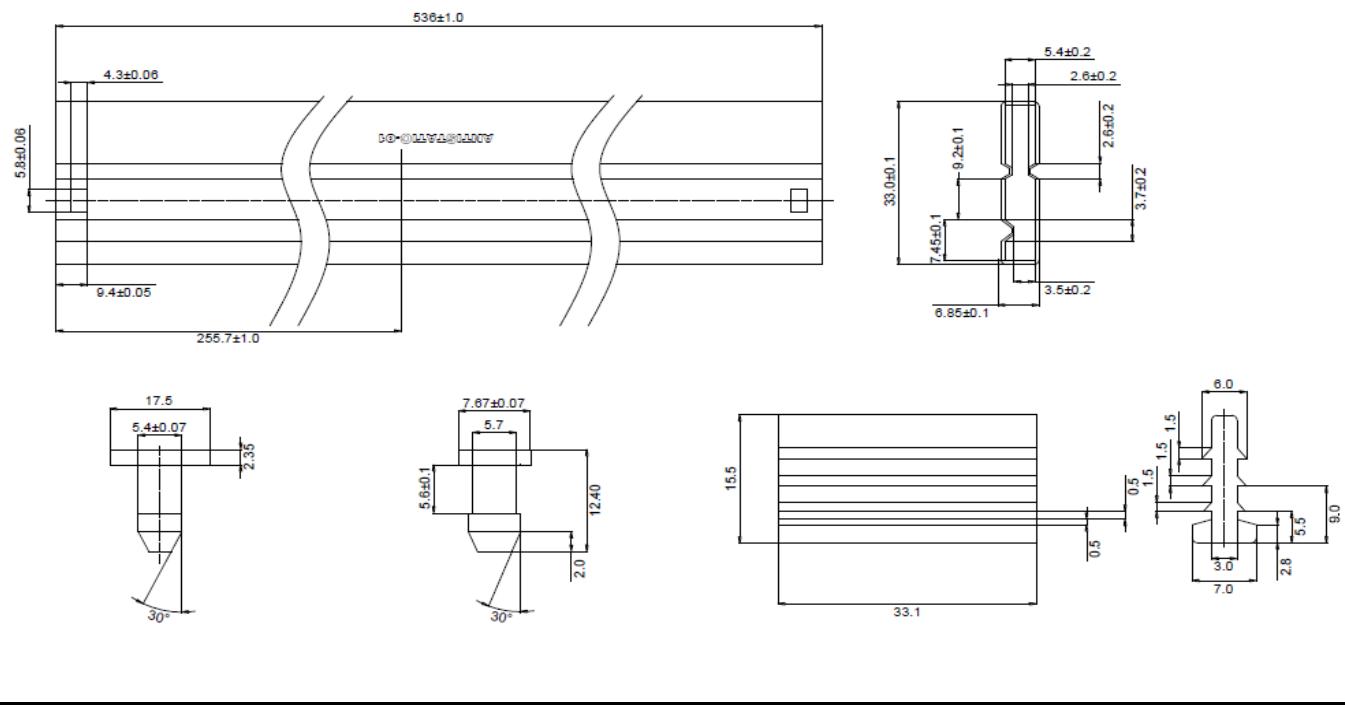
P1610AT

N-Channel Enhancement Mode MOSFET

A. Marking Information



B. Tape&Reel Information: 50pcs/Tube



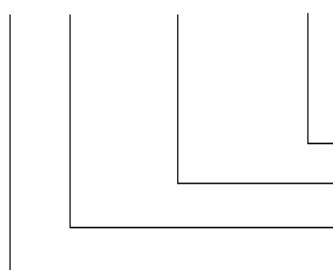
P1610AT

N-Channel Enhancement Mode MOSFET

C. Lot.No. & Date Code rule

1.LOT.NO.

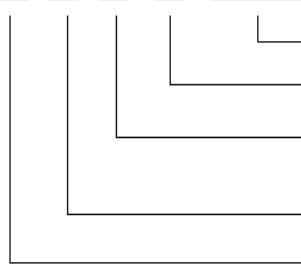
M N 15M21 03



- #8~9 Sub-lot No
- Order series no.
- Foundry site
- Assembly site

2.Date Code

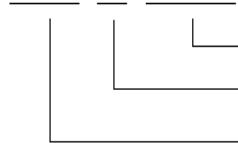
D Y M X XXX



- Order series no. & Sub-lot No
- Week
- M : Month (A:Jan , B:Feb , C:Mar ,D :Apr ,E:May ,F:Jun,G:Jul,H:Aug,I:Sep,J:Oct,K:Nov,L:Dec.)
- Y : Year (N : 2011, O : 2012 ...)
- Assembly site

3.Date Code (for Small package)

XX Y WW



- Week
- Y : Year (9: 2009,A : 2010, B : 2011 ...)
- Device Name

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D.Label rule

标签内容(Label content)



1	Label Size	30 * 90 mm
2	Font style	Times New Roman or Arial (或可区分英文“0”和数字“0”，“G”和“Q”的字型即可)
3	Great Power	Height: 4 mm
4	Package	Height: 2 mm
5	Date	Height: 2 mm Shipping date: YYYY/MM/DD, ex. 2008/09/12
6	Device	Height: 3 mm (Max: 16 Digit)
7	Lot	Height: 3 mm (Max: 9 Digit) Sub lot
8	D/C	Height: 3 mm (Max: 7 Digit)
9	QTY	Height: 3 mm (Max: 6 Digit) Thousand mark is no needed
10	Pb Free label	 Diameter: 1 cm bottom color: Green Font color: Black Font style: Arial
11	Halogen Free label	 Diameter: 1 cm bottom color: Green Font color: Black Font style: Arial
12	Scan info	Device / Lot / D/C / QTY , Insert “ / ” between every parts. for example: P3055LDG/G12345601/GGG2301/2000 DPI (Dots per inch): Over 300 dpi Code : Code 128 Height: 6 mm at least