

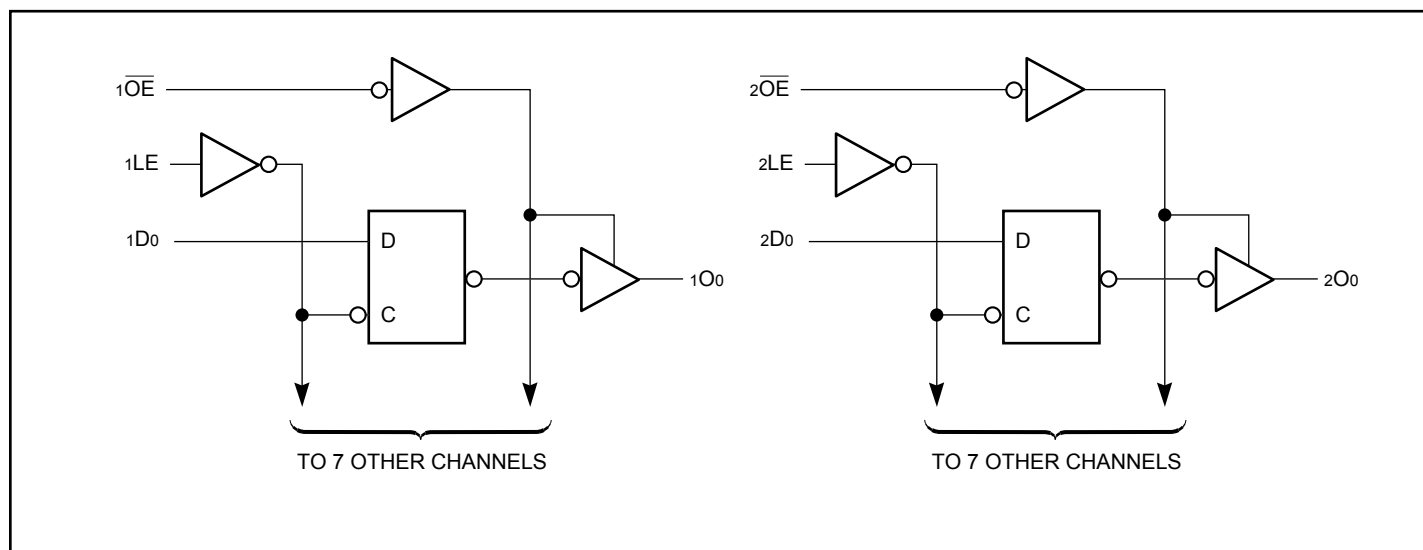
**Fast CMOS 3.3V 16-Bit
Transparent Latch**
Features

- Compatible with LCX[™] and LVT[™] families of products
- Supports 5V Tolerant Mixed Signal Mode Operation
 - Input can be 3V or 5V
 - Output can be 3V or connected to 5V bus
- Advanced Low Power CMOS Operation
- Excellent output drive capability:
Balanced drives (24 mA sink and source)
- Pin compatible with industry standard double-density pinouts
- Low ground bounce outputs
- Hysteresis on all inputs
- Industrial operating temperature range: -40°C to +85°C
- Multiple center pins and distributed Vcc/GND pins minimize switching noise
- Packaging:
 - 48-pin 240-mil wide thin plastic TSSOP (A)
 - 48-pin 300-mil wide plastic SSOP (V)

Description

Pericom Semiconductor's PI74LPT16373 is a 16-bit transparent latch designed with 3-state outputs and are intended for bus oriented applications. The Output Enable and Latch Enable controls are organized to operate as two 8-bit latches or one 16-bit latch. When Latch Enable (LE) is HIGH, the flip-flops appear transparent to the data. The data that meets the set-up time when LE is LOW is latched. When OE is HIGH, the bus output is in the high impedance state.

The PI74LPT16373 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

Block Diagram


Maximum Ratings

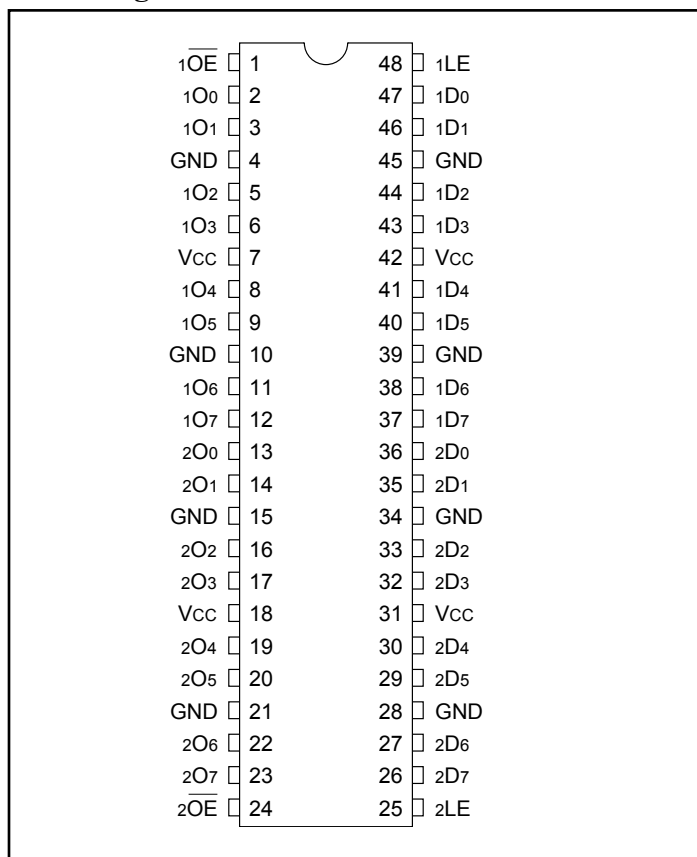
(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & V _{CC} Only).....	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only) ...	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current.....	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Pin Configuration



Truth Table

Inputs ⁽¹⁾			Outputs ⁽¹⁾
xDx	xLE	xOE	xOx
H	H	L	H
L	H	L	L
X	X	H	Z

Note:

1. H = High Voltage Level, X = Don't Care, L = Low Voltage Level, Z = High Impedance

Pin Description

Pin Name	Description
\overline{xOE}	3-State Output Enable Inputs (Active LOW)
xLE	Latch Enable Inputs (Active HIGH)
xDx	Data Inputs
xOx	3-State Outputs
GND	Ground
V _{CC}	Power

Capacitance ($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

Parameters ⁽¹⁾	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	4.5	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	5.5	8	

Note:

1. This parameter is determined by device characterization but is not production tested.

DC Electrical Characteristics (Over the Operating Range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 2.7V$ to $3.6V$)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
V_{IH}	Input HIGH Voltage (Input pins)	Guaranteed Logic HIGH Level		2.2	—	5.5	V
	Input HIGH Voltage (I/O pins)			2.0	—	5.5	
V_{IL}	Input LOW Voltage (Input and I/O pins)	Guaranteed Logic LOW Level		-0.5	—	0.8	
I_{IH}	Input HIGH Current (Input pins)	$V_{CC} = \text{Max.}$	$V_{IN} = 5.5V$	—	—	± 1	μA
	Input HIGH Current (I/O pins)	$V_{CC} = \text{Max.}$	$V_{IN} = V_{CC}$	—	—	± 1	
I_{IL}	Input LOW Current (Input pins)	$V_{CC} = \text{Max.}$	$V_{IN} = \text{GND}$	—	—	± 1	
	Input LOW Current (I/O pins)	$V_{CC} = \text{Max.}$	$V_{IN} = \text{GND}$	—	—	± 1	
I_{OZH}	High Impedance Output Current	$V_{CC} = \text{Max.}$	$V_{OUT} = 5.5V$	—	—	± 1	
I_{OZL}	(3-State Output pins)	$V_{CC} = \text{Max.}$	$V_{OUT} = \text{GND}$	—	—	± 1	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
I_{ODH}	Output HIGH Current	$V_{CC} = 3.3V, V_{IN} = V_{IH}$ or $V_{IL}, V_O = 1.5V^{(3)}$		-36	-60	-110	mA
I_{ODL}	Output LOW Current	$V_{CC} = 3.3V, V_{IN} = V_{IH}$ or $V_{IL}, V_O = 1.5V^{(3)}$		50	90	200	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$	$I_{OL} = -0.1\text{ mA}$	$V_{CC}-0.2$	—	—	V
		$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = -3\text{ mA}$	2.4	3.0	—	
		$V_{CC} = 3.0V,$	$I_{OL} = -8\text{ mA}$	2.4 ⁽⁵⁾	3.0	—	
		$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = -24\text{ mA}$	2.0	—	—	
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$	$I_{OL} = 0.1\text{ mA}$	—	—	0.2	
		$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 16\text{ mA}$	—	0.2	0.4	
			$I_{OL} = 24\text{ mA}$	—	0.3	0.5	
I_{OS}	Short Circuit Current ⁽⁴⁾	$V_{CC} = \text{Max.}^{(3)}, V_{OUT} = \text{GND}$		-60	-85	-240	mA
I_{OFF}	Power Down Disable	$V_{CC} = 0V, V_{IN}$ or $V_{OUT} \leq 4.5V$		—	—	± 100	μA
V_H	Input Hysteresis			—	150	—	mV

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 3.3V$, $+25^\circ\text{C}$ ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. $V_{OH} = V_{CC} - 0.6V$ at rated current.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	10	μA
ΔI _{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max.	V _{IN} = V _{CC} - 0.6V ⁽³⁾			500	
I _{CCD}	Dynamic Power Supply ⁽⁴⁾	V _{CC} = Max., Outputs Open x \overline{OE} = GND xLE = V _{CC} One Bit Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		50	75	μA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle x \overline{OE} = GND One Bit Toggling	V _{IN} = V _{CC} - 0.6V V _{IN} = GND		0.6 xLE = V _{CC}	2.3	mA
		V _{CC} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle x \overline{OE} = GND 16 Bits Toggling	V _{IN} = V _{CC} - 0.6V V _{IN} = GND		2.1 xLE = V _{CC}	4.7 ⁽⁵⁾	

Notes:

- For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 3.3V, +25°C ambient.
- Per TTL driven input; all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current (I}_{CCL}, I_{CCCH} \text{ and } I_{CCZ})$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input}$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$
 All currents are in milliamps and all frequencies are in megahertz.

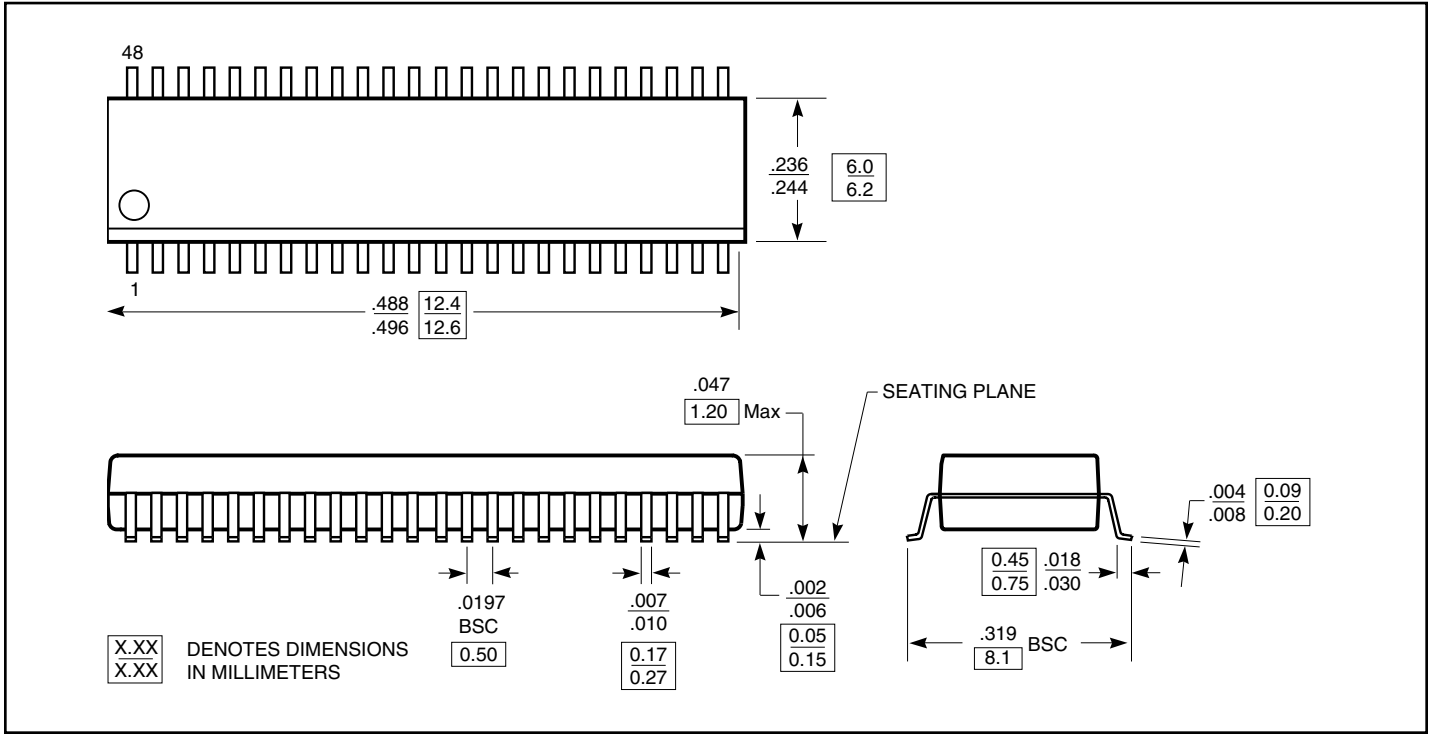
Switching Characteristics over Operating Range⁽¹⁾

Parameters	Description	Conditions ⁽²⁾	LPT16373		LPT16373A		LPT16373C		Units
			Com.		Com.		Com.		
			Min ⁽³⁾	Max	Min ⁽³⁾	Max	Min ⁽³⁾	Max	
t _{PLH} t _{PHL}	Propagation Delay xDx to xOx	C _L = 50pF R _L = 500Ω	1.5	7.0	1.5	5.2	1.5	4.2	ns
t _{PLH} t _{PHL}	Propagation Delay xLE to xOx		2.0	7.0	2.0	6.5	2.0	5.5	
t _{PZH} t _{PZL}	Output Enable Time xOE to xOx		1.5	7.2	1.5	6.5	1.5	5.5	
t _{PHZ} t _{PLZ}	Output Disable Time ⁽⁴⁾ xOE to xOx		1.5	7.2	1.5	5.5	1.5	5.0	
t _{SU}	Setup Time HIGH or LOW, xDx to xLE		2.0		2.0		2.0		
t _H	Hold Time HIGH or LOW, xDx to xLE		1.5		1.5		1.5		
t _w	xLE Pulse Width ⁽⁴⁾ HIGH		6.0		5.0		5.0		
t _{SK(o)}	Output Skew ⁽⁵⁾		0.5		0.5		0.5		

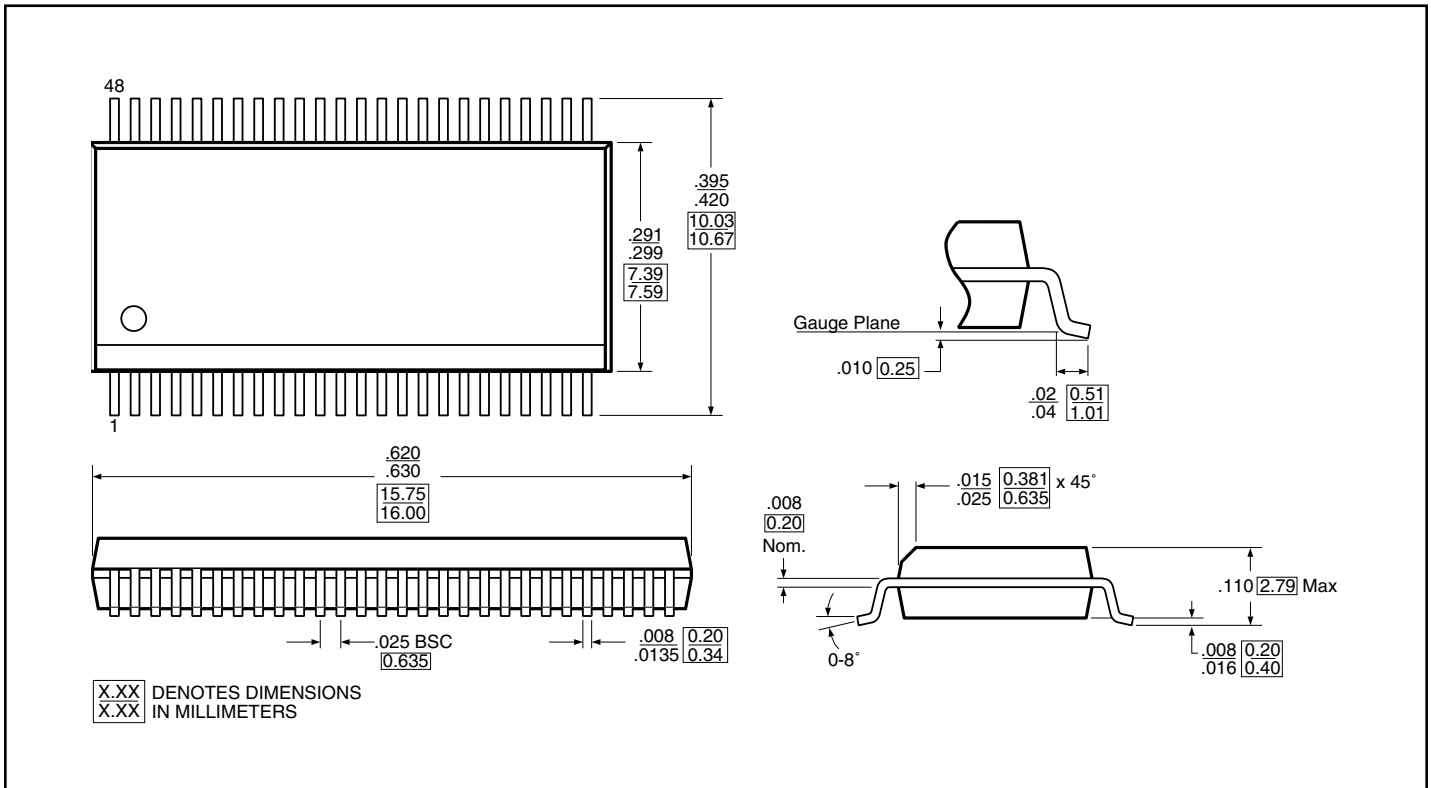
Notes:

1. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
2. See test circuit and waveforms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.
4. This parameter is guaranteed but not production tested.
5. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Packaging Mechanical: 48-pin TSSOP (L)



Packaging Mechanical: 48-pin SSOP (V)



Ordering Information

Ordering Code	Package Code	Speed Grade	Description
PI74LPT16373A	A	Blank	48-pin 173 mil wide plastic TSSOP
PI74LPT16373AA	A	A	48-pin 173 mil wide plastic TSSOP
PI74LPT16373AV	V	A	48-pin 300 mil wide plastic SSOP
PI74LPT16373CA	A	C	48-pin 173 mil wide plastic TSSOP
PI74LPT16373CV	V	C	48-pin 300 mil wide plastic SSOP

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/