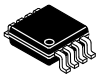
P1817A, P1817B

Product Preview

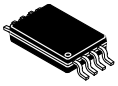
Low-Power Mobile VGA EMI Reduction IC

ON Semiconductor®

http://onsemi.com

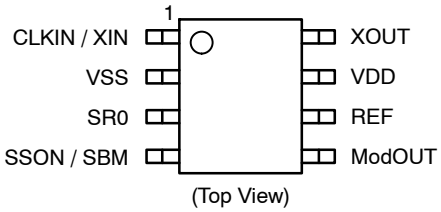


SOIC−8
S SUFFIX
CASE 751BD



TSSOP−8
T SUFFIX
CASE 948AL

PIN CONFIGURATION



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

Description

The P1817 is a versatile spread spectrum frequency modulator designed specifically for input clock frequencies. The P1817 reduces electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of down stream clock and data dependent signals. The P1817 allows significant system cost savings by reducing the number of circuit board layers, ferrite beads, shielding and other passive components that are traditionally required to pass EMI regulations.

The P1817 modulates the output of a single PLL in order to “spread” the bandwidth of a synthesized clock, and more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal’s bandwidth is called ‘spread spectrum clock generation.’

The P1817 uses the most efficient and optimized modulation profile approved by the FCC and is implemented in a proprietary all digital method.

Applications

The P1817 is targeted towards notebook LCD displays, and other displays using an LVDS interface, PC peripheral devices, and embedded systems.

Features

- FCC Approved Method of EMI Attenuation
- Generates a Low EMI Spread Spectrum Clock of the Input Frequency
- Optimized for Frequency Range from:
  - P1817A – 20 to 32 MHz
  - P1817B – 10 to 20 MHz
- Internal Loop Filter Minimizes External Components and Board Space
- Two Selectable Spread Ranges
- Low Inherent Cycle−to−Cycle Jitter
- 3.3 V or 5 V Operating Voltage Range
- TTL or CMOS Compatible Inputs and Outputs
- Ultra−low Power CMOS Design
  - 3.17 mA @ 3.3 V, 10 MHz | 6.20 mA @ 5.0 V, 10 MHz
  - 4.28 mA @ 3.3 V, 14 MHz | 7.50 mA @ 5.0 V, 14 MHz
  - 5.50 mA @ 3.3 V, 20 MHz | 9.50 mA @ 5.0 V, 20 MHz
- Supports Notebook VGA and Other LCD Timing Controller Applications
- SSON / SBM Pin for Spread Spectrum On/Off and Standby Mode Controls
- Available in 8−pin SOIC and TSSOP
- These are Pb−Free Devices

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

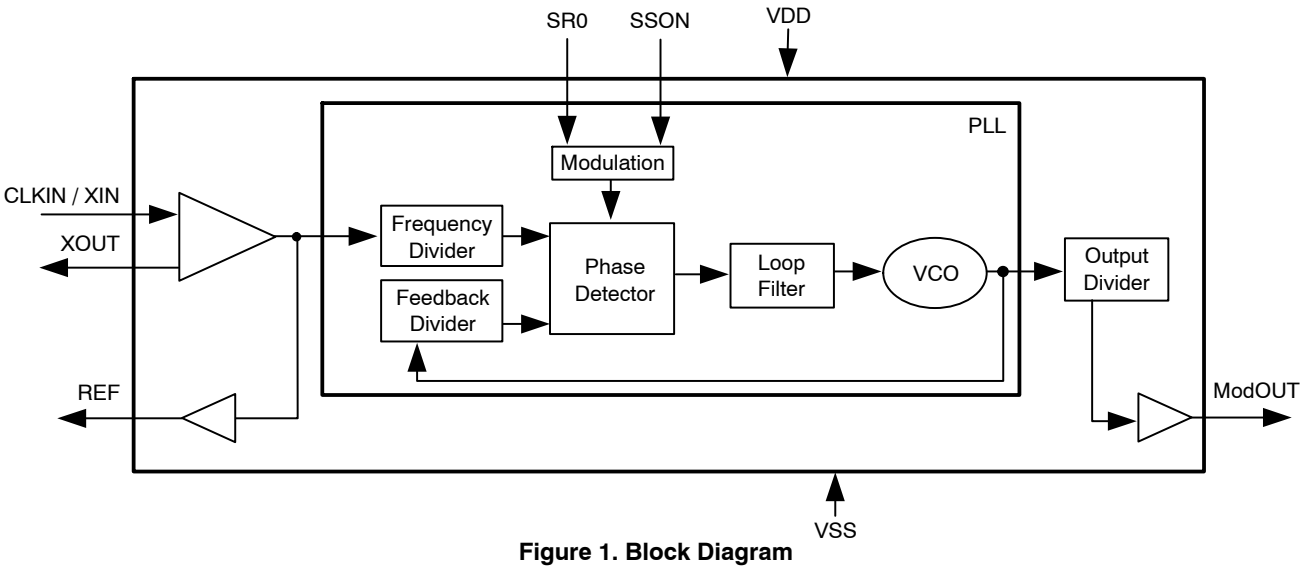


Figure 1. Block Diagram

Table 1. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
VDD, V_{IN}	Voltage on any pin with respect to GND	−0.5 to +7.0	V
T_{STG}	Storage temperature	−65 to +125	°C
T_A	Operating temperature	0 to 70	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22− A114−B)	2	KV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 2. DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Min	Typ	Max	Unit
V_{IL}	Input low voltage		GND−0.3	−	0.8	V
V_{IH}	Input high voltage		2.0	−	VDD+0.3	V
I_{IL}	Input low current (pull−up resistors on inputs SR0, and SSON / SBM)		−	−	−35	μA
I_{IH}	Input high current (pull−down resistors on inputs SR0, and SSON / SBM)		−	−	35	μA
I_{XOL}	X_{OUT} output low current	@ 0.4 V, VDD = 3.3 V	−	3	−	mA
		@ 0.4 V, VDD = 5.0 V		20		
I_{XOH}	X_{OUT} output high current	@ 2.5 V, VDD = 3.3 V	−	3	−	mA
		@ 4.5 V, VDD = 5.0 V		20		
V_{OL}	Output low voltage	VDD = 3.3 V, I_{OL} = 20 mA	−	−	0.4	V
		VDD = 5.0 V, I_{OL} = 20 mA	−			
V_{OH}	Output high voltage	VDD = 3.3 V, I_{OH} = 20 mA	2.5	−	−	V
		VDD = 5.0 V, I_{OH} = 20 mA	4.5			
I_{CC}	Dynamic supply current standby mode	Normal Mode	f_{IN-min}	f_{IN-typ}	f_{IN-max}	mA
		3.3 V and 10 pF loading	3.2	−	7.0	
		5.0 V and 10 pF loading	6.2	−	13.6	
I_{DD}	Static supply current standby mode		−	0.6	−	mA
VDD	Operating voltage		2.7	3.3	5.5	V
t_{ON}	Power up time (first locked clock cycle after power up)		−	0.18	−	mS
Z_{OUT}	Clock output impedance		−	50	−	Ω

Table 3. AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Min	Typ	Max	Unit
f_{IN}	Input frequency (See device type P1817A or 1817B)		10	–	32	MHz
f_{OUT}	Output frequency (See device type P1817A or 1817B)		10	–	32	MHz
t_{LH} (Note 1)	Output rise time	Measured at 0.8 V to 2.0 V	0.7	0.9	1.1	nS
		Measured at 1.2 V to 3.75 V	–	0.75	–	
t_{HL} (Note 1)	Output fall time	Measured at 0.8 V to 2.0 V	0.6	0.8	1.0	nS
		Measured at 1.2 V to 3.75 V	–	0.75	–	
t_{JC}	Jitter (cycle−to−cycle)		–	–	360	pS
t_D	Output duty cycle		45	50	55	%

1. t_{LH} and t_{HL} are measured into a capacitive load of 15 pF.

Table 4. PIN DESCRIPTION

Pin#	Pin Name	Type	Description
1	CLKIN / XIN	I	Crystal connection or external reference frequency input. This pin has dual functions. It can be connected either to an external crystal or an external reference clock. To put the part into standby mode, disable the input clock signal to this pin and pull SSON/SBM (pin4) low. Refer to *Standby Mode Selection* Table.
2	VSS	P	Ground Connection. Connect to system ground.
3	SR0	I	Digital logic input used to select Spreading Range. Refer to *Spread Spectrum Selection* Table. This pin has an internal pull−up resistor.
4	SSON / SBM	I	Spread Spectrum On/Off and standby mode control. Refer to *Standby Mode Selection* Table.
5	ModOUT	O	Spread spectrum clock output or Reference output. Refer to *Standby Mode Selection* Table.
6	REF	O	Reference Output.
7	VDD	P	Connect to +3.3 V or 5.0 V.
8	XOUT	O	Connect to crystal. No connect if externally generated clock signal is used.

Table 5. STANDBY MODE SELECTION

CLKIN	SSON / SBM	Spread Spectrum	ModOUT	PLL	Mode
Disabled	0	N/A	Disabled	Disabled	Standby
Disabled	1	N/A	Disabled	Free Running	Free Running
Enabled	0	OFF	Reference	Disabled	Buffer out
Enabled	1	ON	Normal	Normal	Normal

Table 6. SPREAD RANGE SELECTION, VDD = 5 V

CLKIN Frequency	SR0	Spreading Range	Modulation Rate
10 MHz	1	±1.50%	(CLKIN/10) * 20.83 KHz
	0	±1.90%	
14.318 MHz	1	±1.36%	
	0	±1.64%	
15 MHz	1	±1.30%	
	0	±1.50%	
20 MHz	1	±0.95%	
	0	±1.125%	

Table 7. SPREAD RANGE SELECTION, VDD = 3.3 V

CLKIN Frequency	SR0	Spreading Range	Modulation Rate
10 MHz	1	±1.50%	(CLKIN/10) * 20.83 KHz
	0	±1.65%	
14.318 MHz	1	±1.40%	
	0	±1.70%	
15 MHz	1	±1.37%	
	0	±1.63%	
20 MHz	1	±1.10%	
	0	±1.28%	

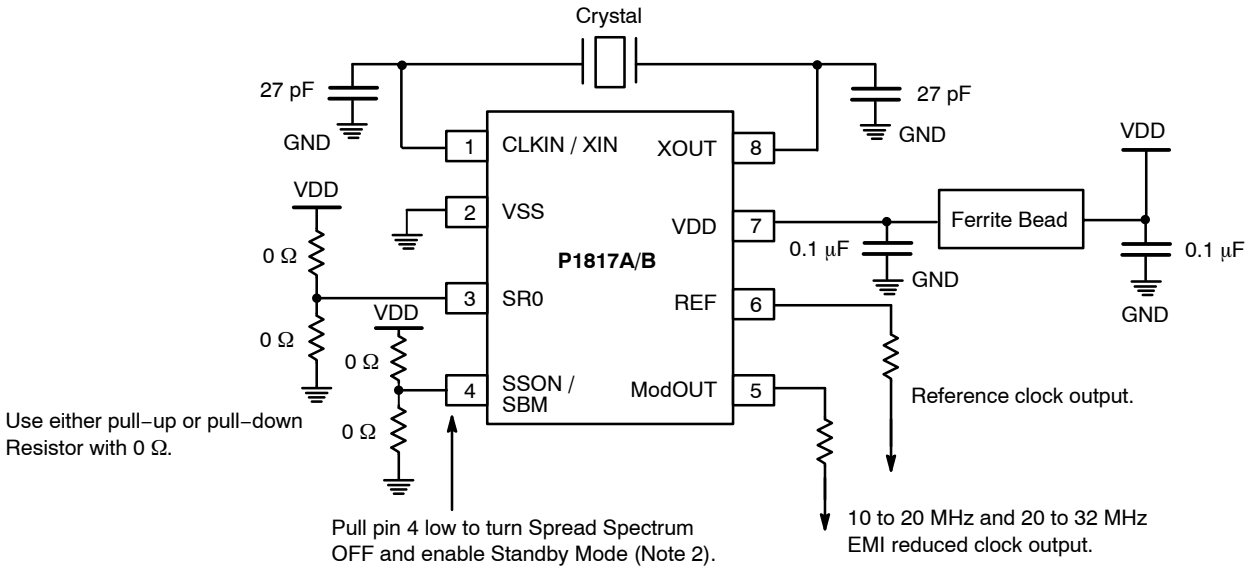
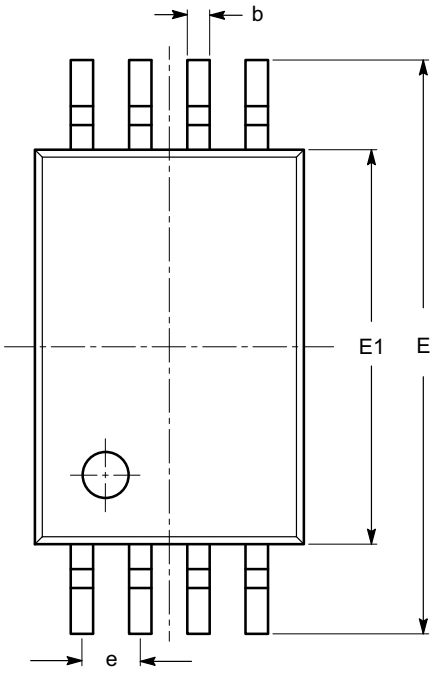


Figure 2. Schematic for Notebook VGA Application

2. To set the P1817 to standby mode, disable the input clock (pin 1, CLKIN) and pull pin 4 SSON / SBM low.

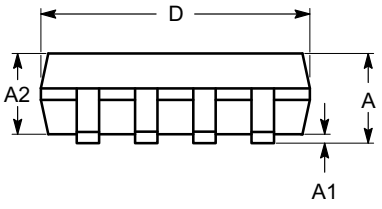
PACKAGE DIMENSIONS

TSSOP8, 4.4x3
CASE 948AL−01
ISSUE O

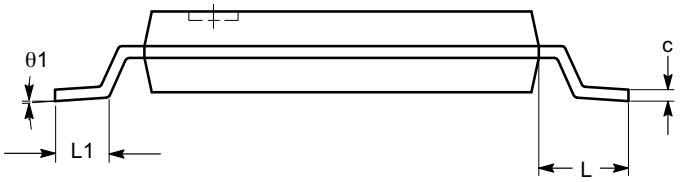


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0º		8º



SIDE VIEW



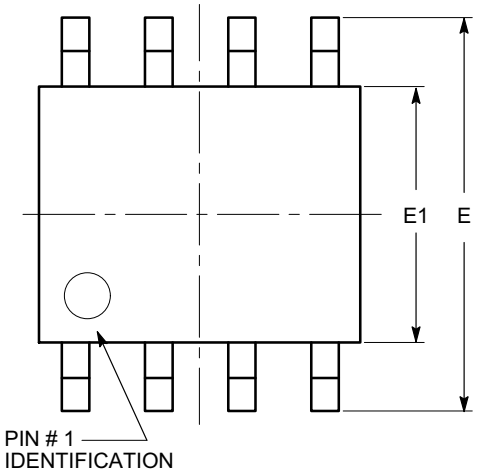
END VIEW

Notes:

(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

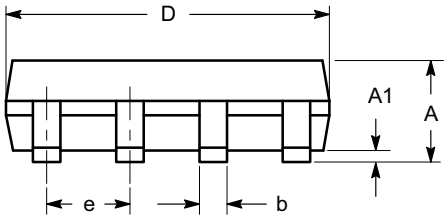
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD−01
ISSUE O

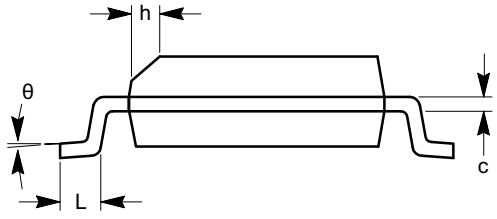


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

Table 8. ORDERING INFORMATION

Part Number	Marking	Input Frequency (MHz)	Package Type	Temperature (°C)
P1817A−08ST	P1817A	20−32	8−pin SOIC, tube	0 to 70
P1817AF−08ST	P1817AF	20−32	8−pin SOIC, tube, pb free	0 to 70
I1817A−08SR	I1817A	20−32	8−pin SOIC, tape and reel	−20 to +85
I1817BF−08SR	I1817BF	10−20	8−pin SOIC, tape and reel, pb free	−20 to +85

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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P1817A/D