LCD Panel EMI Reduction IC

Features

- FCC approved method of EMI attenuation.
- Provides up to 20dB of EMI suppression.
- Generates a low EMI spread spectrum clock of the input frequency.
- Input frequency range: 30MHz to 100MHz.
- Optimized for VGA, SVGA, and higher resolution XGA LCD Panels.
- Internal loop filter minimizes external components and board space.
- Six selectable high spread ranges up to ± 2%.
- Two selectable modulation rates.
- SSON# control pin for spread spectrum enable and disable options.
- Low cycle-to-cycle jitter.
- Wide operating range.
- Low power CMOS design.
- Supports most mobile graphic accelerator specifications.
- Products available for automotive temperature range. *(Refer Spread Spectrum Range Selection Tables)*
- Available in 8-pin SOIC and TSSOP Packages.

Product Description

The P2040A is a versatile spread spectrum frequency modulator designed specifically for digital flat panel applications. The P2040A reduces electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of down stream clock and data dependent signals. The P2040A allows significant system cost savings by reducing the number of circuit board layers ferrite beads, shielding and other passive components that are traditionally required to pass EMI regulations.

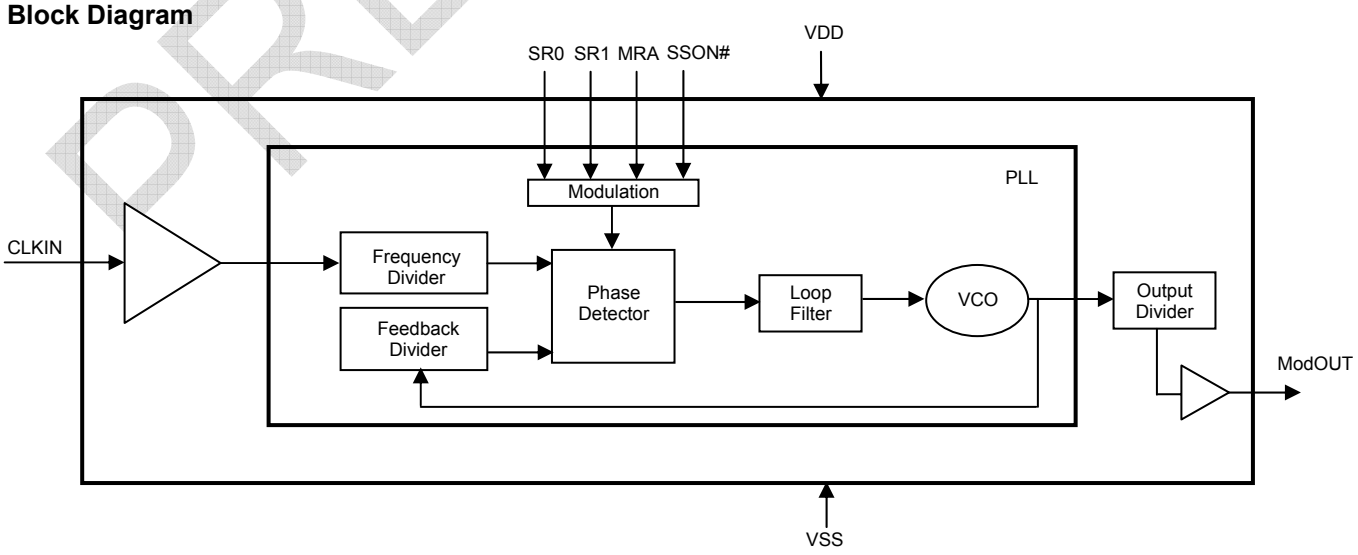
The P2040A uses the most efficient and optimized modulation profile approved by the FCC and is implemented in a proprietary all digital method.

The P2040A modulates the output of a single PLL in order to "spread" the bandwidth of a synthesized clock, and more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal's bandwidth is called 'spread spectrum clock generation'.

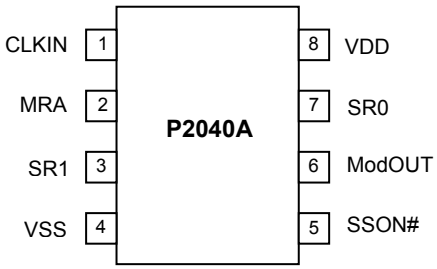
Applications

The P2040A is targeted towards digital flat panel applications for notebook PCs, palm-size PCs, office automation equipments and LCD monitors.

Block Diagram



Pin Configuration



Pin Description

Pin#	Pin Name	Type	Description
1	CLKIN	I	External reference frequency input. Connect to externally generated reference signal.
2	MRA	I	Digital logic input used to select modulation rate. This pin has an internal pull-up resistor.
3	SR1	I	Digital logic input used to select Spreading Range. This pin has an internal pull-up resistor.
4	VSS	P	Ground to entire chip. Connect to system ground.
5	SSON#	I	Digital logic input used to enable Spread Spectrum function (Active LOW). Spread Spectrum function enabled when LOW, disabled when HIGH. This pin has an internal pull-low resistor.
6	ModOUT	O	Spread spectrum clock output.
7	SR0	I	Digital logic input used to select Spreading Range. This pin has an internal pull-up resistor.
8	VDD	P	Power supply for the entire chip (3.3V)

Modulation Selection (Commercial)

MRA	SR1	SR0	Spreading Range	Modulation Rate (KHz)
0	0	0	± 1.125	(FIN /40) * 34.72KHz
0	0	1	± 1.75	(FIN /40) * 34.72KHz
0	1	0	± 0.75	(FIN /40) * 34.72KHz
0	1	1	± 1.25	(FIN /40) * 34.72KHz
1	0	0	± 1.25	(FIN /40) * 20.83KHz
1	0	1	± 2.00	(FIN /40) * 20.83KHz
1	1	0	Reserved	Reserved
1	1	1	Reserved	Reserved

Spread Range Selection at 50MHz (Automotive)

MRA	SR1	SR0	Spreading Range	Modulation Rate
0	0	0	± 1.25	(F_{IN}/40) * 34.72KHz
0	0	1	± 2.00	(F_{IN}/40) * 34.72KHz
0	1	0	± 1.00	(F_{IN}/40) * 34.72KHz
0	1	1	± 1.50	(F_{IN}/40) * 34.72KHz
1	0	0	± 1.25	(F_{IN}/40) * 20.83KHz
1	0	1	± 2.00	(F_{IN}/40) * 20.83KHz
1	1	0	± 1.25	(F_{IN}/40) * 20.83KHz
1	1	1	± 2.00	(F_{IN}/40) * 20.83KHz

Spread Range Selection at 70MHz (Automotive)

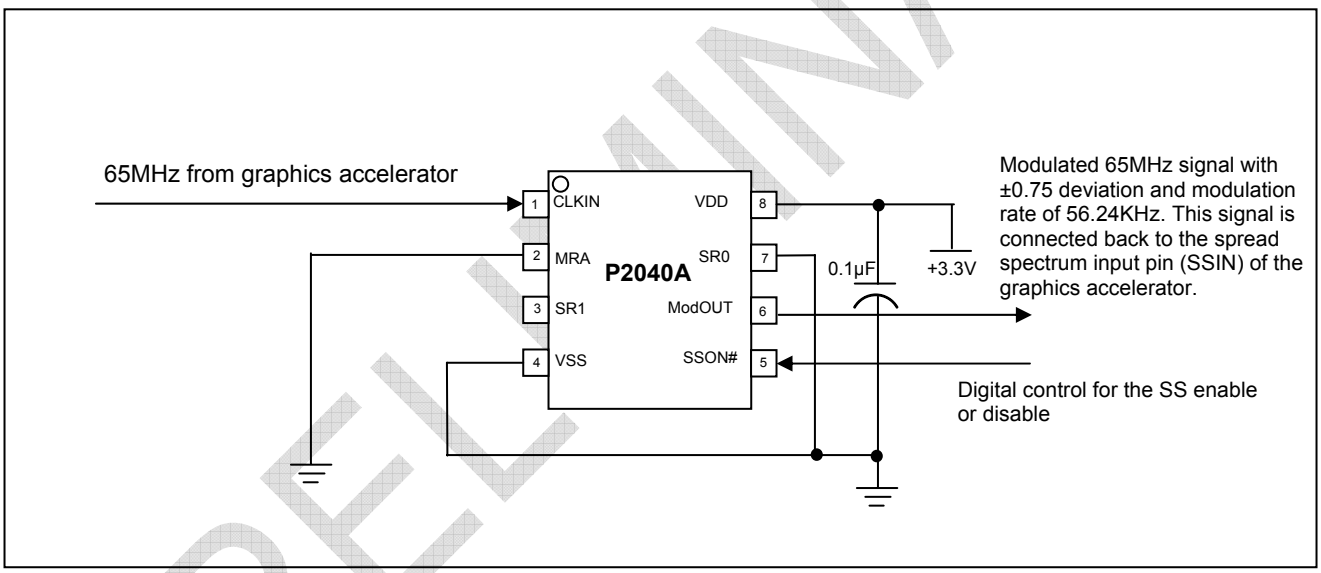
MRA	SR1	SR0	Spreading Range	Modulation Rate
0	0	0	± 1.00	(F_{IN}/40) * 34.72KHz
0	0	1	± 1.50	(F_{IN}/40) * 34.72KHz
0	1	0	± 0.70	(F_{IN}/40) * 34.72KHz
0	1	1	± 1.00	(F_{IN}/40) * 34.72KHz
1	0	0	± 1.15	(F_{IN}/40) * 20.83KHz
1	0	1	± 2.00	(F_{IN}/40) * 20.83KHz
1	1	0	± 1.15	(F_{IN}/40) * 20.83KHz
1	1	1	± 1.75	(F_{IN}/40) * 20.83KHz

Spread Spectrum Selection

The *Modulation Selection Table* defines the possible spread spectrum options. The optimal setting should minimize system EMI to the fullest without affecting system performance. The spreading is described as a percentage deviation of the center frequency. (Note: The center frequency is the frequency of the external reference input on CLKIN, pin1).

For example, P2040A is designed for high-resolution, flat panel applications and is able to support an XGA (1024 x 768) flat panel operating at 65MHz (F_{IN}) clock speed. A spreading selection of MRA=0, SR1=1 and SR0=0 provides a percentage deviation of ±0.75% from F_{IN}. This results in the frequency on ModOUT being swept from 64.51MHz to 65.49MHz at a modulation rate of 56.24KHz. *Refer Modulation Selection Table*. The example in the following illustration is a common EMI reduction method for a notebook LCD panel and has already been implemented by most of the leading OEM and mobile graphic accelerator manufacturers.

Application Schematic for Mobile LCD Graphics Controllers



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VDD, V_{IN}	Voltage on any pin with respect to Ground	-0.5 to +7.0	V
T_{STG}	Storage temperature	-65 to +125	°C
T_C	Operating temperature-Commercial	0 to 70	°C
T_A	Operating temperature – Automotive	-40 to +125	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

DC Electrical Characteristics

(Test condition: All parameters are measured at room temperature (+25°C) unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input low voltage	VSS - 0.3	-	0.8	V
V_{IH}	Input high voltage	2.0	-	VDD + 0.3	V
I_{IL}	Input low current (pull-up resistor on inputs SR0, SR1 and MRA)	-35	-	-	µA
I_{IH}	Input high current (pull-down resistor on input SSON#)	-	-	35	µA
V_{OL}	Output low voltage (VDD = 3.3V, I_{OL} = 20mA)	-	-	0.4	V
V_{OH}	Output high voltage (VDD = 3.3V, I_{OH} = 20mA)	2.5	-	-	V
I_{DD}	Static supply current standby mode	-	0.6	-	mA
I_{CC}	Dynamic supply current (3.3V and 10pF loading)	7	10	13	mA
VDD	Operating voltage	2.7	3.3	3.7	V
t_{ON}	Power-up time (first locked cycle after power up)	-	0.18	-	mS
Z_{OUT}	Clock output impedance	-	50	-	Ω

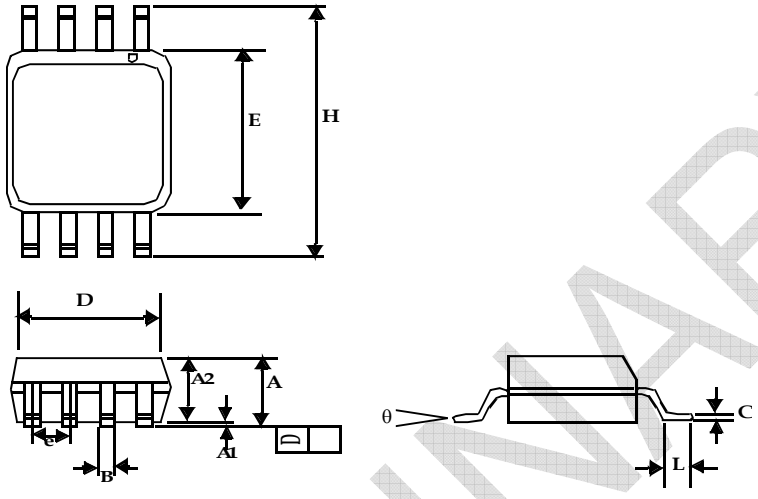
AC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input frequency	30	-	100	MHz
f_{OUT}	Output frequency	30	-	100	MHz
t_{LH}*	Output rise time (measured at 0.8V to 2.0V)	0.7	0.9	1.1	nS
t_{HL}*	Output fall time (measured at 2.0V to 0.8V)	0.6	0.8	1.0	nS
t_{JC}	Jitter (cycle to cycle)	-	-	360	pS
t_D	Output duty cycle	45	50	55	%

*t_{LH} and t_{HL} are measured into a capacitive load of 15pF

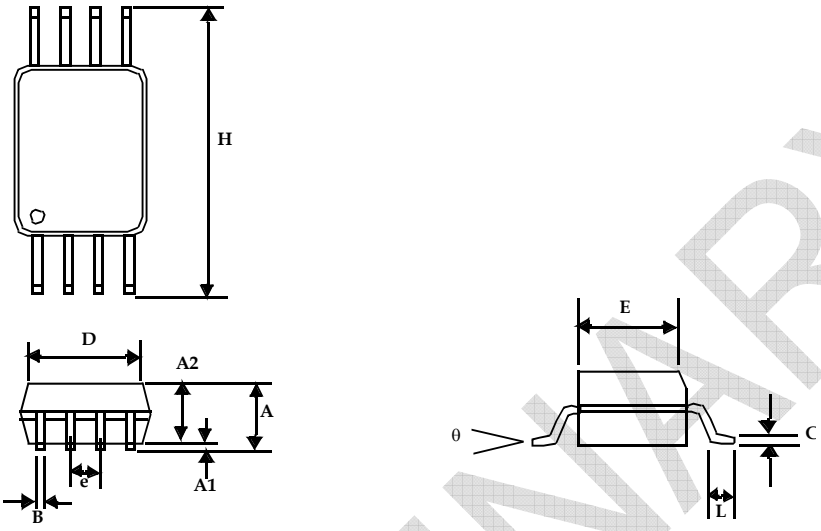
Package Information

8-lead (150-mil) SOIC Package



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A1	0.004	0.010	0.10	0.25
A	0.053	0.069	1.35	1.75
A2	0.049	0.059	1.25	1.50
B	0.012	0.020	0.31	0.51
C	0.007	0.010	0.18	0.25
D	0.193 BSC		4.90 BSC	
E	0.154 BSC		3.91 BSC	
e	0.050 BSC		1.27 BSC	
H	0.236 BSC		6.00 BSC	
L	0.016	0.050	0.41	1.27
θ	0°	8°	0°	8°

8-lead Thin Shrunk Small Outline Package (4.40-MM Body)

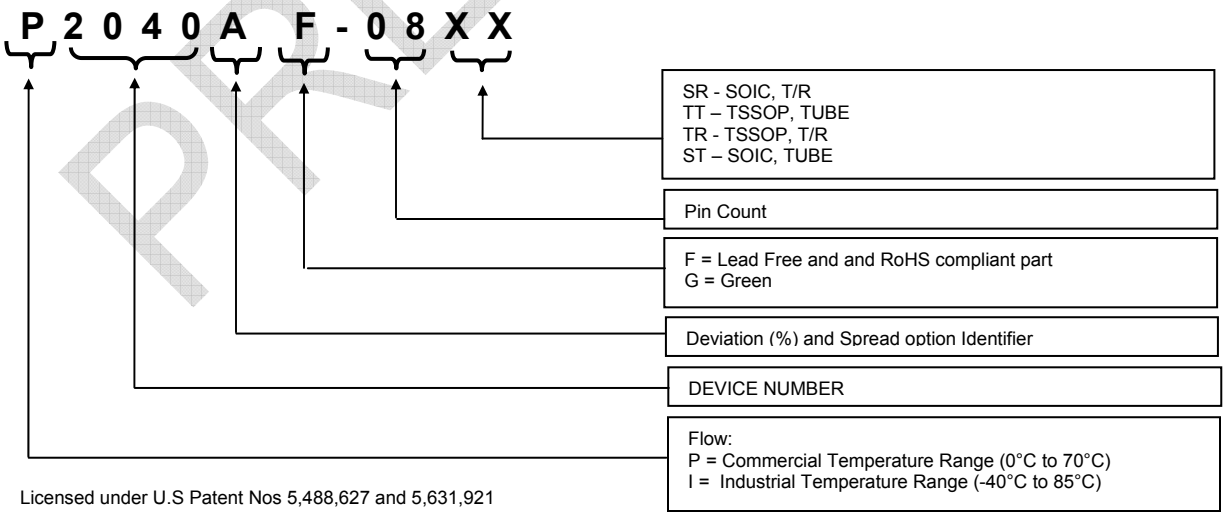


Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A		0.043		1.10
A1	0.002	0.006	0.05	0.15
A2	0.033	0.037	0.85	0.95
B	0.008	0.012	0.19	0.30
c	0.004	0.008	0.09	0.20
D	0.114	0.122	2.90	3.10
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.252 BSC		6.40 BSC	
L	0.020	0.028	0.50	0.70
θ	0°	8°	0°	8°

Ordering Information

Part number	Marking	Package Type	Temperature
P2040A -08-ST	P2040A	8-Pin SOIC,Tube	Commercial
P2040A -08-SR	P2040A	8-Pin SOIC, Tape and Reel	Commercial
P2040AF-08-ST	P2040AF	8-Pin SOIC, Tube, Pb Free	Commercial
P2040AF-08-SR	P2040AF	8-Pin SOIC, Tape and Reel, Pb Free	Commercial
P2040AG-08-ST	P2040AG	8-Pin SOIC, Tube, Green	Commercial
P2040AG-08-SR	P2040AG	8-Pin SOIC, Tape and Reel, Green	Commercial
I2040A-08-ST	I2040A	8-Pin SOIC, Tube	Industrial
I2040A-08-SR	I2040A	8-Pin SOIC, Tape and Reel	Industrial
I2040AF-08-ST	I2040AF	8-Pin SOIC, Tube, Pb Free	Industrial
I2040AF-08-SR	I2040AF	8-Pin SOIC, Tape and Reel, Pb Free	Industrial
I2040AG-08-ST	I2040AG	8-Pin SOIC, Tube, Green	Industrial
I2040AG-08-SR	I2040AG	8-Pin SOIC, Tape and Reel, Green	Industrial
P2040A-08-TT	P2040A	8-Pin TSSOP, Tube	Commercial
P2040A-08-TR	P2040A	8-Pin TSSOP, Tape and Reel	Commercial
P2040AF-08-TT	P2040AF	8-Pin TSSOP, Tube, Pb Free	Commercial
P2040AF-08-TR	P2040AF	8-Pin TSSOP, Tape and Reel, Pb Free	Commercial
P2040AG-08-TT	P2040AG	8-Pin TSSOP, Tube, Green	Commercial
P2040AG-08-TR	P2040AG	8-Pin TSSOP, Tape and Reel, Green	Commercial
I2040A-08-TT	I2040A	8-Pin TSSOP, Tube	Industrial
I2040A-08-TR	I2040A	8-Pin TSSOP, Tape and Reel	Industrial
I2040AF-08-TT	I2040AF	8-Pin TSSOP, Tube, Pb Free	Industrial
I2040AF-08-TR	I2040AF	8-Pin TSSOP, Tape and Reel, Pb Free	Industrial
I2040AG-08-TT	I2040AG	8-Pin TSSOP, Tube, Green	Industrial
I2040AG-08-TR	I2040AG	8-Pin TSSOP, Tape and Reel, Green	Industrial

Device Ordering Information



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Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to Alliance Semiconductor, dated 11-11-2003