

P20FE12SLK

Power MOSFETs
120V, 20A, N-channel

Feature

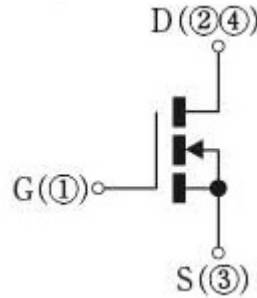
- N-channel
- SMD
- Low Ron
- 4.5V Gate Drive
- Low Capacitance
- Based on AEC-Q101
- Pb free terminal
- RoHS:Yes

OUTLINE

Package (House Name): FE
Package (JEDEC Code): TO-252AB similar
Package (JEITA Code): SC-63



Equivalent circuit



Absolute Maximum Ratings (unless otherwise specified : Tc=25°C)

Item	Symbol	Conditions	Ratings	Unit
Storage temperature	Tstg		-55 to 175	°C
Channel temperature	Tch		-55 to 175	°C
Drain-source voltage	V _{DSS}		120	V
Gate-source voltage	V _{GSS}		±20	V
Continuous drain current(DC)	I _D		20	A
Continuous drain current(Peak)	I _{DP}	Pulse width 10µs, duty=1/100	60	A
Total power dissipation	P _T		44	W
Single avalanche current	I _{AS}	Starting T _{ch} =25°C T _{ch} ≤150°C	17	A
Single avalanche energy	E _{AS}	Starting T _{ch} =25°C T _{ch} ≤150°C	14	mJ

* : See the original Specifications

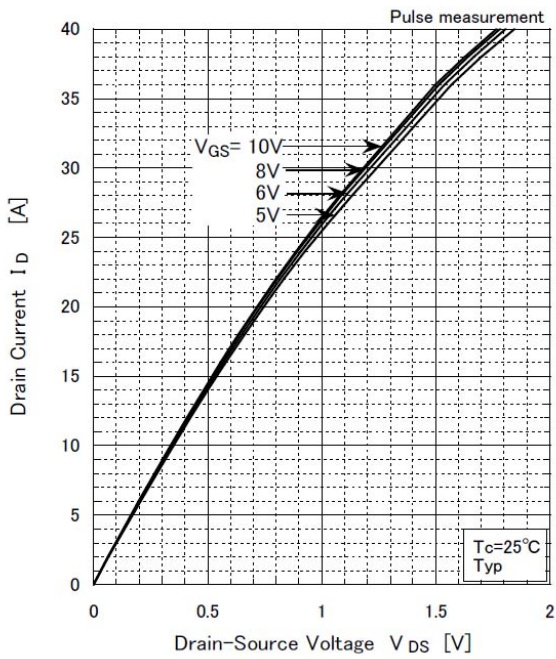
Electrical Characteristics (unless otherwise specified : Tc=25°C)

Item	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Drain-Source breakdown voltage	$V_{(BR)DSS}$	ID=1mA, VGS=0V	120			V
Zero gate voltage drain current	I_{DSS}	VDS=120V, VGS=0V			1	μA
Gate-source leakage current	I_{GSS}	VGS=±20V, VDS=0V			±0.1	μA
Forward transconductance	g_{fs}	ID=10A, VDS=10V	9			S
Static drain-source on-state resistance	$R_{DS(ON)}$	ID=10A, VGS=10V		0.035	0.044	Ω
Static drain-source on-state resistance	$R_{DS(ON)}$	ID=10A, VGS=4.5V		0.037	0.05	Ω
Gate threshold voltage	V_{th}	ID=1mA, VDS=10V	1.5	2	2.5	V
Source-drain diode forward voltage	V_{SD}	IS=20A, VGS=0V			1.5	V
Thermal resistance	$R_{th(j-c)}$	Junction to case, with heatsink			3.4	°C/W
Total gate charge	Q_g	VDD=96V, VGS=10V, ID=20A		46		nC
Gate to source charge	Q_{gs}	VDD=96V, VGS=10V, ID=20A		8		nC
Gate to drain charge	Q_{gd}	VDD=96V, VGS=10V, ID=20A		12		nC
Input capacitance	C_{iss}	VDS=25V, VGS=0V, f=1MHz		2110		pF
Reverse transfer capacitance	C_{rss}	VDS=25V, VGS=0V, f=1MHz		73		pF
Output capacitance	C_{oss}	VDS=25V, VGS=0V, f=1MHz		140		pF
Turn-on delay time	$t_{d(on)}$	ID=10A, RL=6Ω, VDD=60V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		6		ns
Rise time	t_r	ID=10A, RL=6Ω, VDD=60V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		9		ns
Turn-off delay time	$t_{d(off)}$	ID=10A, RL=6Ω, VDD=60V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		32		ns
Fall time	t_f	ID=10A, RL=6Ω, VDD=60V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		18		ns
Diode reverse recovery time	t_{rr}	IF=20A, VGS=0V, di/dt=100A/μs		57		ns
Diode reverse recovery charge	Q_{rr}	IF=20A, VGS=0V, di/dt=100A/μs		120		nC

* : See the original Specifications

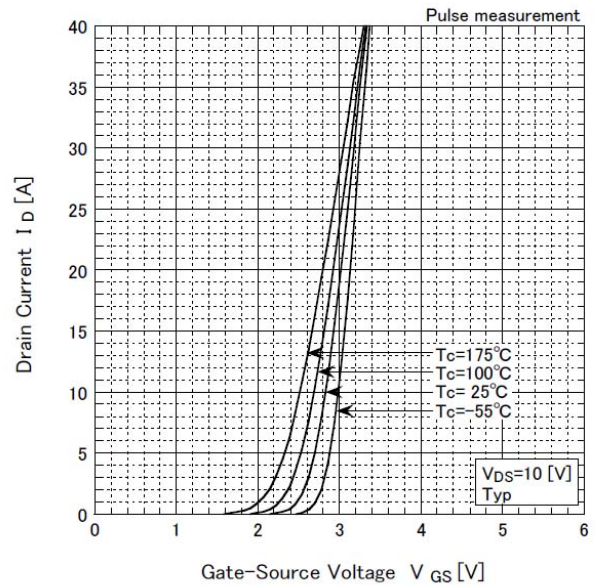
CHARACTERISTIC DIAGRAMS

Typical Output Characteristics



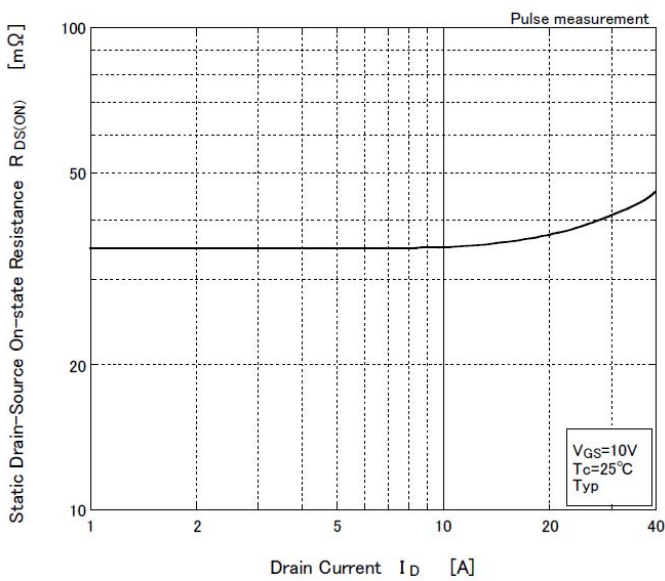
Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Transfer Characteristics



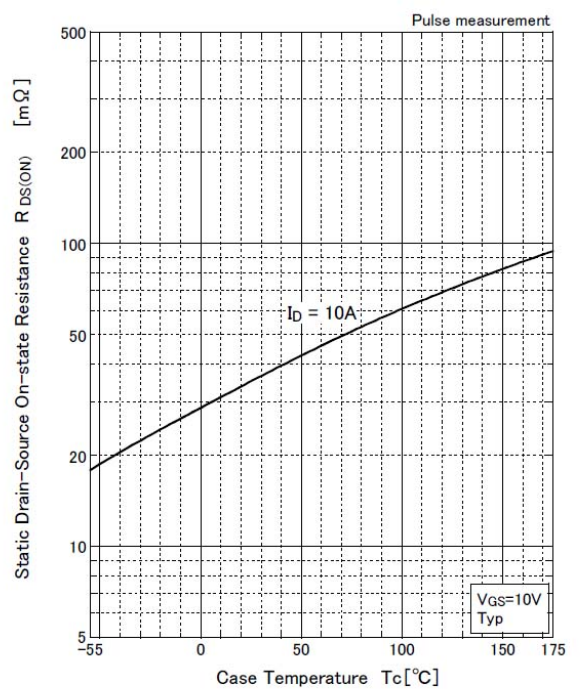
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Static Drain-Source On-state Resistance vs Drain Current



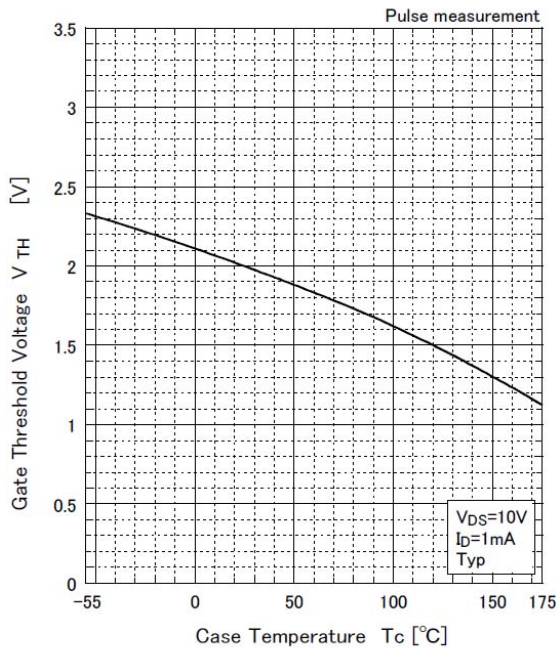
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Static Drain-Source On-state Resistance vs Case Temperature



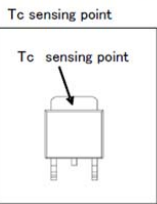
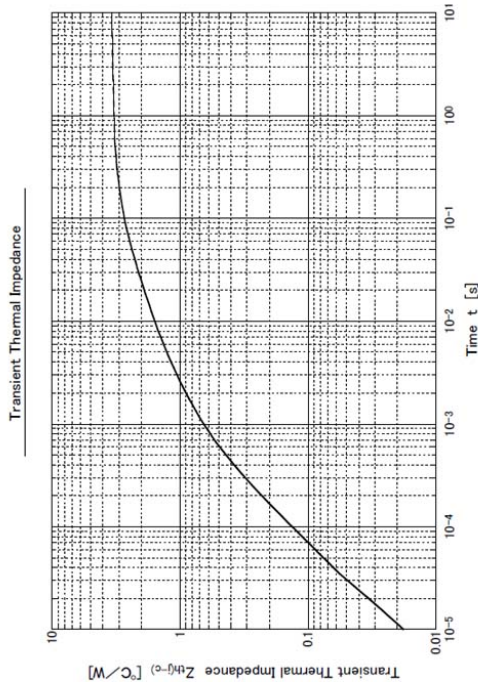
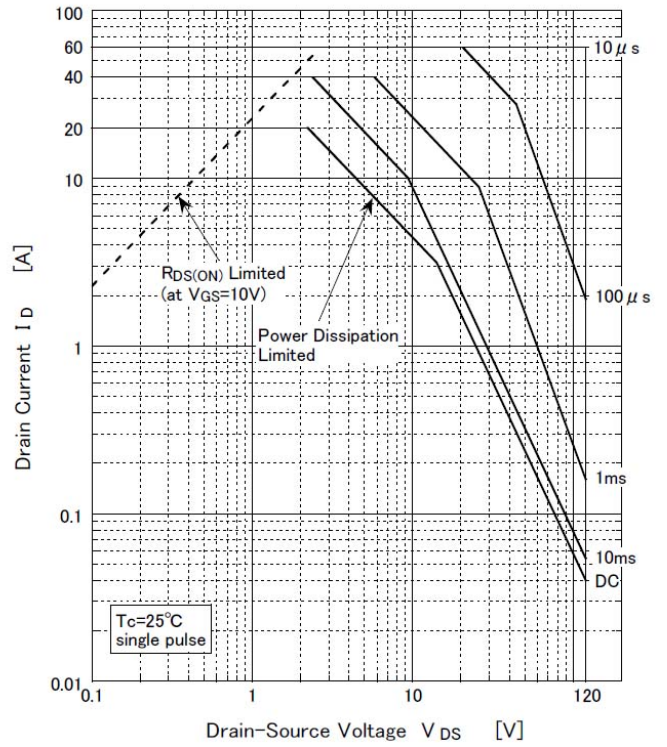
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Gate Threshold Voltage vs Case Temperature

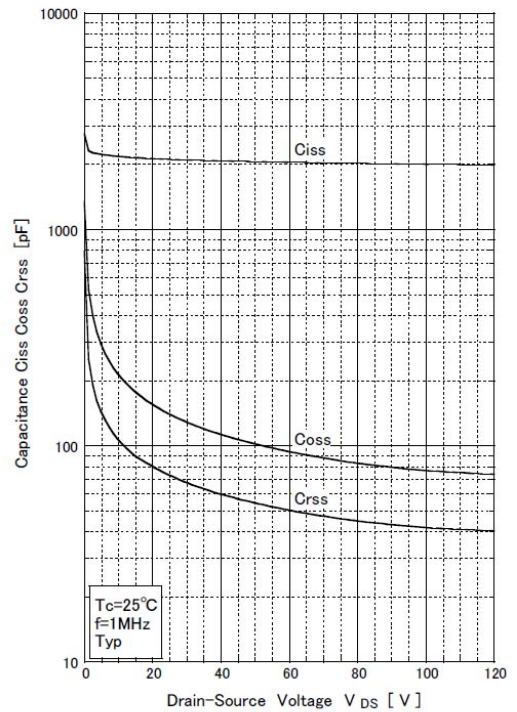


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Safe Operating Area

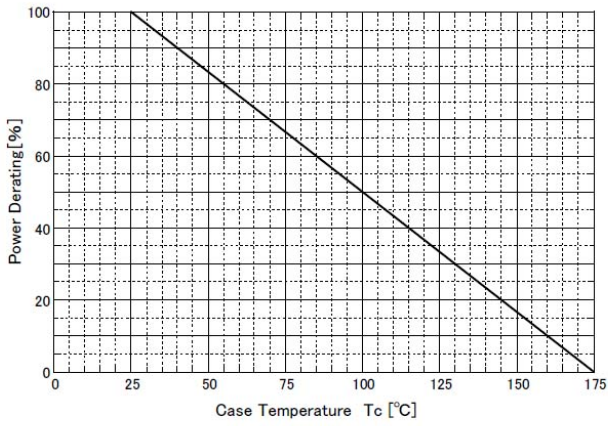


Capacitance Characteristics

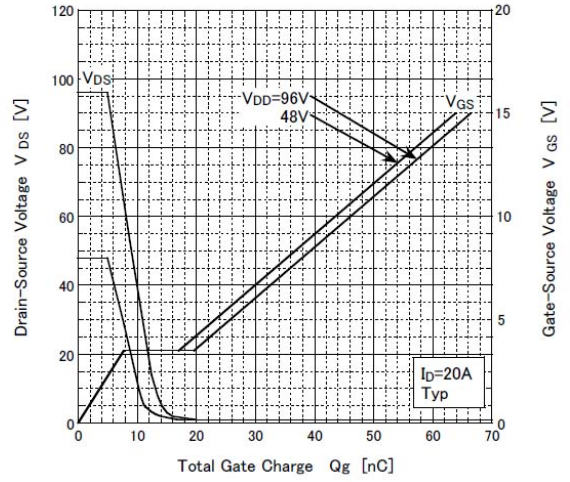


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Power Derating – Case Temperature

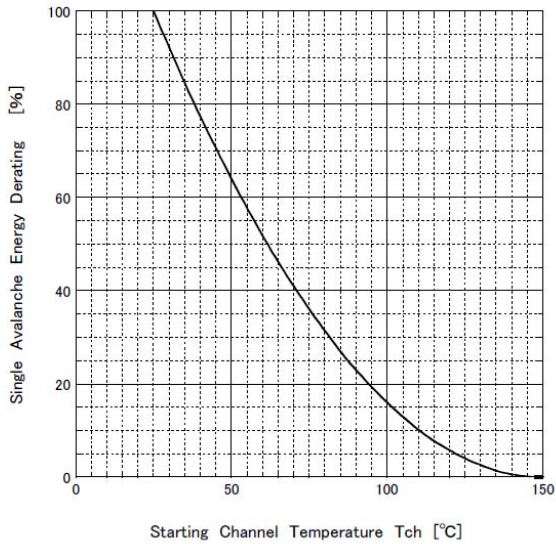


Gate Charge Characteristics



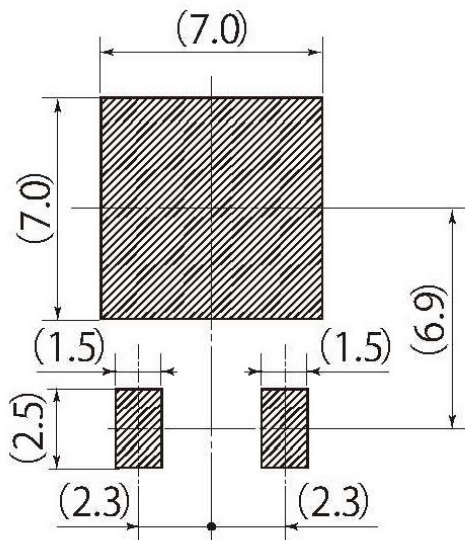
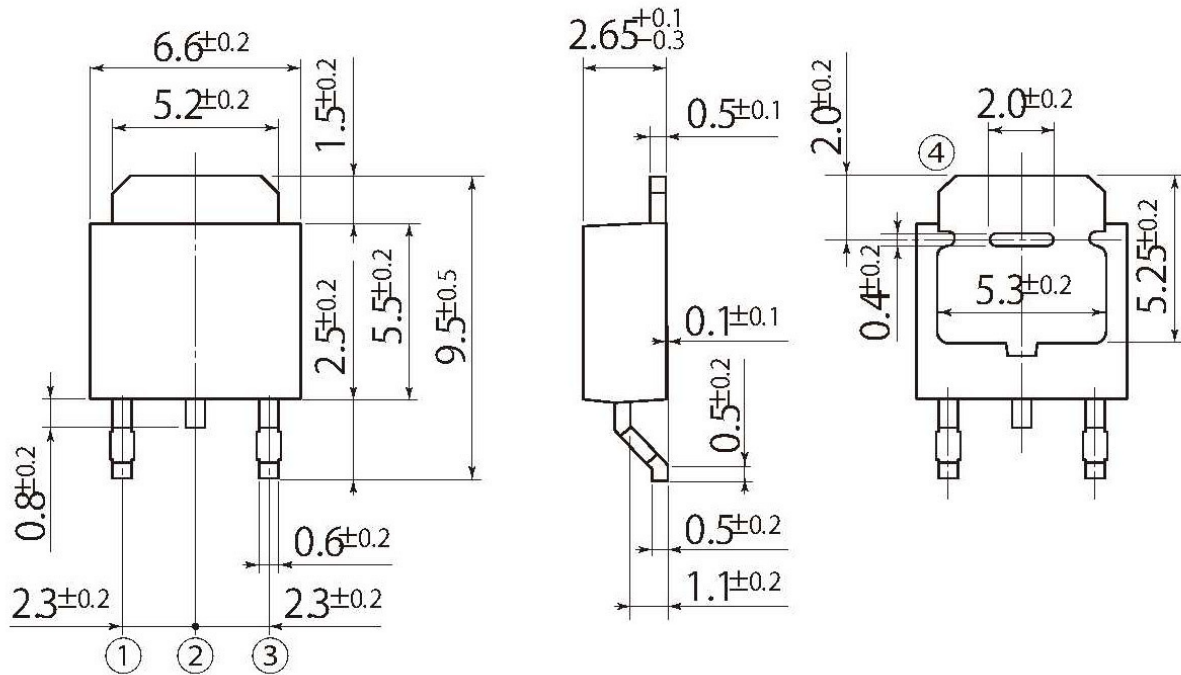
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Single Avalanche Energy Derating vs Channel Temperature



G3

JEDEC Code	TO-252AB similar
JEITA Code	SC-63
House Name	FE



Referential Soldering Pad

• Optimize soldering pad to the board design and soldering condition.

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