P24C32D

I²C-Compatible Serial E²PROM

Data Sheet Rev.1.0

General Description

The P24C32D is 32-KbitI²C-compatibleSerial EEPROM (Electrically Erasable Programmable Memory) device. It contains a memory array of 4096× 8bits, which is32-byteper page. P24C32D provides the following devices for different application.

Device Selection Table

Device Name	Suppy	Temp. Range	Max. Clock Frequency
P24C32D-MI	1.7V~5.5V	-40°C ~ 85°C	1MHz[1]

Note 1: 400 kHz for V_{CC}< 2.5V.

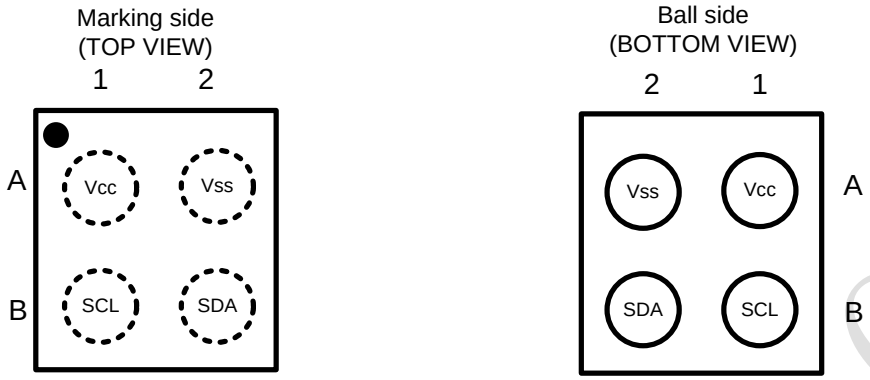
Features

- Single Supply Voltage and High Speed
  - ✧ Minimum operating voltage down to 1.7V
  - ✧ Max 1 MHz clock from 2.5V to 5.5V
  - ✧ Max 400kHz clock from 1.7V to 2.5V
- Low power CMOS technology
  - ✧ Read current 100uA, maximum
  - ✧ Write current 0.5mA, maximum
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Sequential & Random Read Features
- Page Write Modes, Partial Page Writes Allowed
- Additional Write Lockable Page and 128-bit Serial Number
- Self-timed Write Cycle (5ms maximum)
- High Reliability
  - ✧ Endurance: 2 Million Write Cycles
  - ✧ Data Retention: 200 Years
  - ✧ ESD Protection(HBM): 4KV
  - ✧ Latch up Capability: +/- 200mA (25°C)
- Package:
  - ✧ 4-balls WLCSP. Ball Pitch 400umx400um

1.Pin Configuration

1.1 Pin Configuration

Figure 1-1 WLCSP-4 Balls (Ball pitch 400um*400um)



1.2 Pin Definition

Table 1-1Pin Definition for Package WLCSP4-balls (Ball pitch 400um)

Pin	Name	Type	Description
A1	V_{CC}	Power	Power Supply
A2	Vss	Ground	Ground
B1	SCL	Input	Serial Clock Input
B2	SDA	I/O	Serial Data Input and Serial Data Output

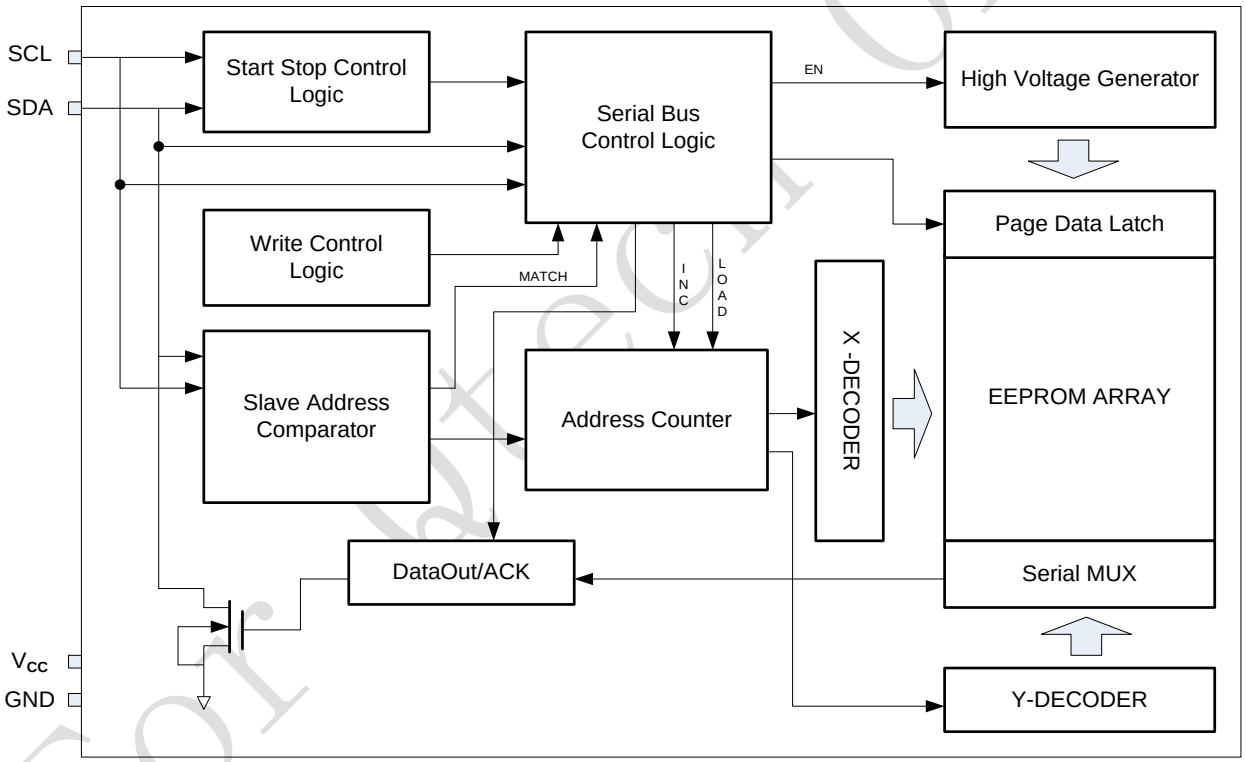
1.3 Pin Descriptions

Serial Clock (SCL): The SCL input is used to clock in data at positive edges and clock out data of the device at negative edges.

Serial Data (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open drain driven and may be wired-OR with any number of other open-drain or open-collector devices.

2. Block Diagram

Figure 2-1 Block Diagram



3. Electrical Characteristics

Absolute Maximum Ratings

- Storage Temperature .....-65°C to +150°C
- Operation Temperature .....-40°C to +125°C
- Maximum Operation Voltage..... 6.25V
- Voltage on Any Pin with Respect to Ground.....-1.0V to (Vcc+1.0)V
- DC Output Current .....5.0 mA

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to thedevice. This is a stress rating only and functional operation of the device at those or any other conditions above thoseindicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions forextended periods may affect device reliability.

Table 3-1 Pin Capacitance[1]

Symbol	Parameter	Max.	Units	Test Condition
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$=Vss
C_{IN}	Input Capacitance (SCL)	6	pF	V_{IN}=Vss

Note: [1] Test Conditions: T_A= 25°C, Freq. = 1MHz, Vcc = 5.0V.

Table 3-2 DC Characteristics （Unless otherwise specified, V_{CC} = 1.7V to 5.5V, T_A = –40°C to 125°C）

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{CC}	Supply Voltage	1.7	-	5.5	V	P24C32D-MI
Isb	Standby Current	-	-	0.6	µA	Vcc = 3.3V, T_A = 85°C
		-	-	1.0	µA	Vcc = 5.5V, T_A = 85°C
		-	-	2.0	uA	Vcc = 5.5V, T_A = 105°C
I_{CC1}	Supply Current	-	0.1	0.2	mA	Vcc=5.5V, Read at 400Khz
I_{CC2}	Supply Current	-	0.5	1	mA	Vcc=5.5V Write at 400Khz
I_{LI}	Input Leakage Current	-	0.10	1.0	µA	V_{IN} = V_{CC} or Vss
I_{LO}	Output Leakage Current	-	0.05	1.0	µA	V_{OUT} = V_{CC} or Vss
V_{IL}	Input Low Level	–0.6	-	0.3V_{CC}	V	
V_{IH}	Input High Level	0.7V_{CC}	-	V_{CC}+0.5	V	
V_{OL1}	Output Low Level V_{CC} = 1.7V (SDA)	-	-	0.2	V	I_{OL} = 1.5 mA
V_{OL2}	Output Low Level V_{CC} = 3.0V(SDA)	-	-	0.4	V	I_{OL} = 2.1 mA

Table 3-3 AC Characteristics（Unless otherwise specified, V_{CC} = 1.7V to 5.5V, T_A = –40°C to 125°C, C_L=100pF, Test Conditions are listed in Notes [2] ）

Symbol	Parameter	1.7≤V_{CC}<2.5			2.5≤V_{CC}≤5.5			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Clock Frequency, SCL	-	-	400	-	-	1000	kHz
t_{LOW}	Clock Pulse Width Low	1.3	-	-	0.4	-	-	μs
t_{HIGH}	Clock Pulse Width High	0.6	-	-	0.4	-	-	μs
t_{AA}	Clock Low to Data Out Valid	0.05	-	0.9	0.05	-	0.55	μs
t_I	Noise Suppression Time	-	-	0.1	-	-	0.05	μs
t_{BUF}	Time the bus must be free before a new transmission can start	1.3	-	-	0.5	-	-	μs
$t_{HD.STA}$	START Hold Time	0.6	-	-	0.25	-	-	μs
$t_{SU.STA}$	START Setup Time	0.6	-	-	0.25	-	-	μs
$t_{HD.DAT}$	Data In Hold Time	0	-	-	0	-	-	μs
$t_{SU.DAT}$	Data In Setup Time	0.1	-	-	0.1	-	-	μs
t_R	Inputs Rise Time[1]	-	-	0.3	-	-	0.3	μs
t_F	Inputs Fall Time[1]	-	-	0.3	-	-	0.1	μs
$t_{SU.STO}$	STOP Setup Time	0.6	-	-	0.25	-	-	μs
t_{DH}	Data Out Hold Time	0.05	-	-	0.05	-	-	μs
$t_{SU.WCB}$	WCB pin Setup Time	1.2	-	-	0.6	-	-	μs
$t_{HD.WCB}$	WCB pin Hold Time	1.2	-	-	0.6	-	-	μs
t_{WR}	Write Cycle Time	-	-	5	-	-	5	ms

Notes: [1] This parameter isensured by characterization not 100% tested

[2] AC measurement conditions:

- ✧ R_L (connects to V_{CC}): 1.3kΩ(2.5V, 5.5V), 10kΩ(1.7V)
- ✧ Input pulse voltages: 0.3 V_{CC} to 0.7 V_{CC}
- ✧ Input rise and fall times: ≤50ns
- ✧ Input and output timing reference voltages: 0.5V_{CC}

Table 3-4 ReliabilityCharacteristic [1]

Symbol	Parameter	Min.	Typ.	Max.	Unit
EDR[2]	Endurance	2,000,000			Write cycles
DRET	Data retention	200			Years

Note:[1] This parameter is ensured by characterization and is not 100% tested

[2] Under the condition: 25°C, 3.3V, Page mode

Figure 3-1 Bus Timing

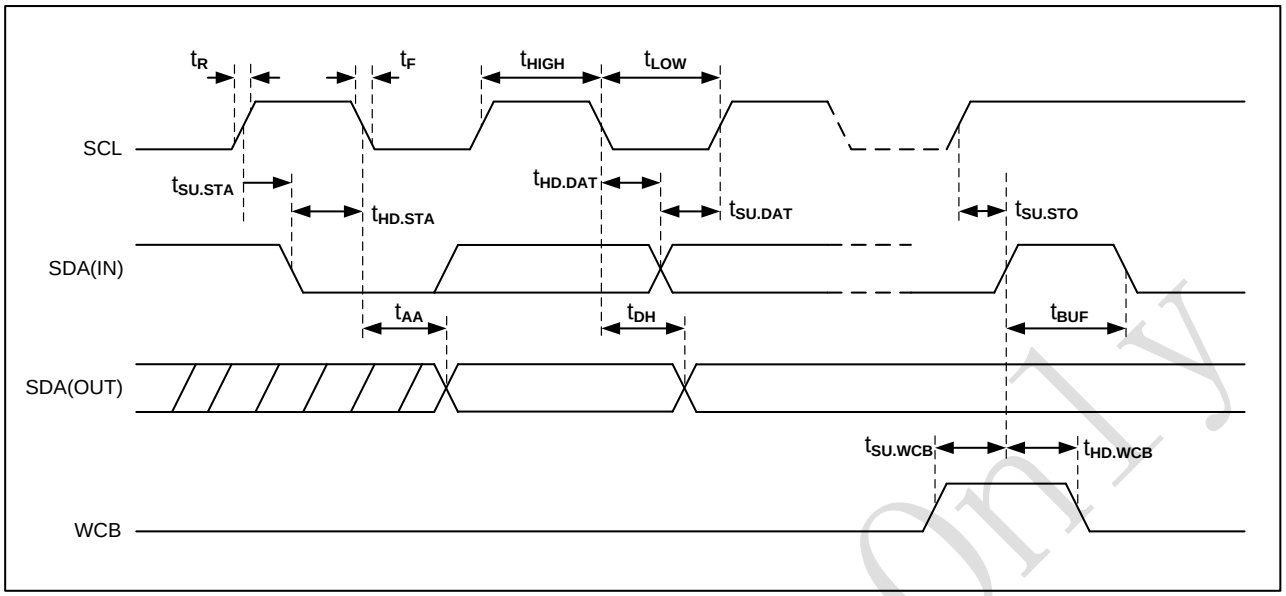
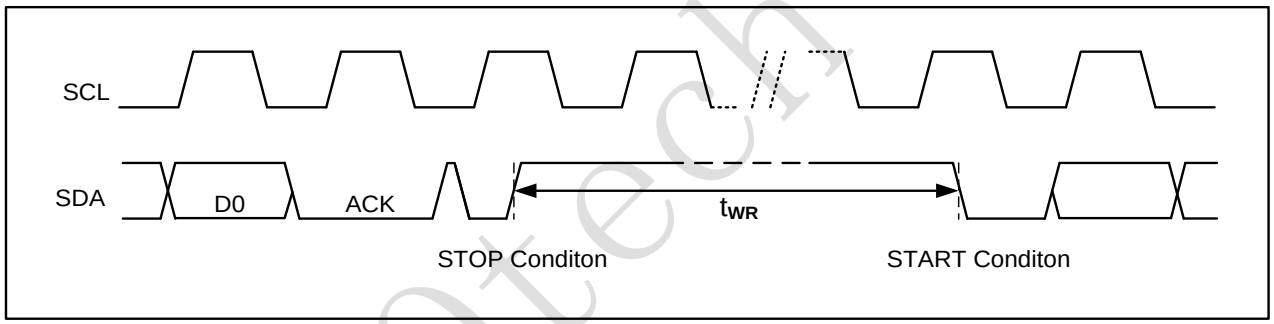


Figure 3-2 Write Cycle Timing



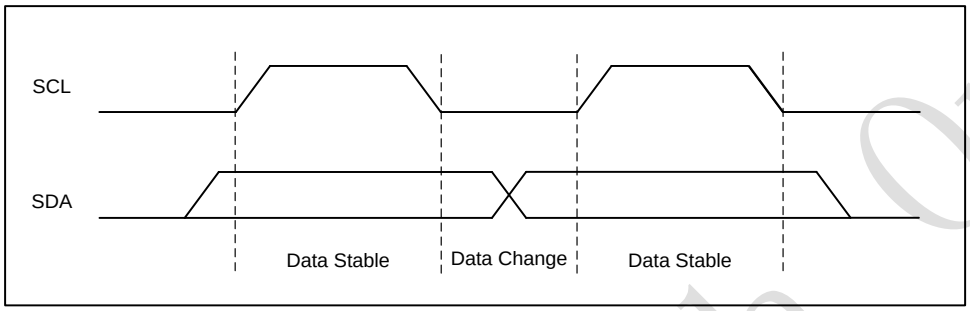
Note: [1] The write cycle time t_{WR} is the time from a valid STOP condition of a write sequence to the end of the internal clear/write cycle.

4. Device Operation

4.1 Data Input

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low periods (Refer to Figure 4-1). Data changes during SCL high periods will indicate a START or STOP bit as defined below.

Figure 4-1 Data Validity



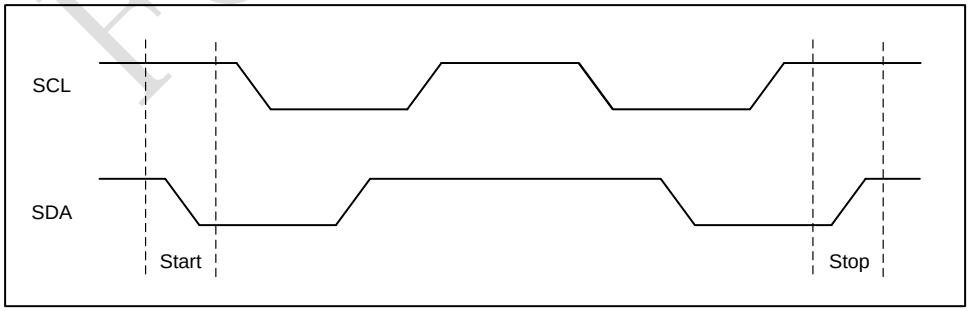
4.2 START Condition

A high-to-low transition of SDA with SCL high is a START condition which must precede any other command bits (Refer to Figure 4-2).

4.3 Stop Condition

A low-to-high transition of SDA with SCL high is a STOP condition. After a read sequence, the STOP bit will place the P24C32D in a standby mode (Refer to Figure 4-2).

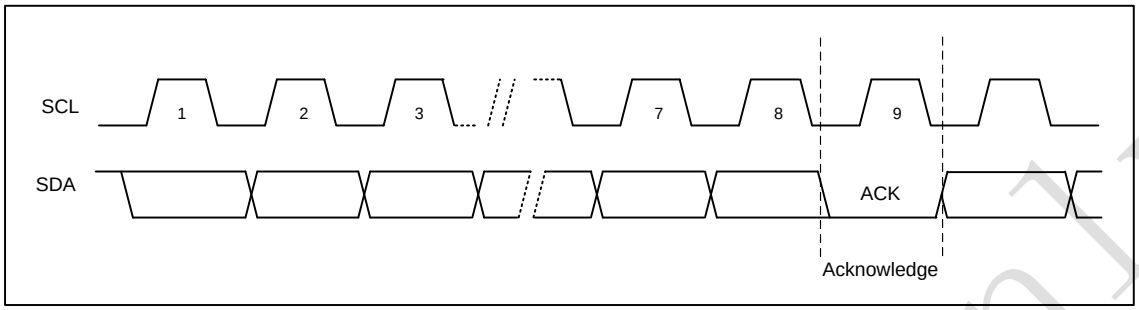
Figure 4-2 START and Stop Definition



4.4 Acknowledge(ACK)

All addresses and data are serially transmitted to and from the P24C32D in 8-bit data. The P24C32D sends a "0" to acknowledge that it has received each data byte. This happens during the ninth clock cycle.

Figure 4-3 Acknowledge Bit Definition



4.5 Standby Mode

The P24C32D features a low-power standby mode which is enabled:

(a) After a fresh power up

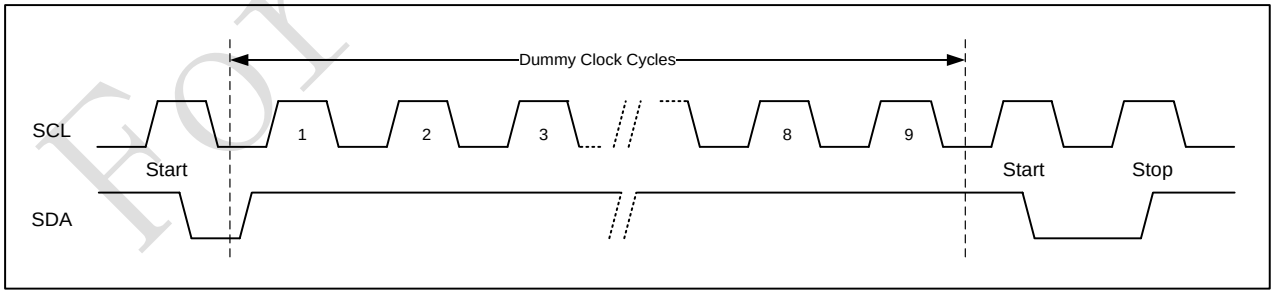
(b) After receiving a STOP bit in read mode

(c)After completing a self-time internal programming operation

4.6 Soft Reset

After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps: (a) Create a START condition, (b) Clock in nine data bits "1" and (c) create another START bit followed by STOP bit condition, as shown below. The device is ready for the next communication after the above steps have been completed.

Figure 4-4 Soft Reset



4.7 Device Addressing

The P24C32 requires an 8-bit device address following a START condition to enable the chip for a read or write operation (Refer totable below). The device address consists of a mandatory one-zero sequence for

the first four most-significant bits, as shown.

Table 4-1 Device Address

Chip	Access area	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P24C32D	Normal Area	1	0	1	0	0	0	0	R/W
	ID Page	1	0	1	1	0	0	0	R/W
	Lock Bit	1	0	1	1	0	0	0	R/W
	Serial Number	1	0	1	1	0	0	0	1

Table 4-2 Word Address0

Chip	Data	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P24C32D	Normal Area	0	X	X	X	A11	A10	A9	A8
	ID Page	X	X	X	X	0	0	X	X
	Lock Bit	X	X	X	X	0	1	X	X
	Serial Number	X	X	X	X	1	0	X	X

Table 4-3 Word Address1

Chip	Data	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P24C32D	Normal Area	A7	A6	A5	A4	A3	A2	A1	A0
	ID Page	X	X	X	A4	A3	A2	A1	A0
	Lock Bit	X	X	X	X	X	X	X	X
	Serial Number	X	X	X	X	A3	A2	A1	A0

The bit0 of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low. Upon a matched comparison of the device address, the Chip will output a zero. If not, the device will return to a standby state.

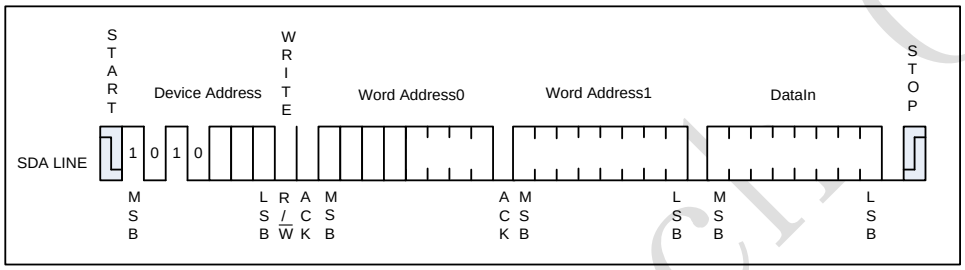
5. Instructions

5.1 Write Operations

5.1.1Byte Write

A write operation requires one 8-bit device address following the two-byte word address and acknowledgment. Upon receipt of this device address, the P24C32D will again respond with a “0” and then clock in the first 8-bit data. Following receipt of the 8-bit data word, the P24C32D will output a “0” and the master, such as a master, must terminate the write sequence with a STOP bit. And then the P24C32D enters an internally timed write cycle. All inputs are disabled during this write cycle and the P24C32D will not respond until the write is complete (Refer to Figure 5-1).

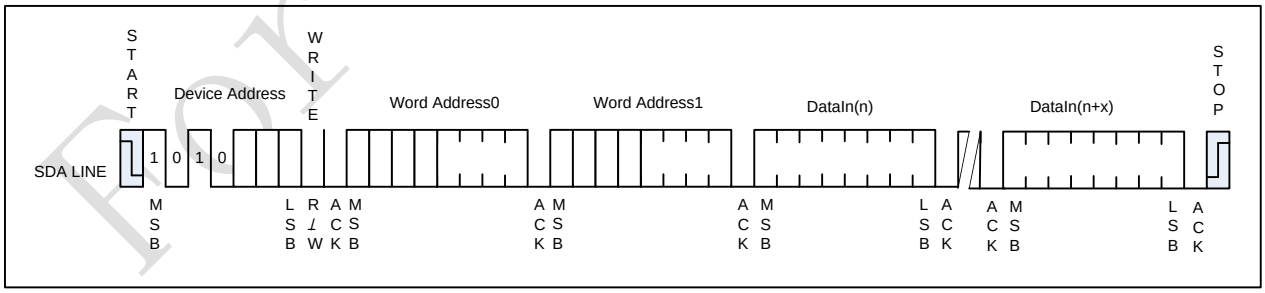
Figure 5-1 Byte Write



5.1.2 Page Write

A page write is initiated in the same way as a byte write. But the master does not send a STOP bit after the first data word is clocked in. Instead, after the P24C32D acknowledges receipt of the first data, the master can transmit more data continuously. The P24C32D will respond with a “0” after each data byte received. The master must terminate the page write sequence with a STOP bit.

Figure 5-2Page Write



The lowest five page address bits of the word address, the page address for P24C32D respectively, are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the page boundary is reached, the word address rolls over to the beginning of the same page. And previous data will be overwritten.

5.1.3 Acknowledge Polling

Once the internally timed write cycle has started, the P24C32D inputs are disabled and acknowledge polling can be initiated. This involves sending a START condition followed by the device address. The read/write bit is representative of the operation desired. Until the internal write cycle has completed will the device respond with a “0”, allowing the read or write sequence to continue.

5.1.4 Write Identification Page

The Identification Page (32bytes) is an additional page which can be written and later permanently locked in Read-only mode. It is written by the Write Identification Page instruction. This instruction uses the same protocol and format as Page Write (into memory array), except for the following differences:

- Device type identifier = 1011b
- Word Address bits A11/A10which must be ‘00’.
- Address bits A4~A0 define the byte address inside the Identification page for P24C32D respectively.

If the Identification page is locked, the data bytes transferred during the Write Identification Page instruction are not acknowledged (No-ACK).

5.1.5 Lock Identification Page

The Lock Identification Page instruction (Lock ID) permanently locks the Identification page in Read-only mode. The Lock ID instruction is similar to Byte Write (into memory array) with the following specific conditions:

- Device type identifier = 1011b
- Address bit A11A10 must be ‘01’; all other address bits are don’t care
- The data byte must be equal to the binary value xxxx xx1x, where x is don’t care

5.2 Read Operations

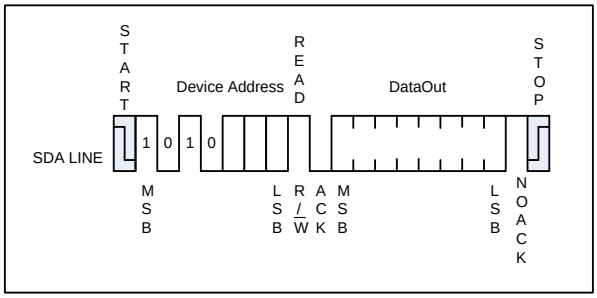
Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to “1”. There are three read operations: Current Address Read; Random Address Read and Sequential Read.

5.2.1 Current Address Read

The last address accessed during the last read or write operation is always incremented by one after the STOP bit of the last command. Then the Current Address Read instruction read data start from that address and increased by one after every data byte read. The address counter rolls over to the first byte of the first page if the last byte of the last memory page is encountered.

Once the device address with the read/write select bit set to “1” is clocked in and acknowledged by the device, the data at the current address is serially clocked out. The master does not respond with an input “0” but generate a STOP bit (Refer to Figure 5-3)。

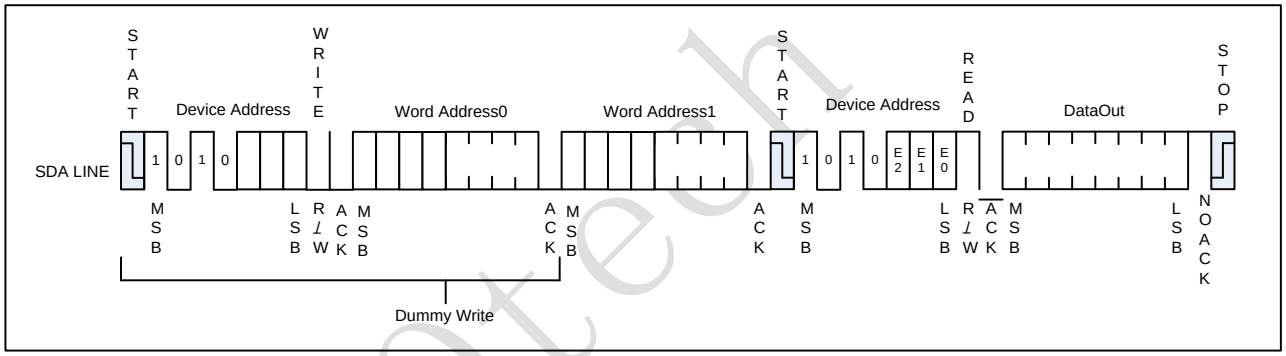
Figure 5-3 Current Address Read



5.2.2 Random Read

A Random Read requires a “dummy” byte write sequence to load in the word address. Once the device address and word address are clocked in and acknowledged by the device, the master must generate another START condition. The master now initiates a Current Address Read by sending a device address with the read/write select bit high. The device acknowledges the device address and serially clocks out the data word. The master does not respond with a “0” but generate a STOP bit (Refer to Figure 5-4).

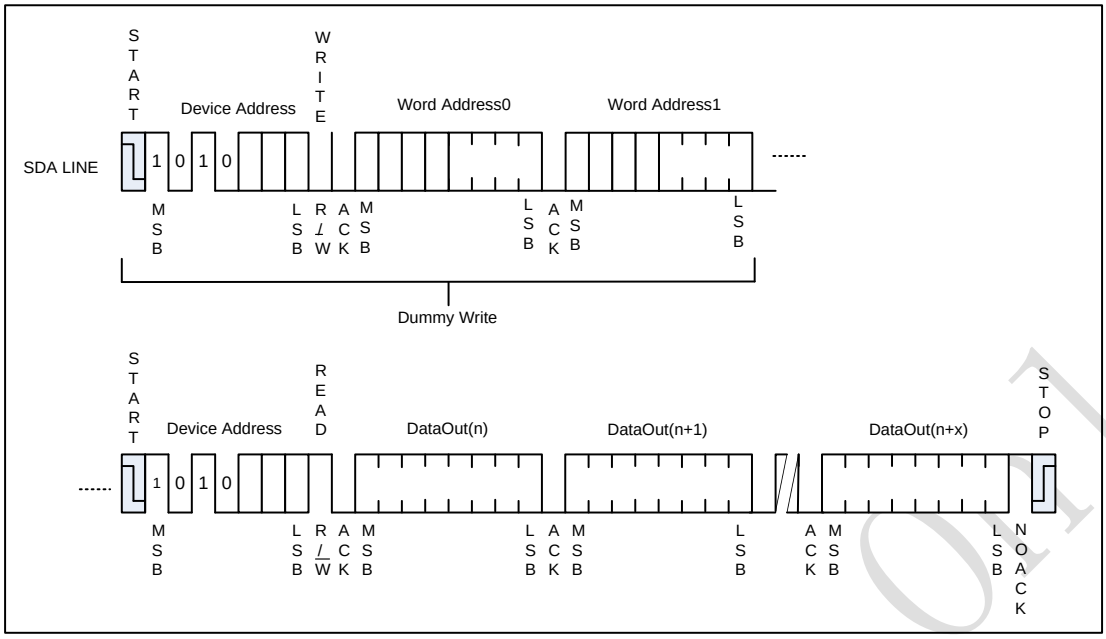
Figure 5-4 Random Read



5.2.3 Sequential Read

Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the master receives a data byte, it responds with acknowledge. As long as the device receives acknowledge, it will continue to increment the word address and serially clock out sequential data bytes. When the memory address limit (Max. address) is reached, the word address will roll-over and the Sequential Read will continue. The Sequential Read operation is terminated when the master does not respond with a “0” but generate a STOP bit (Refer to Figure 5-5)

Figure 5-5 Sequential Read



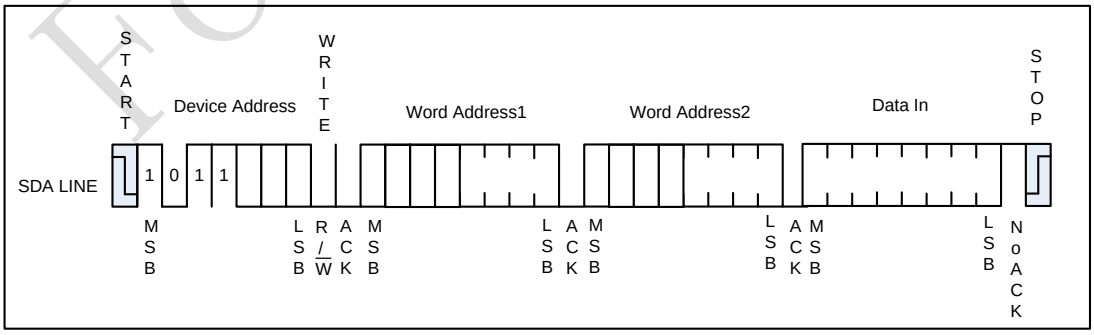
5.2.4 Read Identification Page

The Identification Page (16 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. The Identification Page can be read by Read Identification Page instruction. The instruction uses the same protocol and format as the Read Command (from memory array) with device type identifier defined as 1011b. The MSB address bits A7/A6 must be 0 while A5 is don't care, and the LSB address bits A4/A0 define the byte address inside the Identification Page. The number of bytes to read in the ID page must not exceed the page boundary (e.g. when reading the Identification Page from location 10d, the number of bytes should be less than or equal to 6, as the ID page boundary is 16 bytes).

5.2.5 Read the Lock Status

The locked status of the Identification page can be checked by transmitting an specific truncated command [Identification Page Write instruction + one data byte] to the device. The device returns an acknowledge bit if the Identification page is unlocked, otherwise a NoACK bit if the Identification page is locked.

Figure 5-5Lock Status Read (When Identification page locked, return NoACK after one data byte)



5.2.6 Read Serial Number

The Identification Page (16 bytes) is an additional page which can be written and (later)permanently locked in Read-only mode.

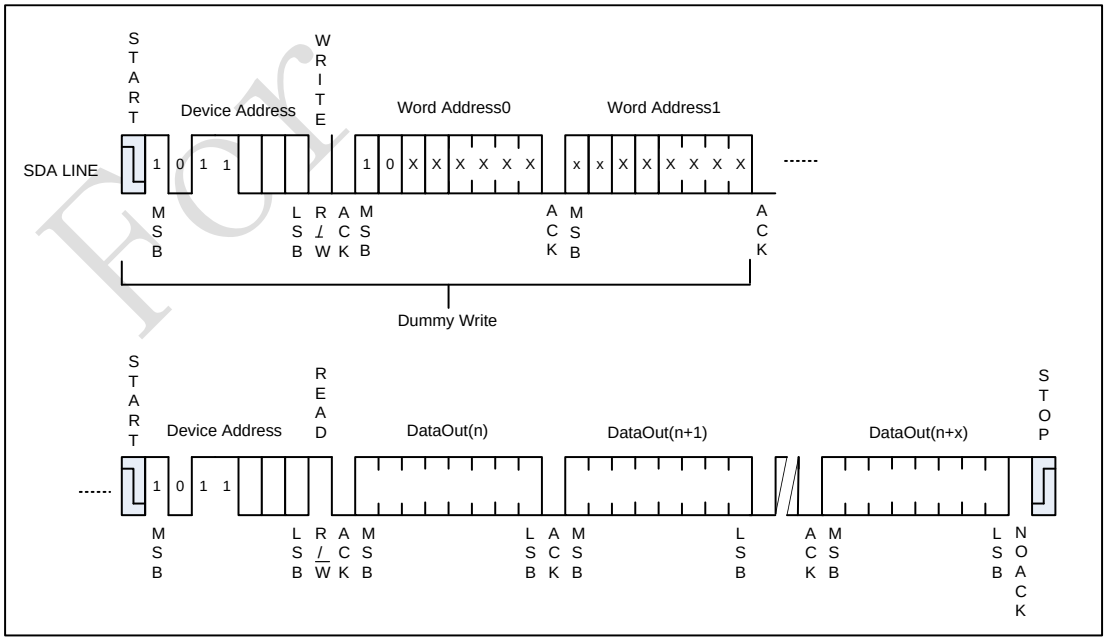
Reading the serial number is similar to the sequential read sequence but requires use of the device address Refer to Table 4-1 on page 9, a dummy write, and the use of a specific word address. The entire 128-bit value must be read from the starting address of the serial number block to guarantee a unique number.

Since the address pointer of the device is shared between the regular EEPROM array and the serial number block, a dummy write sequence, as part of a Random Read or Sequential Read protocol, should be performed to ensure the address pointer is set to zero. A Current Address Read of the serial number block is supported but if the previous operation was to the EEPROM array, the address pointer will retain the last location accessed, incremented by one. Reading the serial number from a location other than the first address of the block will not result in a unique serial number.

Additionally, the word address contains a '10' sequence in bit A7 and A6 of the word address, regardless of the intended address as depicted in Table 4-2 on page 9. If a word address other than '10' is used, then the device will output undefined data.
Example: If the application desires to read the first byte of the serial number, the word address input would need to be 0800h.

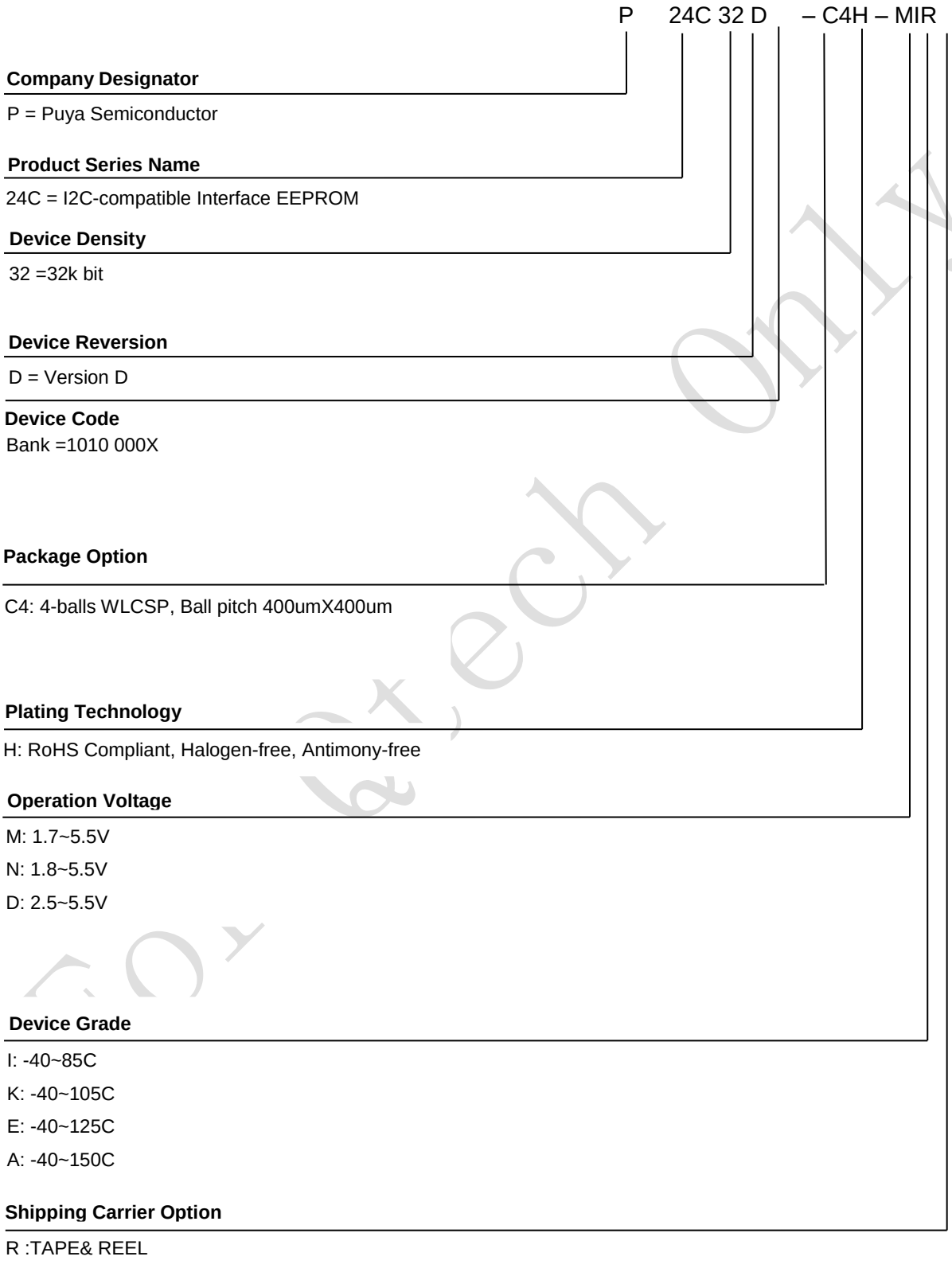
When the end of the 128-bit serial number is reached (16 bytes of data), continued reading of the extended memory region will result in an additional 16 bytes of 00h data. Upon reaching the end of the 16-byte extended memory region, the data word address will roll-over back to the beginning of the 128-bit serial number. The Serial Number Read operation is terminated when the master does not respond with a zero (ACK) and instead issues a STOP bit (Refer to Figure 5-6)

Figure 5-6 Sequential Read



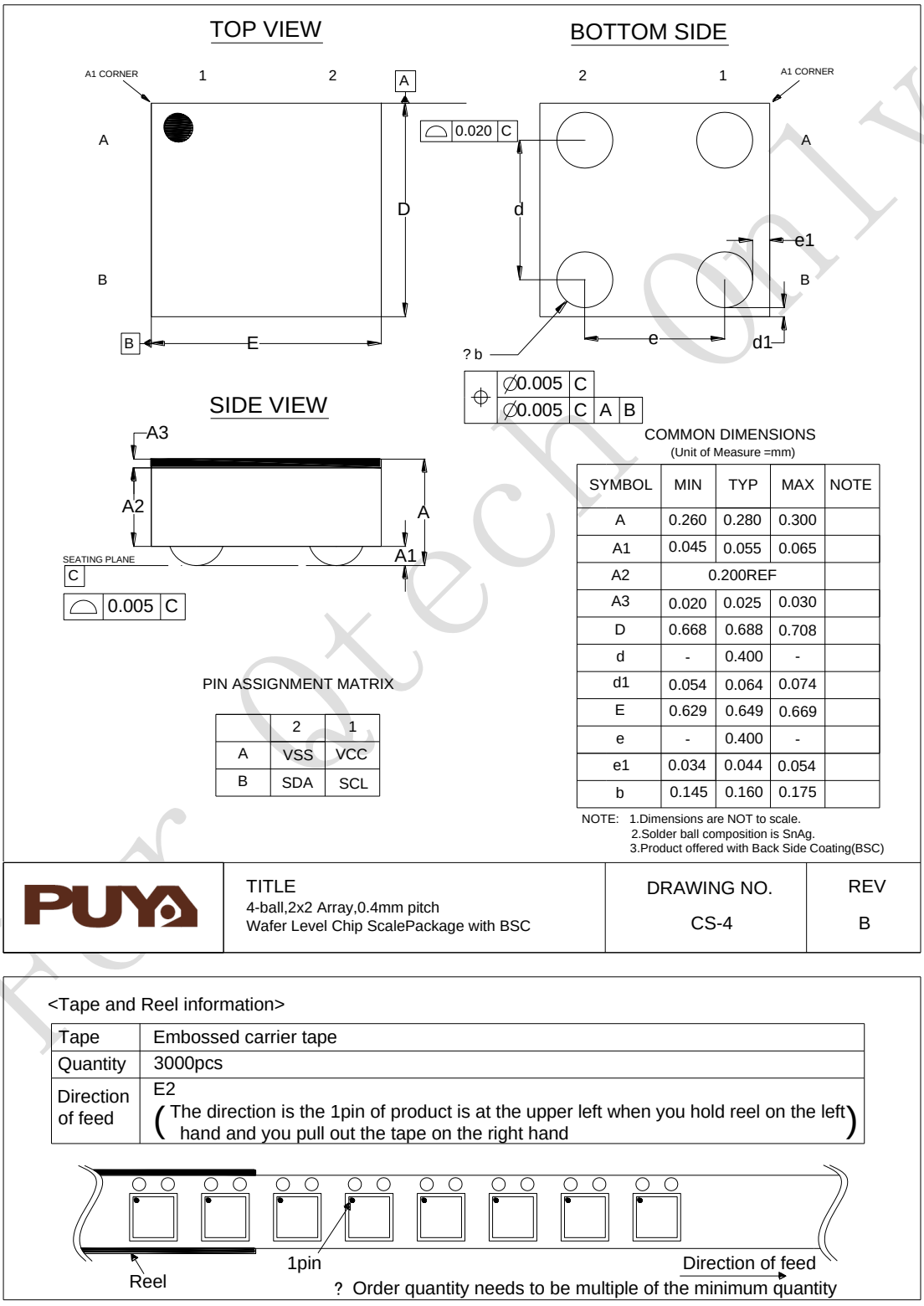
6.Ordering Code Detail

Example:



7.Package information

7.14-Balls WLCSP(Ball Pitch 400um*400um)



COMMON DIMENSIONS
(Unit of Measure =mm)

SYMBOL	MIN	TYP	MAX	NOTE
A	0.260	0.280	0.300	
A1	0.045	0.055	0.065	
A2		0.200REF		
A3	0.020	0.025	0.030	
D	0.668	0.688	0.708	
d	-	0.400	-	
d1	0.054	0.064	0.074	
E	0.629	0.649	0.669	
e	-	0.400	-	
e1	0.034	0.044	0.054	
b	0.145	0.160	0.175	

NOTE: 1.Dimensions are NOT to scale.
2.Solder ball composition is SnAg.
3.Product offered with Back Side Coating(BSC)

PIN ASSIGNMENT MATRIX

	2	1
A	VSS	VCC
B	SDA	SCL

	TITLE	DRAWING NO.	REV
PUYA	4-ball,2x2 Array,0.4mm pitch Wafer Level Chip ScalePackage with BSC	CS-4	B

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)

? Order quantity needs to be multiple of the minimum quantity

8. Revision History

Version	Content	Date
Rev1.0	Initial Release	2016-12-12

Puya Semiconductor Co., Ltd.