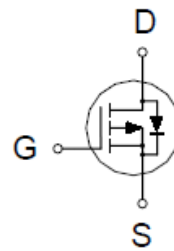
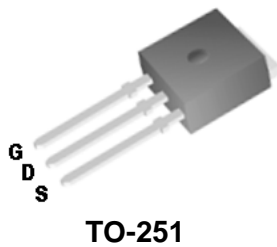


P2504EI

P-Channel Logic Level Enhancement Mode MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
-40V	25.8m Ω @ $V_{GS} = -10V$	-30A



ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	-40	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	$T_C = 25\text{ }^\circ\text{C}$	I_D	-30	A
	$T_C = 70\text{ }^\circ\text{C}$		-24	
Pulsed Drain Current ¹		I_{DM}	-65	
Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	42	W
	$T_C = 70\text{ }^\circ\text{C}$		27	
Operating Junction & Storage Temperature Range		T_J, T_{STG}	-55 to 150	$^\circ\text{C}$
Lead Temperature ($1/16$ " from case for 10 sec.)		T_L	275	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta JC}$		3	$^\circ\text{C} / \text{W}$
Junction-to-Ambient	$R_{\theta JA}$		75	

¹Pulse width limited by maximum junction temperature.

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ELECTRICAL CHARACTERISTICS (T_C = 25 °C, Unless Otherwise Noted)

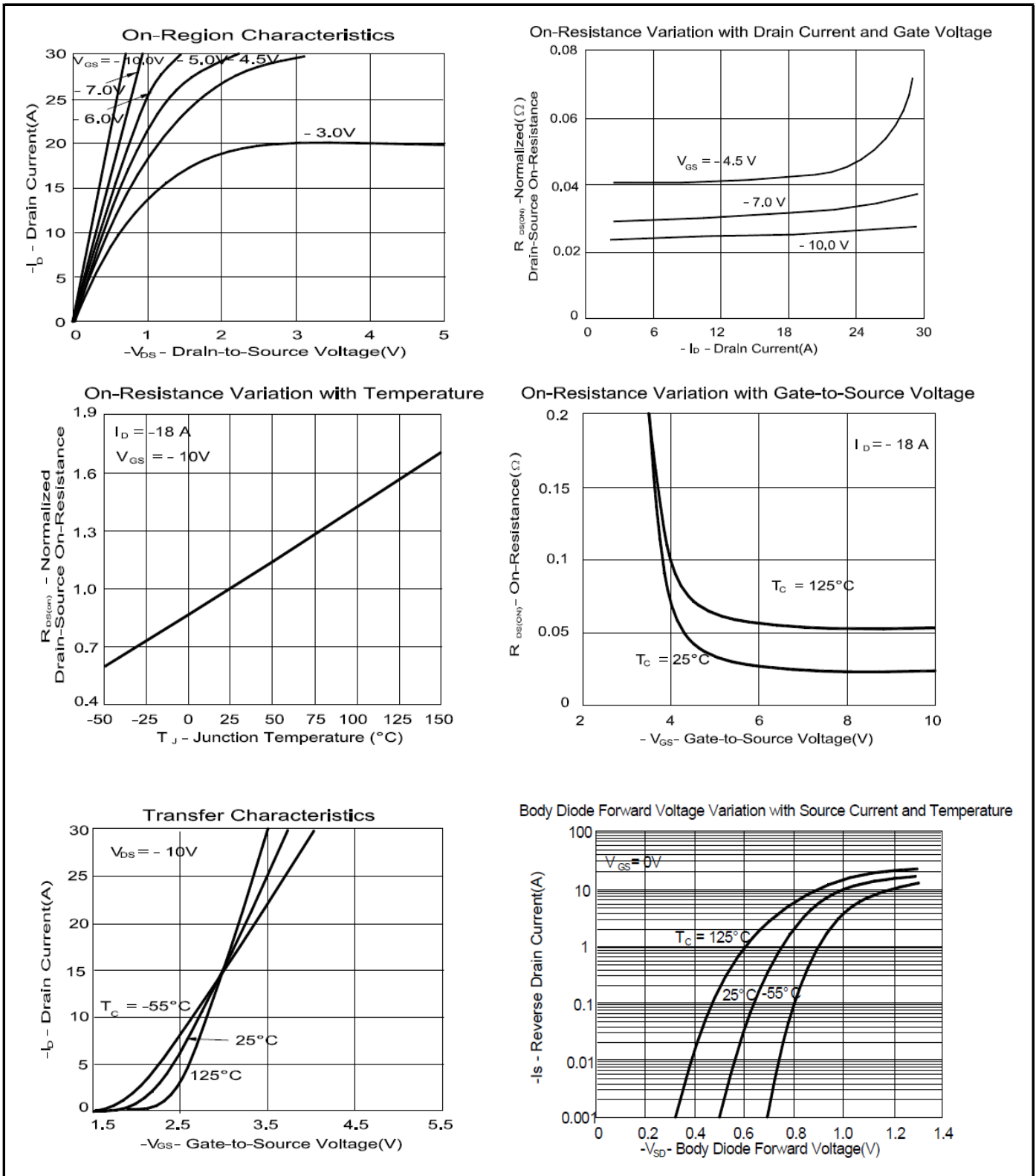
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250μA	-40			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	-1.2	-2.2	-3	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±250	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -32V, V _{GS} = 0V			1	μA
		V _{DS} = -30V, V _{GS} = 0V, T _J = 125 °C			10	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = -5V, V _{GS} = -10V	-65			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = -7V, I _D = -10A		30	40	mΩ
		V _{GS} = -10V, I _D = -18A		22	25.8	
Forward Transconductance ¹	g _{fs}	V _{DS} = -5V, I _D = -18A		20		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = -15V, f = 1MHz		1570		pF
Output Capacitance	C _{oss}			320		
Reverse Transfer Capacitance	C _{rss}			210		
Total Gate Charge ²	Q _g	V _{DS} = 0.5V _{(BR)DSS} , V _{GS} = -10V, I _D = -18A		29		nC
Gate-Source Charge ²	Q _{gs}			6		
Gate-Drain Charge ²	Q _{gd}			7		
Turn-On Delay Time ²	t _{d(on)}	V _{DS} = -20V, R _L = 1Ω, I _D ≅ -1A, V _{GS} = -10V, R _{GS} = 6Ω		12		nS
Rise Time ²	t _r			29		
Turn-Off Delay Time ²	t _{d(off)}			42		
Fall Time ²	t _f			33		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I _S				-18	A
Forward Voltage ¹	V _{SD}	I _F = I _S , V _{GS} = 0V			-1.3	V
Reverse Recovery Time	t _{rr}	I _F = -18A, di _F /dt = 100A / μS		29		nS
Reverse Recovery Charge	Q _{rr}				21	

¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

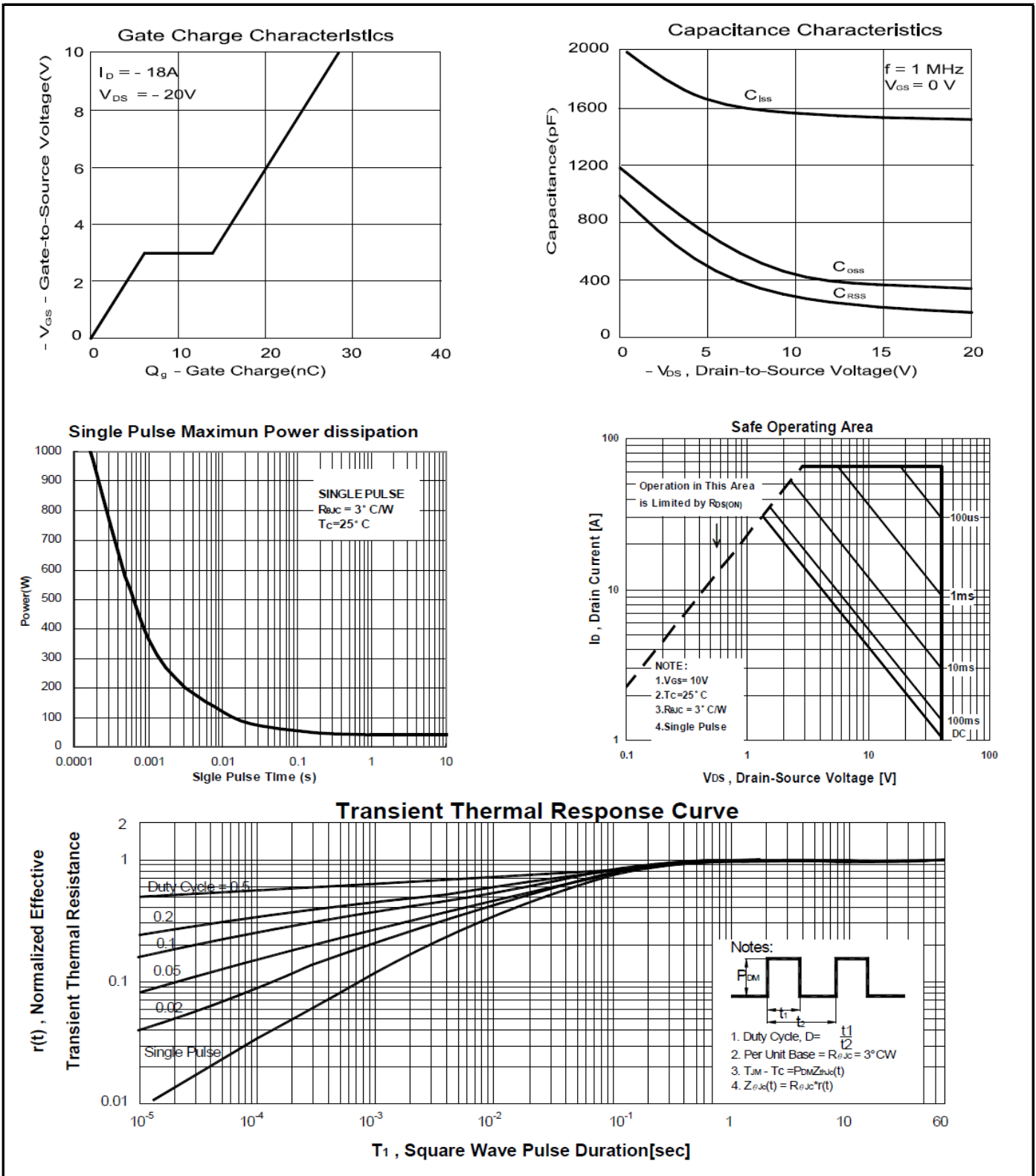
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Package Dimension

TO-251 MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	14	15	17.14	H	0.89		1.7
B	2.1	2.3	2.5	I	6.3		6.8
C	0.4	0.5	0.6	J	4.8		5.5
D	0.35	0.5	0.65	K	0.5	0.84	1.14
E	0.9	1.1	1.5	L	0.4	0.76	0.912
F	7		9.65	M		2.3	
G	5.3		6.22	N	1.4	2.16	2.23

