UNIKC Semiconductor

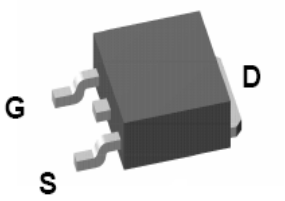
RoHS Compliant

P3003EDG

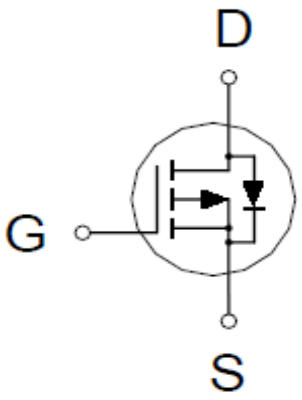
P-Channel Logic Level Enhancement Mode MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
-30V	30mΩ @V_{GS} = -10V	-18A



TO-252



ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C= 25 °C	I_D	-18	A
	T_C= 100 °C		-12	
Pulsed Drain Current[1]		I_{DM}	-30	
Power Dissipation	T_C= 25 °C	P_D	50	W
	T_C= 70°C		20	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta JC}$		2.5	°C / W
Junction-to-Ambient	$R_{\theta JA}$		70	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤1%

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ELECTRICAL CHARACTERISTICS (T_C = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1	-1.5	-3.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±250	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} =-24V, V_{GS} = 0V			1	μA
		V_{DS} =-20V, V_{GS} = 0V, T_J = 125°C			10	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = -5V, V_{GS} = -10V	-30			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} =-5V, I_D =-10A		42	52	mΩ
		V_{GS} =-10V, I_D =-18A		24	30	
Forward Transconductance[1]	g_{fs}	V_{DS} = -10V, I_D = -18A		16		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -10V, f = 1MHz		970		pF
Output Capacitance	C_{oss}			370		
Reverse Transfer Capacitance	C_{rss}			180		
Total Gate Charge[2]	Q_g	V_{DS} =0.5$V_{(BR)DSS}$, V_{GS}= -10V, I_D = -18A		28	40	nC
Gate-Source Charge[2]	Q_{gs}			6		
Gate-Drain Charge[2]	Q_{gd}			12		
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DS} =-15V ,I_D ≅ -10A, V_{GS}=-10V,R_{GS}=6Ω		20		nS
Rise Time[2]	t_r			17		
Turn-Off Delay Time[2]	$t_{d(off)}$			180		
Fall Time[2]	t_f			75		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				-18	A
Forward Voltage[1]	V_{SD}	I_F = -1A, V_{GS} = 0V			-1.2	V
Reverse Recovery Time	t_{rr}	I_F = -5A, dI_F/dt = 100A / μS		15.5		nS
Reverse Recovery Charge	Q_{rr}			7.9		nC

[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[2]Independent of operating temperature.

[3]Pulse width limited by maximum junction temperature.

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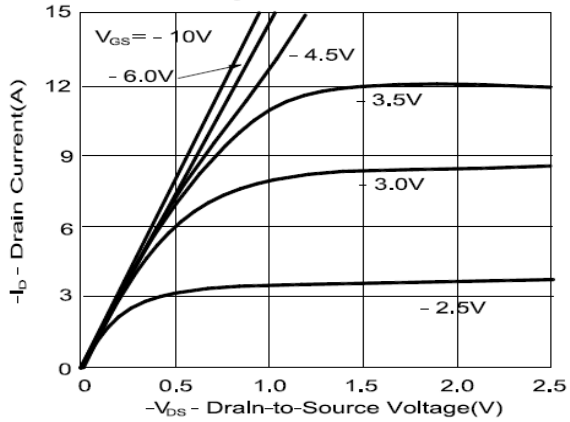
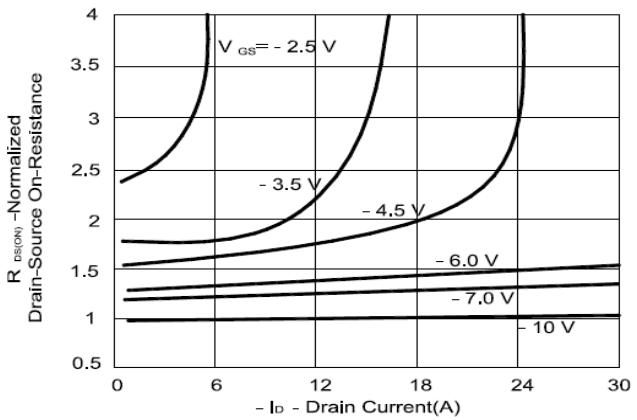
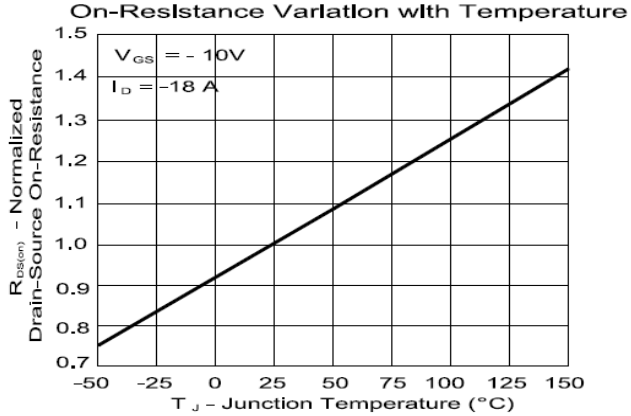
On-Region Characteristics



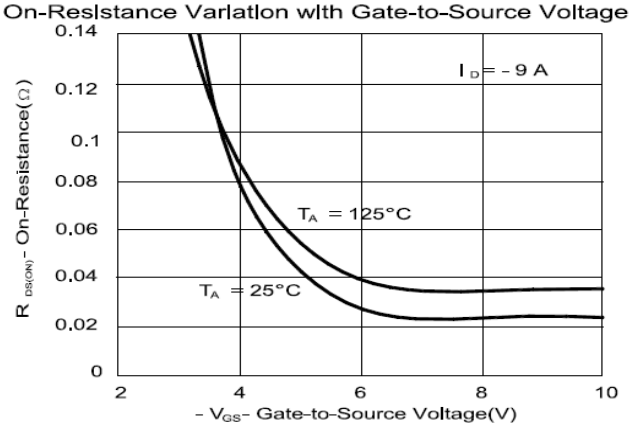
On-Resistance Variation with Drain Current and Gate Voltage



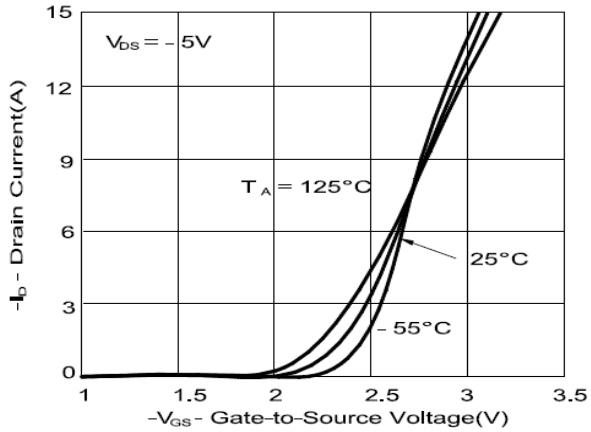
On-Resistance Variation with Temperature



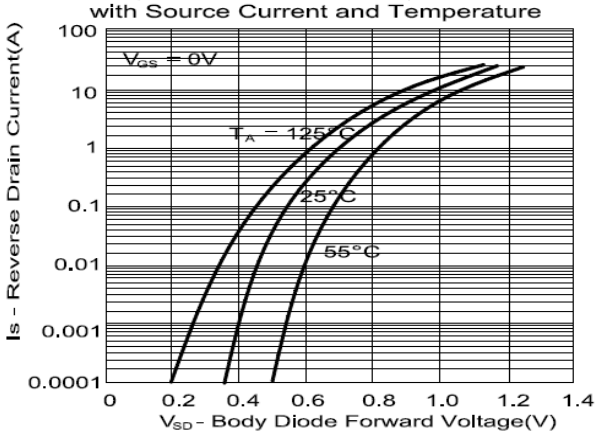
On-Resistance Variation with Gate-to-Source Voltage



Transfer Characteristics



Body Diode Forward Voltage Variation with Source Current and Temperature



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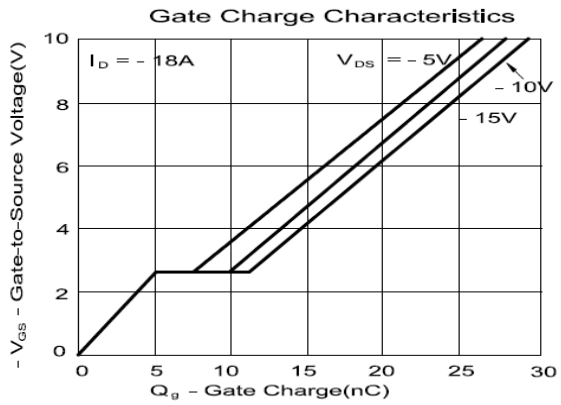

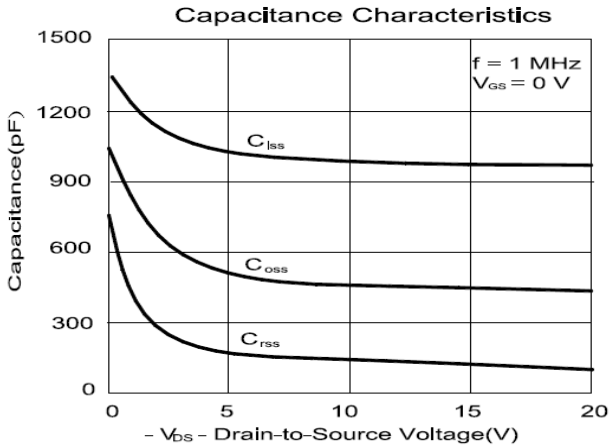

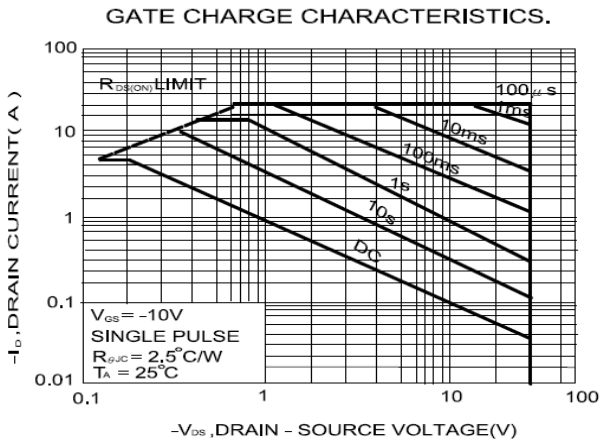

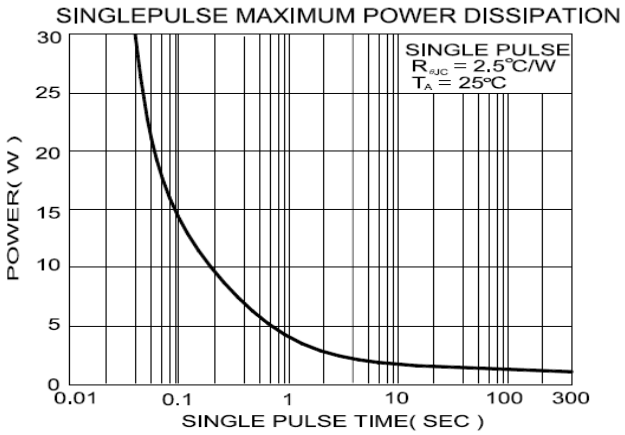

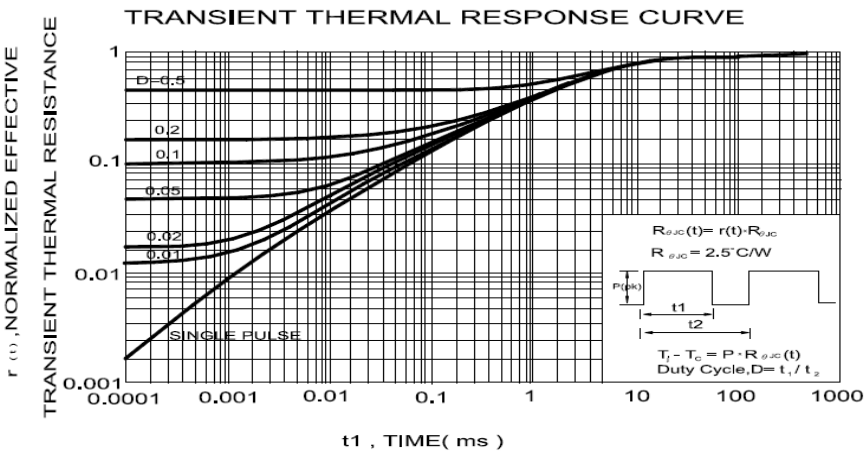

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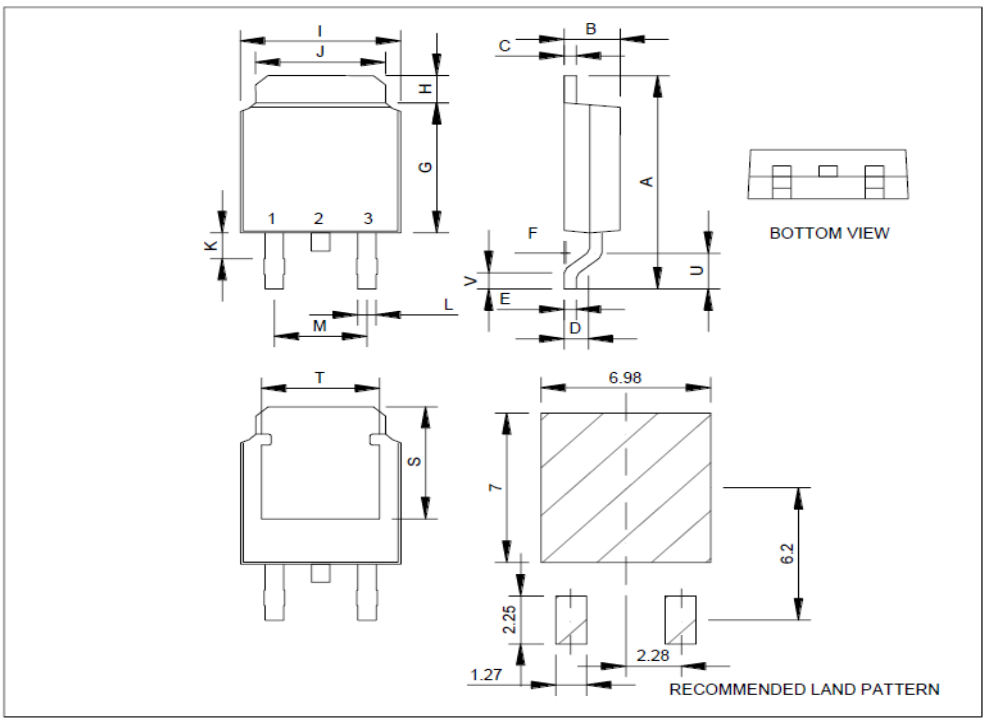
Package Dimension

TO-252 (DPAK) MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	8.9	10	10.41	J	4.8		5.64
B	2.1	2.2	2.4	K	0.15		1.1
C	0.4	0.5	0.61	L	0.4	0.76	0.89
D	0.82	1.2	1.5	M	4.2	4.58	5
E	0.4	0.5	0.61	S	4.9	5.1	5.3
F	0		0.2	T	4.6	4.75	5.44
G	5.3	6.1	6.3	U	1.4		1.78
H	0.9		1.7	V	0.55	1.25	1.7
I	6.3	6.5	6.8				



*因为各家封装模具不同而外观略有所差异，不影响电性及Layout。