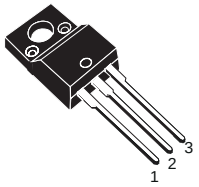
STP30NS15LFP

N-CHANNEL 150V - 0.085 Ω - 10A TO-220FP
MESH OVERLAY™ POWER MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STP30NS15LFP	150 V	<0.1Ω	10 A

- TYPICAL $R_{DS}(on)$ = 0.085Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED

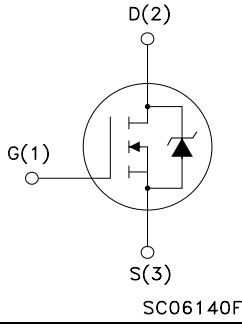


TO-220FP

DESCRIPTION

Using the latest high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of power MOSFETs with outstanding performances. The new patent pending strip layout coupled with the Company's proprietary edge termination structure, gives the lowest RDS(on) per area, exceptional avalanche and dv/dt capabilities and unrivalled gate charge and switching characteristics.

INTERNAL SCHEMATIC DIAGRAM



APPLICATIONS

- SWITCHING "S" CAPACITOR

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	150	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	150	V
V_{GS}	Gate- source Voltage	± 15	V
I_D	Drain Current (continuous) at T_C = 25°C	10	A
I_D	Drain Current (continuous) at T_C = 100°C	7	A
I_{DM}(•)	Drain Current (pulsed)	40	A
P_{tot}	Total Dissipation at T_C = 25°C	30	W
	Derating Factor	0.2	W/°C
E_{AS}(1)	Single Pulse Avalanche Energy	300	mJ
dv/dt (2)	Peak Diode Recovery voltage slope	2.4	V/ns
T_{stg}	Storage Temperature	-55 to 175	°C
T_j	Operating Junction Temperature		

(•) Pulse width limited by safe operating area.

(1) Starting T_j = 25 ºC, I_D = 15A, V_{DD}= 75V
(2) I_{SD} ≤35A, di/dt ≤300A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_j ≤ T_{JMAX}.

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case	Max	5	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	62.5	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	Typ	300	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	150			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating T_C = 125°C			1 10	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 15V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} I_D = 250 µA	1	2	3	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10 V I_D = 5 A V_{GS} = 5 V I_D = 5 A		0.085 0.1	0.1 0.112	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	V_{DS} = 20 V I_D = 7 A		6		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		1080 170 105		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 75 V I_D = 5 A R_G = 4.7 Ω V_{GS} = 4.5 V (Resistive Load, Figure 1)		25 95		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD}=120V I_D=10A V_{GS}=5V (see test circuit, Figure 2)		40 7.5 20	54	nC nC nC

SWITCHING OFF

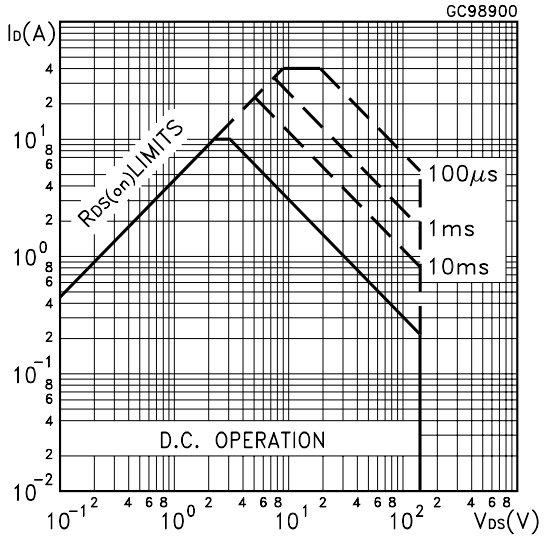
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	V_{DD} = 75 V I_D = 5 A R_G = 4.7Ω, V_{GS} = 5 V (Resistive Load, Figure 1)		55 30		ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	V_{clamp} = 120 V I_D = 10 A R_G = 4.7Ω, V_{GS} = 4.5 V (Inductive Load, Figure 3)		15 30 50		ns ns ns

SOURCE DRAIN DIODE

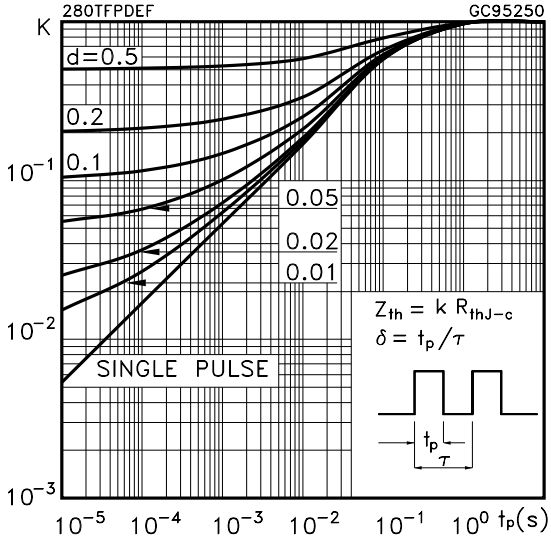
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (•)	Source-drain Current Source-drain Current (pulsed)				10 40	A A
V_{SD} (*)	Forward On Voltage	I_{SD} = 10 A V_{GS} = 0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 10 A di/dt = 100A/µs V_r = 30 V T_j = 150°C (Inductive Load, Figure 3)		160 950 12		ns nC A

(*)Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
(•)Pulse width limited by safe operating area.

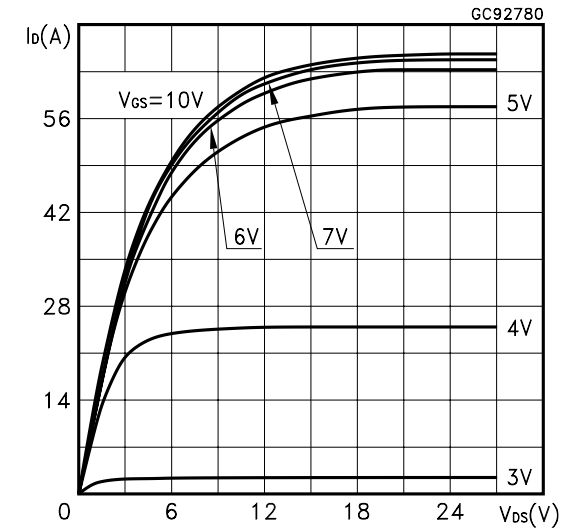
Safe Operating Area



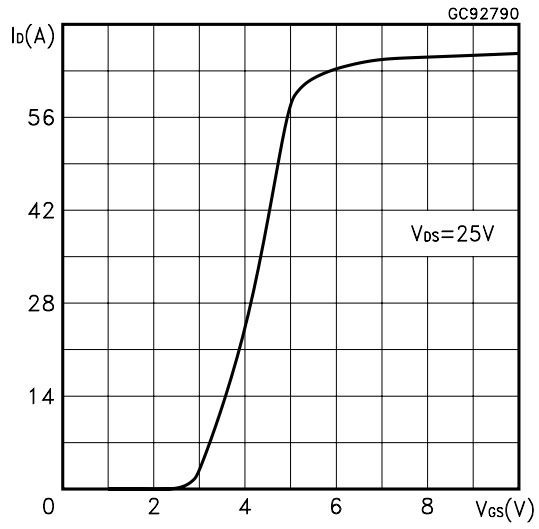
Thermal Impedance



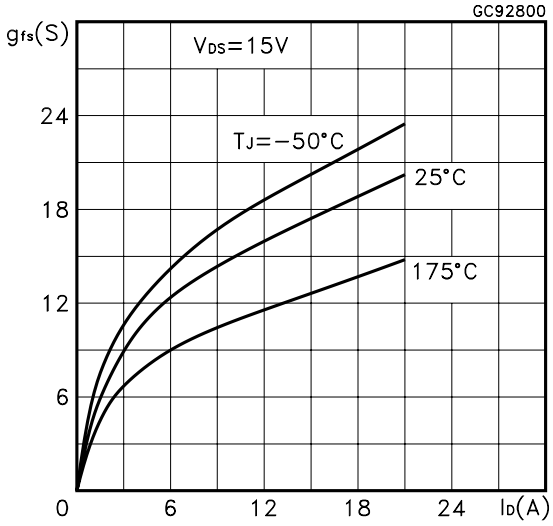
Output Characteristics



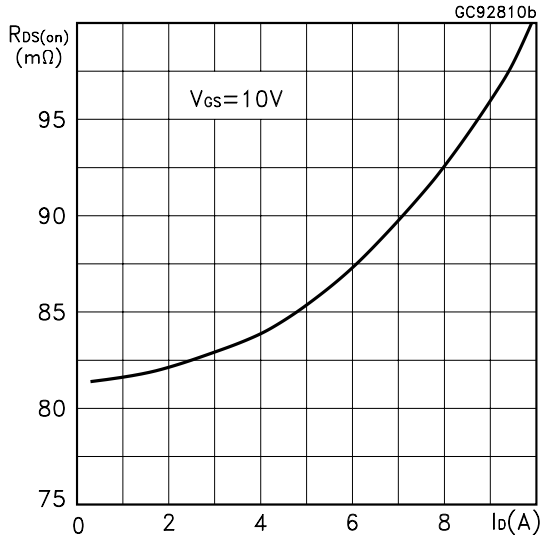
Transfer Characteristics



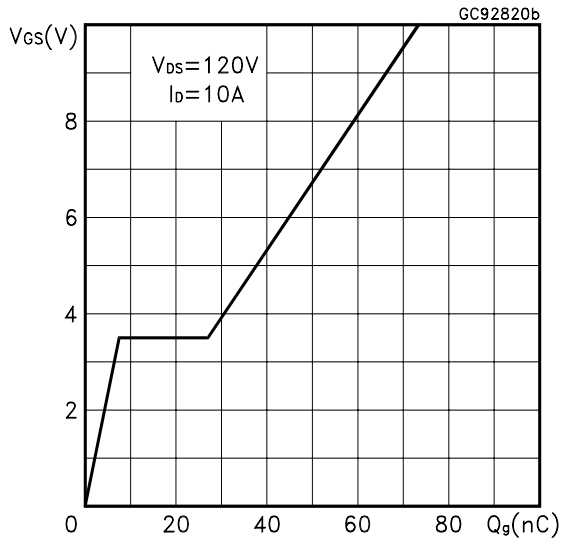
Transconductance



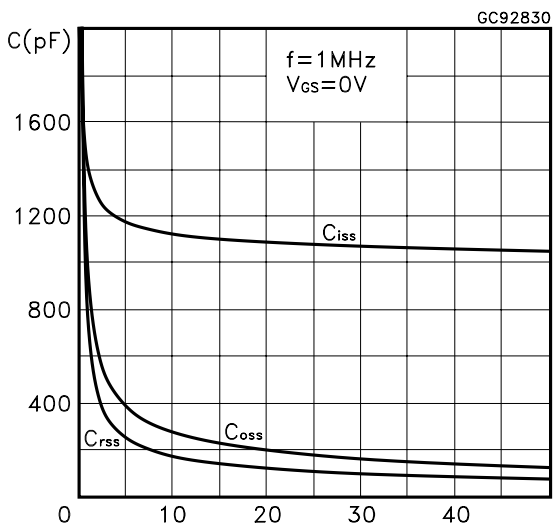
Static Drain-source On Resistance



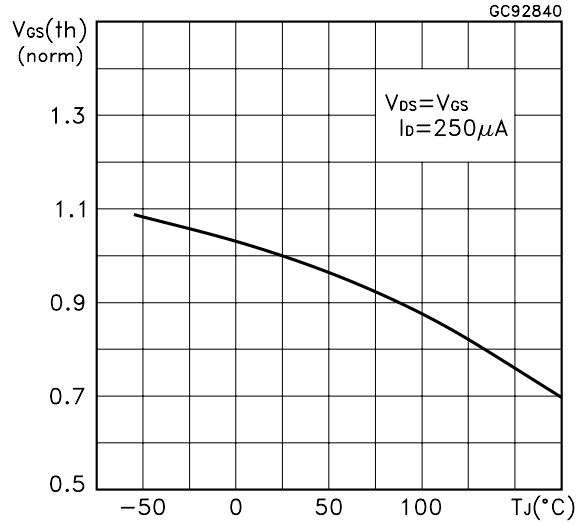
Gate Charge vs Gate-source Voltage



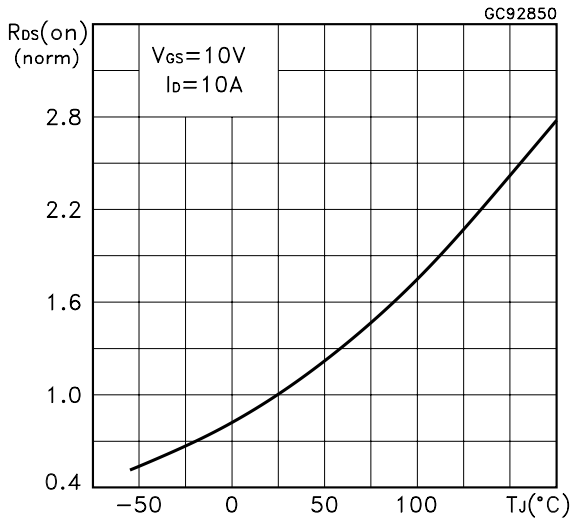
Capacitance Variations



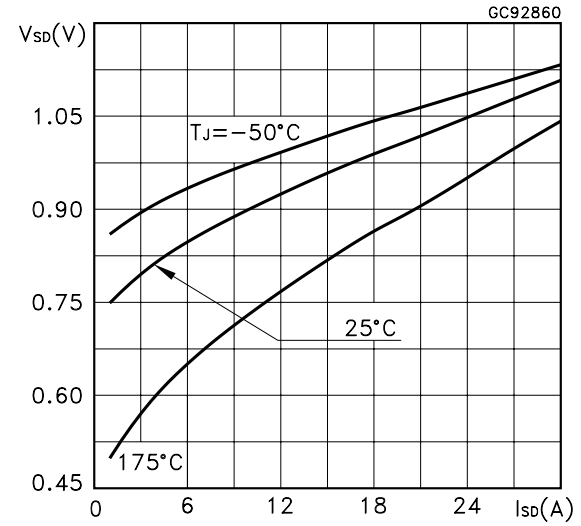
Normalized Gate Threshold Voltage vs Temperature



Normalized on Resistance vs Temperature



Source-drain Diode Forward Characteristics



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Normalized Breakdown Voltage vs Temperature

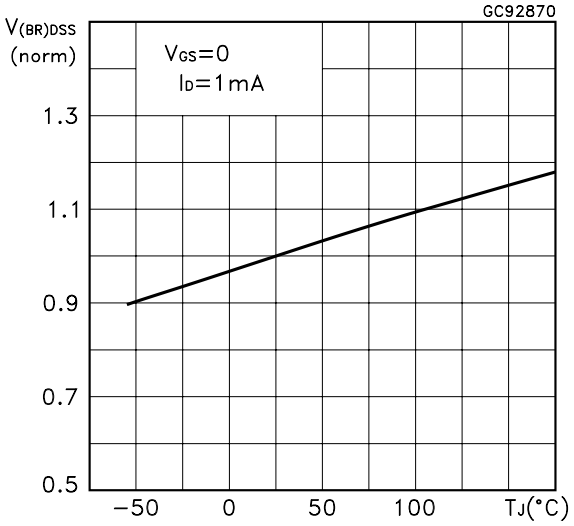

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Fig. 1: Switching Times Test Circuits For Resistive Load

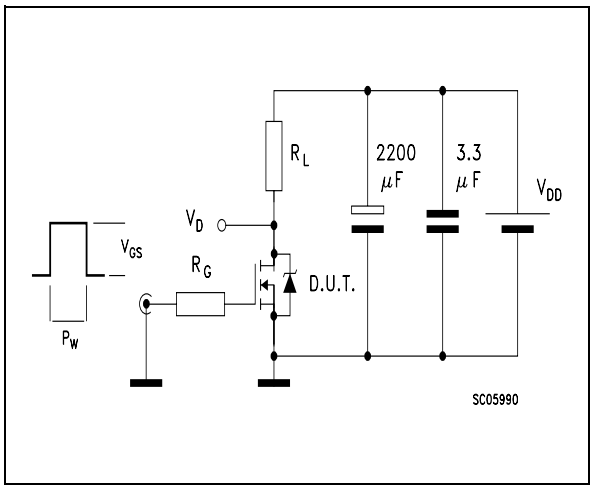


Fig. 2: Gate Charge test Circuit

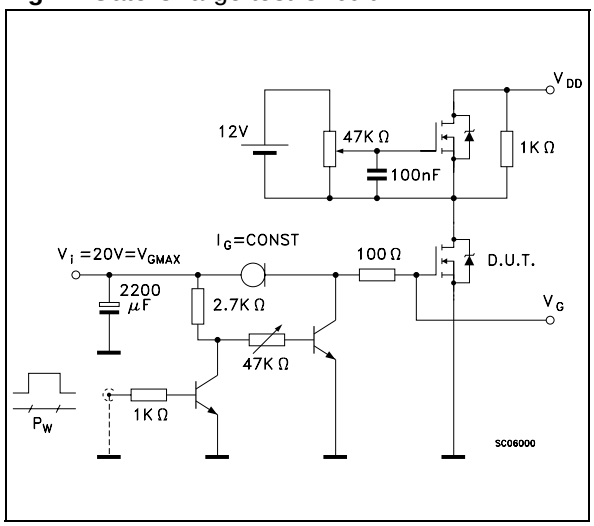
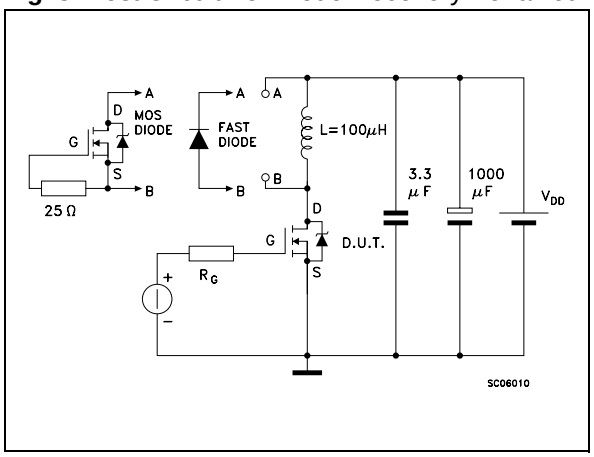
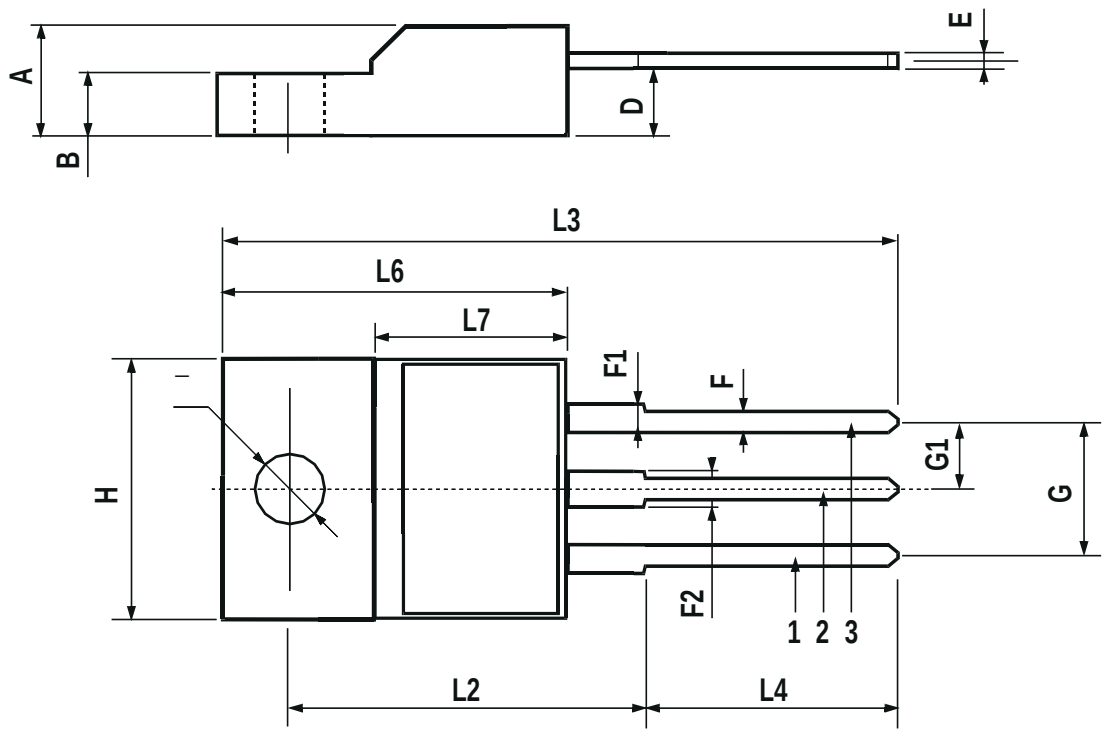


Fig. 3: Test Circuit For Diode Recovery Behaviour



TO-220FP MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	0.385		0.417
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



TO-220FP(023Y) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.009		0.106
C	1		1.4	0.039		0.055
D	2.4		2.75	0.094		0.108
E	0.4		0.7	0.015		0.027
F	0.75		1	0.029		0.039
F1	1.15		1.7	0.045		0.066
F2	1.15		1.7	0.045		0.066
G	4.68		5.48	0.184		0.215
G1	2.24		2.84	0.088		0.111
H	10		10.4	0.393		0.409
L1	18.4		19.2	0.724		0.755
L2		16			0.629	
L3	29		30	1.14		1.18
L4	15.3		16.1	0.60		0.63
L5		3.4			0.133	
L6	15.9		16.4	0.625		0.665
L7	9		9.3	0.354		0.366
L8	22.5		23.6	0.885		0.929
M	4.6		5.4	0.181		0.212
N	2.29		3.29	0.090		0.129
Dia	3		3.2