Version : *Preliminary*

TECHNICAL SPECIFICATION

MODEL NO.：P35EN1A001

☐Customer's Confirmation

Date

By

☐PVI's Confirmation

Confirmed By

Prepared By

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Date : Feb. 22, 1999

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TECHNICAL SPECIFICATION

CONTENTS

1. Application

This target specification applies to 3.5" color TFT-LCD panel. The 3.5” color TFT LCD panel is designed for camcorder, video phone application and other electronic products which require high quality flat panel displays.

2. Features

. No controller chip is necessary

. Compatible with NTSC or PAL system

. High Resolution：140400 Dots (600 × 234)

. High transmittance Ratio： 8.0 %

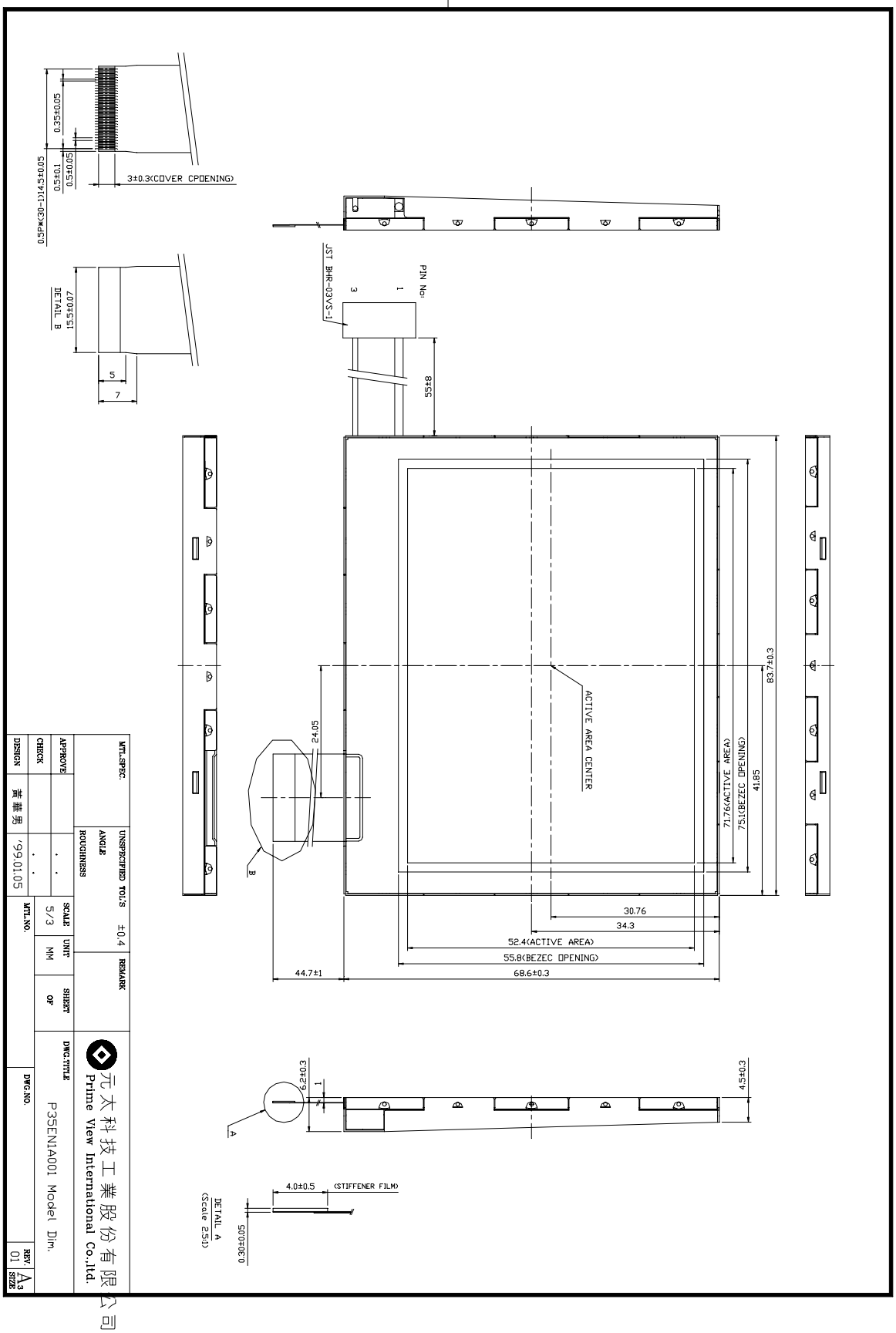
. Optimum Viewing Direction： 6 o’clock

. Up/ Down and Left/Right Image Reversion

3. Mechanical Specifications

Parameter	Specifications	Unit
Screen Size	3.5 (diagonal)	inch
Display Format	600×234	dot
Active Area	71.7 (H) X 52.4(V)	mm^2
Dot Pitch	0.119 (H)×0.224 (V)	mm^2
Pixel Configuration	Delta	
Outline Dimension	See Mechanical Drawing	mm^3
Weight	59	g

4. Mechanical Drawing



5. Input / Output Terminals

Pin No	Symbol	I/O	Description	Remark
1	V_{COM}	I	Common Electrode Voltage	Note 5-1
2	V_{BBA}	I	Supply Voltage for Level Shifter (Low Level)	Note 5-2
3	NC		No Connection	
4	V_{BBC}	I	Supply voltage for panel	Note 5-2
5	V_{SS}	I	Ground for panel	
6	V_{CC}	I	Supply Voltage for Level Shifter (High Level)	Note 5-4
7	V_{PIN}	I	Pulse high level for Level Shifter (High Level)	Note 5-5
8	V_{MIN}	I	Pulse low level for Level Shifter (Low Level)	Note 5-5
9	FRP	O	Control Signal for Video Inversion	
10	$\overline{VSY}$	I/O	Vertical Sync.	
11	$\overline{HSY}$	I/O	Horizontal Sync.	
12	C_{SYNC}	I	Composite Sync.	
13	PD	O	Phase Detector	Note 5-6
14	OSC	I	Clock Input for LC Oscillator	Note 5-6
15	V_{DD}	I	Supply Voltage for Logic Circuit	Note 5-3
16	CKC	I	Control Pin for Select I/O Signal	Note 5-12
17	UD	I	Up / Down Control	Note 5-11
18	LR	I	Left / Right Shift Control	Note 5-7
19	NP	I	NTSC / PAL Selector	Note 5-8
20	V_B	I	Video Input B	
21	V_G	I	Video Input G	
22	V_R	I	Video Input R	
23	GND	I	Ground for High voltage logic	
24	GND	I	Ground for logic	
25	DV_{EE}	I	Voltage supply for source driver high logic	Note 5-9
26	C_{COM}	I	Reference for Sample and Hold	Note 5-10
27	AV_{EE}	I	Voltage supply for sample & hold	Note 5-9
28	GND	I	Ground	
29	OV_{EE}	I	Voltage supply for operation amplifier	Note 5-9
30	VP+	I	Pre-charge high level	Note 5-9

Note 5-1：V_{COM} should be adjusted accurately to get the best contrast ratio.

Note 5-2：V_{BBA},V_{BBC} = -5V (Typ.)

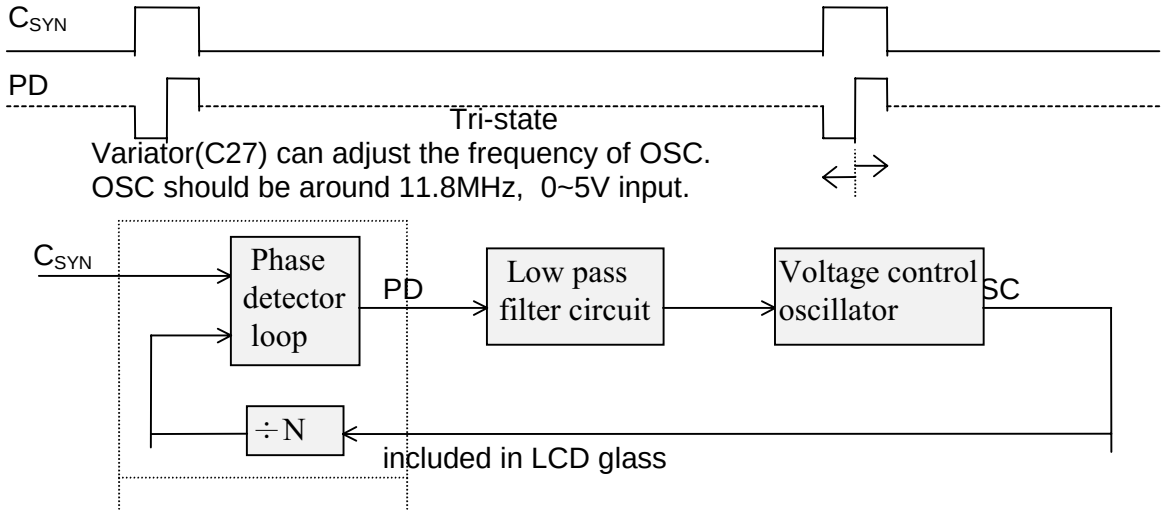
Note 5-3：V_{DD},PV_{DD} = +5V (Typ.)

Note 5-4：V_{CC}=+20V(Typ.)

Note 5-5：V_{PIN} must be more positive than V_{MIN}.

Pin	Symbol	min	Typ.	Max.	Unit
7	V_{PIN}	12	13	14	V
8	V_{MIN}	5	6	7	V

Note 5-6：PD output(0~5V range) from phase detector loop which is included in source driver.



Note 5-7：Left / Right SHIFT .

Note 5-8：Hi (+5V) for NTSC；Low (0V) for PAL.

Note 5-9：DV_{EE},AV_{EE},OV_{EE} and VP+ all equal to +14V

Note 5-10：C_{COM}≒+5V (Typ.)

Note 5-11：UP / Down Shift

Note 5-12；Pin 16(CKC) can select the function for Pin 11($\overline{\text{HSY}}$) and Pin 10($\overline{\text{VSY}}$).

CKC	$\overline{\text{HSY}}$	CSY	$\overline{\text{VSY}}$
Hi	$\overline{\text{HSY}}$ Output	CSY Input	$\overline{\text{VSY}}$ Output
Low	External $\overline{\text{HSY}}$ Input	External Clock Input	External $\overline{\text{VSY}}$ Input

6.Absolute Maximum Ratings:

GND = 0 V， Ta = 25 ℃

Parameter		Symbol	MIN.	MAX.	Unit	Remark
Supply Voltage for Source Driver		DV_{EE} ,AV_{EE} OV_{EE} ,VP+	0	+16	V	
Supply Voltage for Gate Driver	H Level	V_{CC}	0	+26	V	
	L Level	V_{BBA},V_{BBC}	-7	+20	V	
Supply voltage for controller		V_{DD}	0	+6.5	V	
DC bias voltage of common electrode		Vcom	+2	+6	V	
Analog input signals		V_B,V_R,V_G	0	+12	V	

7. Electrical Characteristics

7-1) Recommended Operating Conditions:

A) Driving for TFT-LCD panel

GND = 0V， Ta = 25 ℃

Parameter		Symbol	MIN.	TYP	MAX.	Unit	Remark
Supply voltage for source driver		DV_{EE},AV_{EE} OV_{EE},VP+	+13.5	+14	+14.5	V	
Supply voltage	H Level	V_{CC}	+19	+20	+24	V	
for gate driver	L level	V_{BBA},V_{BBC}	-5.5	-5	-4	V	
Supply voltage for controller		V_{DD}	+4.7	+5	+5.3	V	
Analog input	Amplitude	V_B,V_R,V_G	+1.12		12	V	
voltage	DC component		＋4	＋6	＋8	V	

B) Driving for Backlight

Ta= 25 ℃

Parameter	Min.	Typ.	Max.	Unit	Remark
Lamp voltage		225		Vrms	
Lamp current		3.5		mA	
Lamp frequency		35		KHz	

7-2) Power Consumption

Ta= 25 ℃

Parameter	Conditions	TYP.	Unit	Remark
Current for V_{CC}	V_{CC} = +20V	2.3	mA	
Current for V_{BBA}	V_{BBA} = -5V	2.1	mA	
Current for V_{BBC}	V_{BBC} = -5V	0.05	mA	
Current for DV_{EE}	DV_{EE} = +14V	0.54	mA	
Current for AV_{EE}	AV_{EE} = +14V	3.0	mA	
Current for OV_{EE}	OV_{EE} = +14V	3.7	mA	
Current for V_{DD}	V_{DD} = +5V	5.7	mA	
LCD Panel Power Consumption		0.19	W	
Backlight Power Consumption		0.85	W	

7-3) Input / Output Timing

Parameter		Symbol	MIN.	TYP.	MAX.	Unit	Remarks
Horizontal Sync. Output Pulse	Width	T_{HO}	4.2	4.7	5.2	μs	
	Phase Difference	T_{HP}	0	2		μs	
	Rising Time	T_{HR}	-	-	0.5	μs	
	Falling Time	T_{HF}	-	-	0.5	μs	
Vertical Sync. Output Pulse	Width	T_{VO}	-	4H	-	μs	H=1/15.75KHZ
	Phase Difference	T_{VPO}	-	1H	-	μs	odd field
	Phase Difference	T_{VPE}	-	1.5H	-	μs	even field
	Rising Time	T_{VR}	-	-	2	μs	
	Frequency	f_{FRP}	7.67	7.87	8.07	KH_Z	
Polarity Alternating Signal	Delay time	T_{FD}	-	-	4	μs	
	Falling Time	T_{VF}	-	-	2	μs	

7-4) Display Time Range

A) When sync. signal of NTSC system is applied.

a) Horizontally

12.6 ~ 63.39 μs.

b) Vertical

19 ~ 253 H

B) When sync. signal of PAL system is applied.

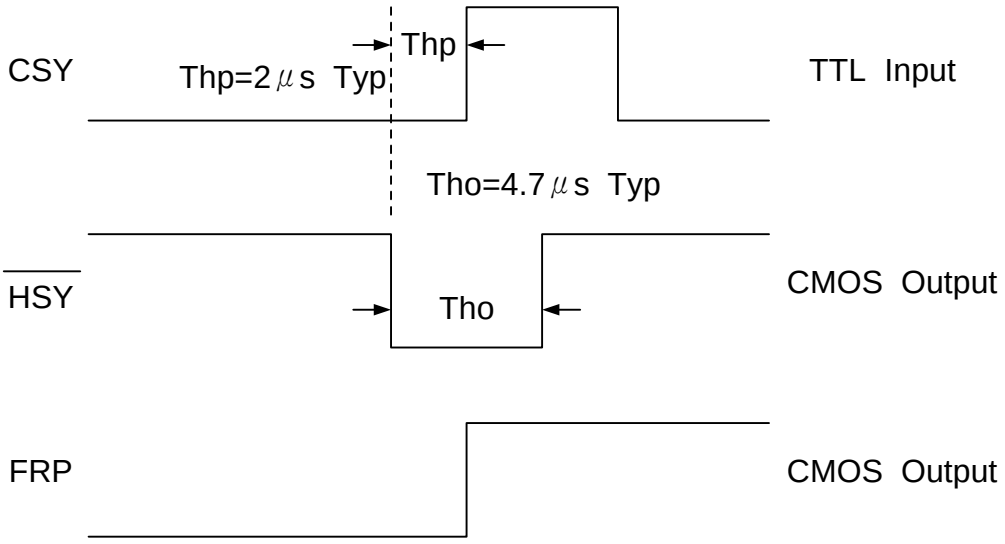
a) Horizontally

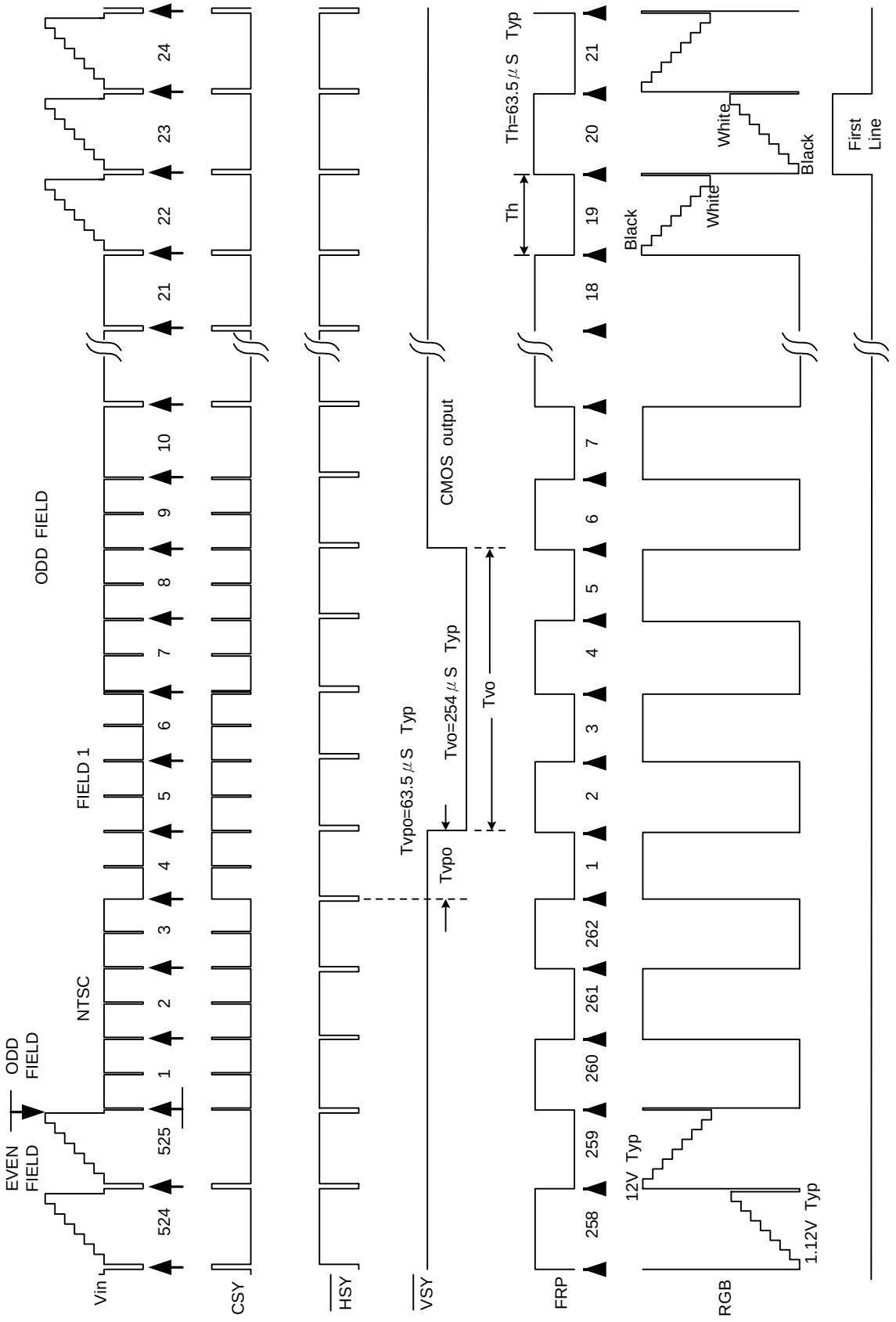
13.0 ~ 63.8 μs .

b) Vertical

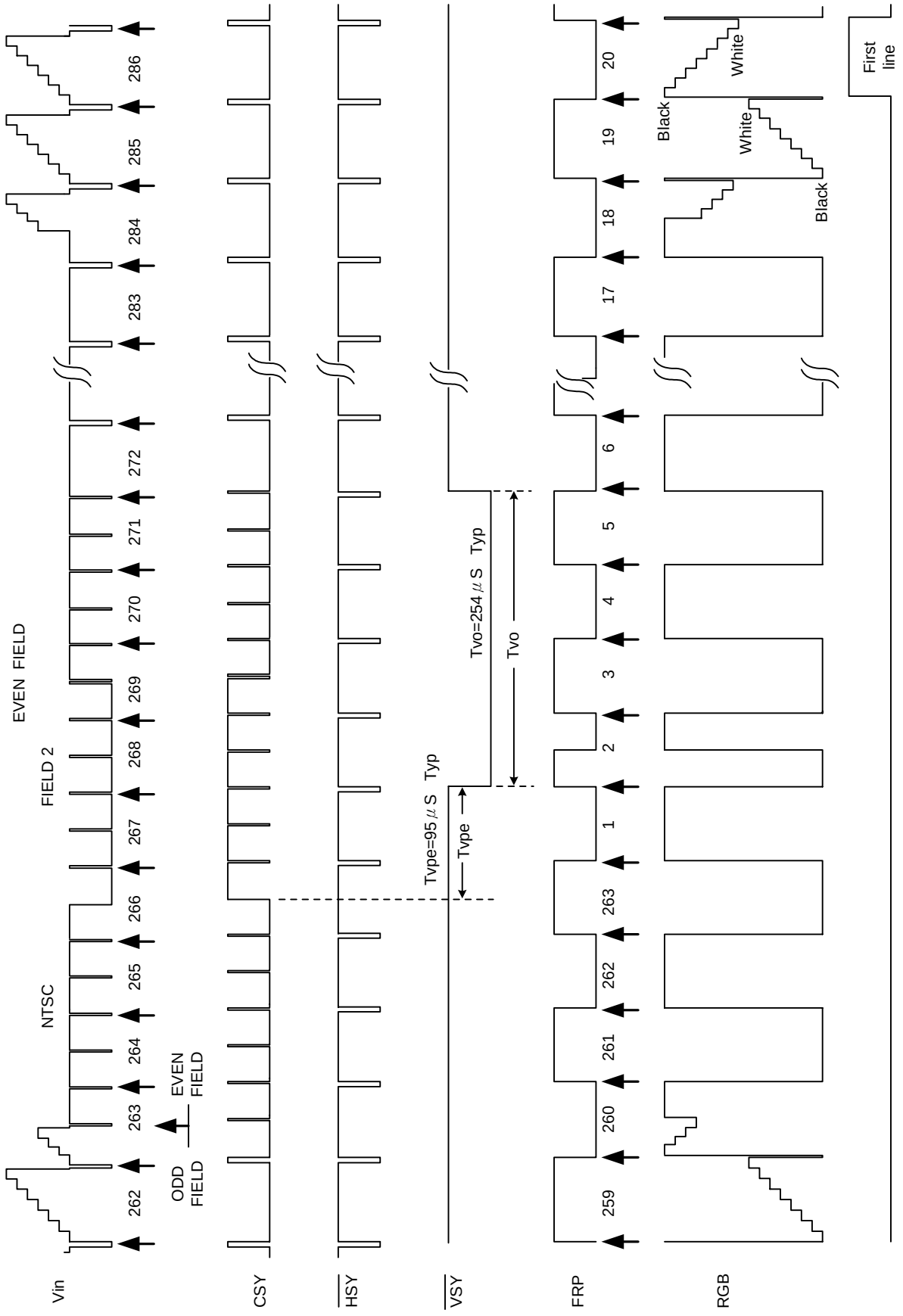
26 ~ 298 H

c) odd field : Scan lines 14n+17 14n+23 (n = 1, 2, 3..) are not displayed.
even field : Scan lines 14n+12 14n+20 (n = 1, 2, 3..) are not displayed.

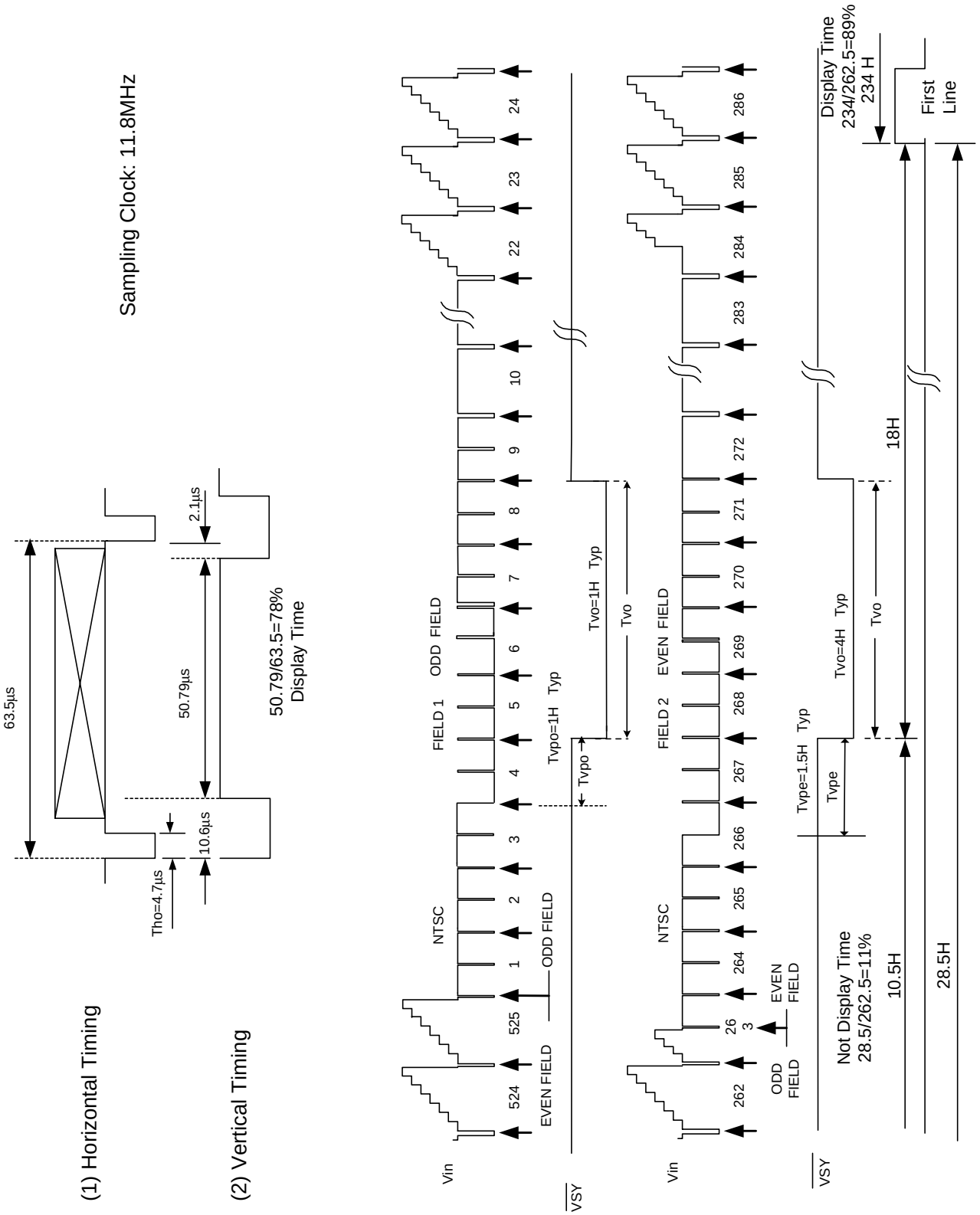




Timing chart of I/O and RGB signal



Timing chart of I/O and RGB signal



8. Optical Characteristics

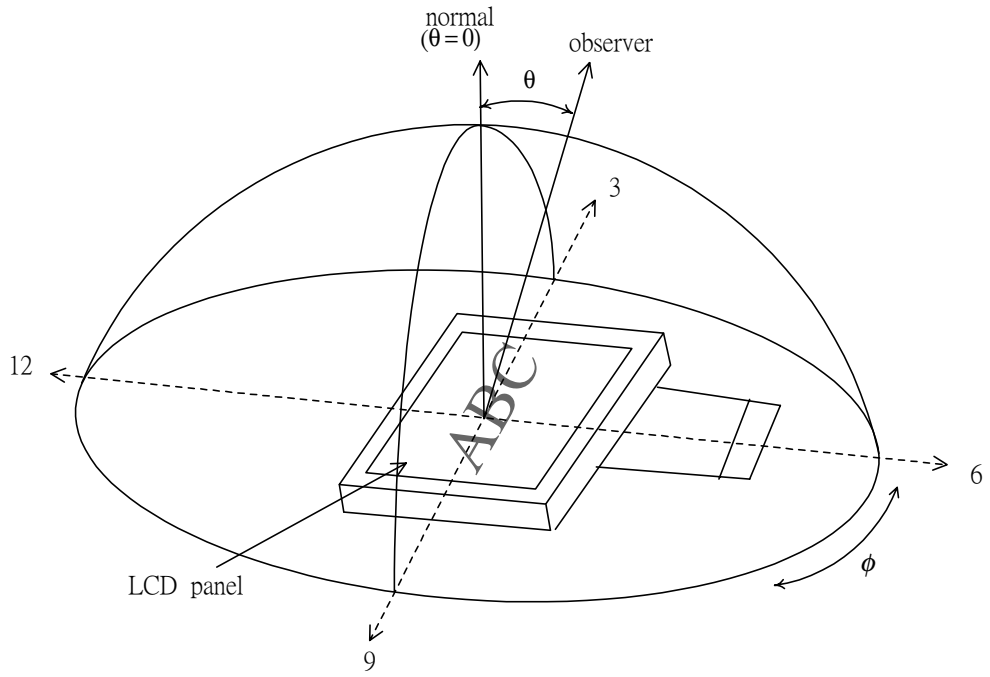
Ta = 25℃

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	θ	CR＞10	±45	±55		deg	Note 8-2
	Vertical	θ (to 12 o'clock)		10	15		deg	
		θ (to 6 o'clock)		30	35		deg	
Contrast Ratio		CR		80	120			Note 8-1
Response time	Rise	Tr	θ =0°		25		ms	Note 8-3
	Fall	Tf	θ =0°		60		ms	
Reflectance	Ratio	R			3.0		%	
Color coordinate	W				(.304, .333)			

Note 8-1：CR ＝ $\frac{\text{Luminance when testing point is White}}{\text{Luminance when testing point is Black}}$

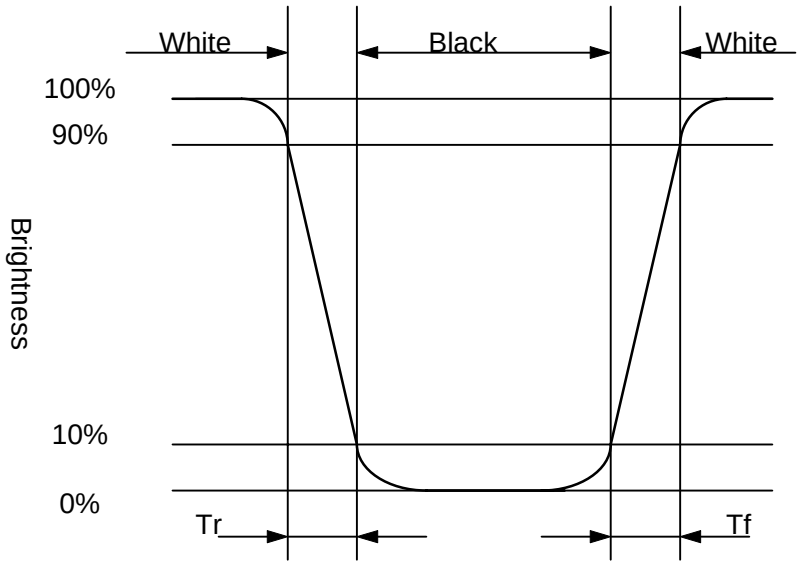
Contrast Ratio is measured in optimum common electrode voltage.
Test configurations see section 8-2.

Note 8-2 : The definitions of viewing angles are as follows.

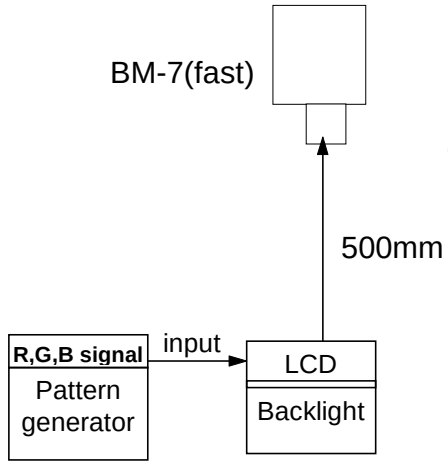


ϕ : Viewing direction
θ : Viewing angle

Note 8-3: The definitions of response time:

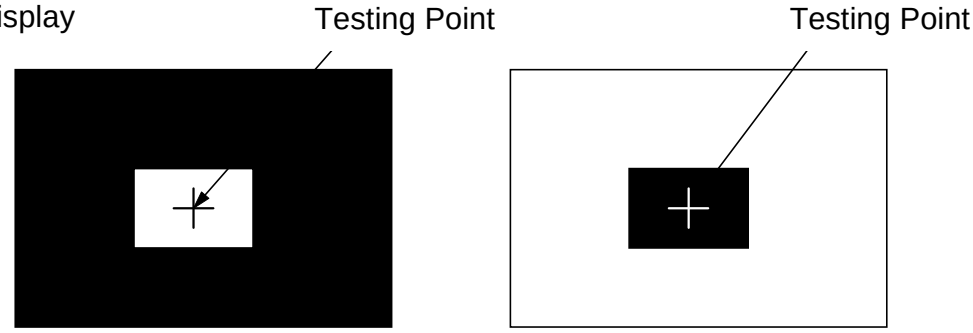


8-2) Test Configuration



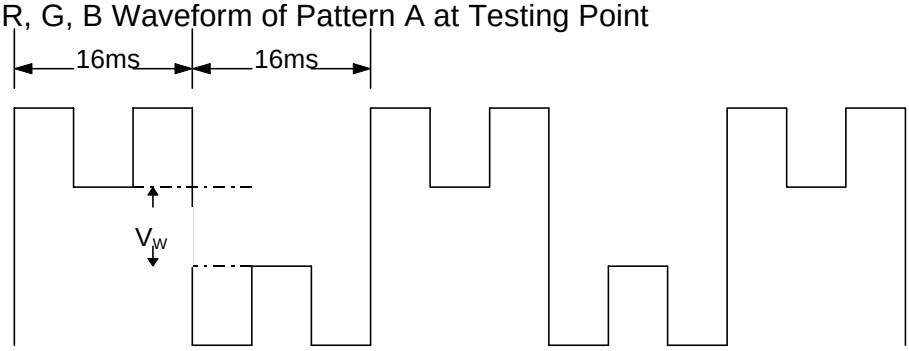
Caution: 1. Environmental illumination ≦ 1 lux
2. Before test CR, Vcom voltage must be adjusted carefully to get the best CR.

- LCD Display



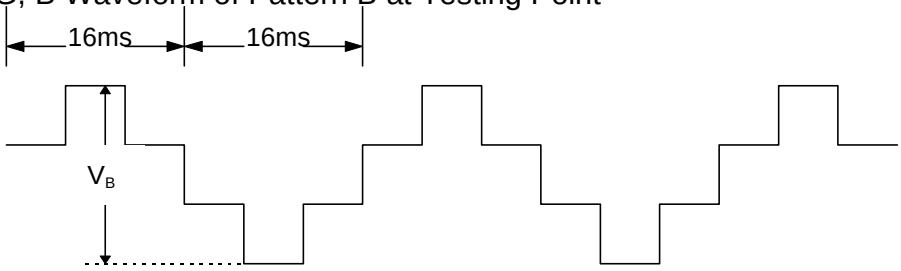
Pattern A　　Pattern B

- R, G, B Waveform of Pattern A at Testing Point



V_W=2.2V ± 0.2V

- G, B Waveform of Pattern B at Testing Point



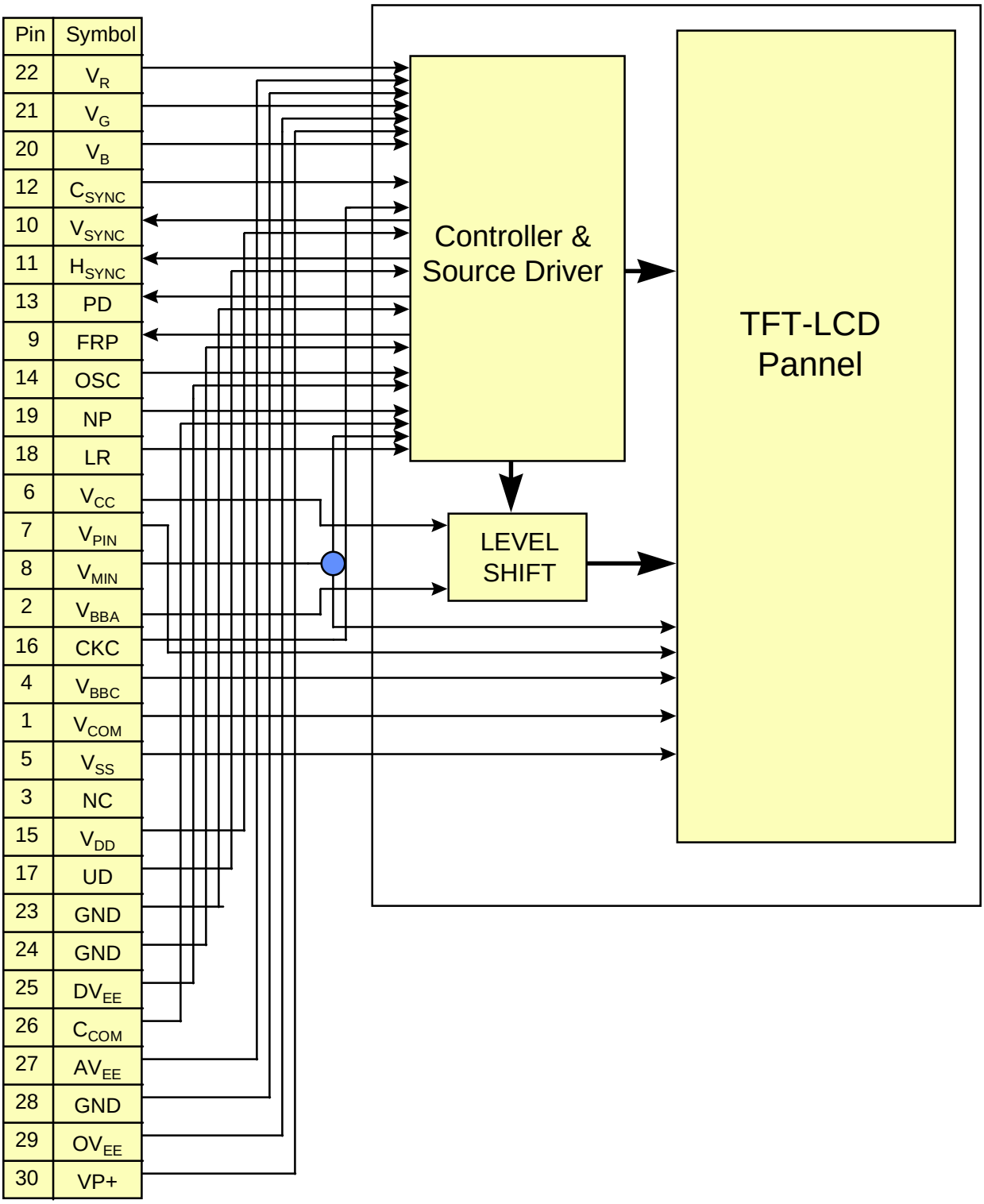
V_B=9.2V ± 0.2V

9. Reliability

No	Test Item	Test Condition
1	High Temperature Storage Test	Ta = +80 ℃, 240 hrs
2	Low Temperature Storage Test	Ta = -20℃, 240 hrs
3	High Temperature Operation Test	Ta= +60 ℃, 240 hrs
4	Low Temperature Operation Test	Ta = -10 ℃, 240 hrs
5	High Temperature & High Humidity Operation Test	Ta = +60℃, 95%RH, 240 hrs
6	Thermal Cycling Test(non-operating)	-25℃ →+25℃→ +70℃, 200 Cycles 30 min 5min 30 min
7	Electrostatic Discharge Test	150pF, 330Ω 10 times/point, 4 points/panel face

Ta: ambient temperature

10. Block diagram:



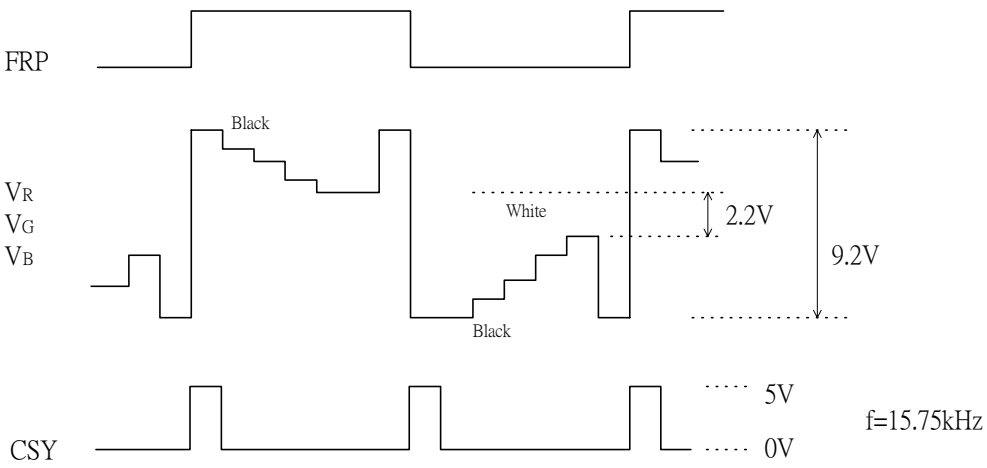
Appendix A: Interface Circuit

Description of the signal 16 pin connector on interface circuit

1.16 pin description:

Pin No	Symbol	I/O	Description	Remark
1	$\overline{HSY}$	I/O	Horizontal Sync. Input / Output	
2	FRP	O	Video Polarity Alternating Signal	Note 1
3	CSY	I	Composite Sync. Signal	
4	V_{GH}	I	Supply Voltage for Gate Driver (Hi level)	
5	V_{GL}	I	Supply Voltage for Gate Driver (Low level)	
6	V_B	I	Video Signal (Blue)	Note 1
7	V_R	I	Video Signal (Red)	Note 1
8	V_G	I	Video Signal (Green)	Note 1
9	GND	I	Ground	
10	V_{DD}	I	Supply voltage for controller	
11	V_{SH}	I	Supply voltage for source driver	
12	GND	I	Ground	
13	V_{DD}	I	Supply voltage for controller	
14	$\overline{VSY}$	I/O	Vertical Sync. Input/ Output	
15	PSI	O	Synchronize Pulse for Backlight Inverter	
16	GND	O	Ground	

Note 1:



2. Recommended operation condition:

GND = 0V， Ta = 25 ℃

Parameter		Symbol	MIN.	TYP	MAX.	Unit	Remark
Supply voltage for source driver		V_{SH}	+13.5	+14	+14.5	V	
Supply voltage for gate driver	H Level	V_{GH}	+19	+20	+24	V	
	L Level	V_{GL}	-5.5	-5	-4	V	
Supply voltage for controller		V_{DD}	+4.7	+5	+5.3	V	
Digital input voltage	H Level		+2.4	-	+5	V	Note 1
	L Level		-0.3	-	+0.8	V	
voltage	H Level		0	-	+0.55	V	Note 2
	L Level		+2.4	+4	+5		

Note 1 : $\overline{\text{HSY}}$, CSY, $\overline{\text{VSY}}$,

Note 2 : $\overline{\text{HSY}}$, FRP, $\overline{\text{VSY}}$, PSI,

Revision History

Rev.	Issued Date	Revised Contents
1	Feb. 22, 1999	NEW