P3T1085UK

I3C, I^{2}C-bus, 0.5 °C accuracy, digital temperature sensor

Rev. 1.2 — 10 September 2024 Product data sheet

1 General description

P3T1085UK is a temperature-to-digital converter with a -40 °C to +125 °C range. It uses an on-chip band gap temperature sensor and A-to-D conversion technique with overtemperature detection. The device contains a number of data registers, including a Configuration register (Conf) to store the device settings (such as device operation mode), and a temperature register (Temp) to store the digital temp reading, which can be communicated by a controller via the 2-wire serial I3C (up to 12.5 MHz) and I^{2}C (up to 3.4 MHz) interface.

The I^{2}C interface supports up to four target addresses and an alert function which becomes active when the temperature exceeds the programmed limits.

The I3C interface supports IBI (In Band Interrupt) where P3T1085UK emits its address into the arbitrated address header on the I3C bus to notify the controller of an interrupt. It does not require an additional interrupt pin. P3T1085UK can be configured for different operation conditions. It can be set in normal mode to periodically monitor the ambient temperature, or in shut-down mode to minimize power consumption. The temperature register always stores a 12 bit two's complement data, giving a temperature resolution of 0.0625 °C.

2 Features and benefits

- I3C (up to 12.5 MHz) and I^2C (up to 3.4 MHz) interface
- Supply range: 1.4 V to 3.6 V
- Programmable undertemperature and overtemperature alerts
- Resolution: 12 bits (0.0625 °C)
- Accuracy:
  - 1.4 V < V_{CC} < 3.6 V
    - ±0.5 °C (maximum) from –20 °C to +85 °C
    - ±1 °C (maximum) from -40 °C to +125 °C
- Low quiescent current: 6 µA supply current
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Package:
  - WLCSP6, 1.18 mm × 0.84 mm package

3 Applications

- Portable devices
- System thermal management
- SSD
- Industrial controllers
- Servers
- PC/Notebook

4 Ordering information

Table 1. Ordering information

Type Number	Topside mark	Package		
		Name	Description	Version
P3T1085UK	5	WLCSP6	wafer level chip-size package; 6 bumps; 1.18 mm x 0.84 mm x 0.48 mm (backside coating included)	SOT1380-6

4.1 Ordering options

Table 2. Ordering options

Type Number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
P3T1085UK	P3T1085UKAZ	WLCSP6	Reel 7” Q1/T1 *special mark chips dry pack	3500	T_{amb} = -40 °C to +125 °C
	P3T1085UKZ	WLCSP6	Reel 13” Q1/T1 *special mark chips dry pack	15000	T_{amb} = -40 °C to +125 °C

5 Block diagram

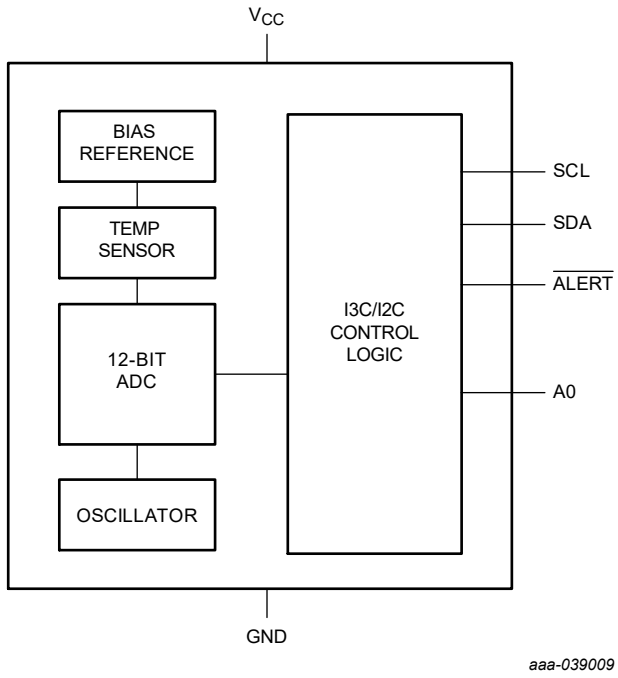
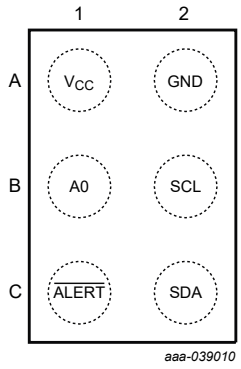


Figure 1. Block diagram of P3T1085UK

6 Pinning information

6.1 Pinning



Transparent top view

Figure 2. Pin configuration for P3T1085UK

6.2 Pin description

Table 3. Pin description for WLCSP6

Symbol	Pin	Description
SDA	C2	Digital I/O. I3C/I²C-bus serial bidirectional data line
SCL	B2	Digital input. I3C/I²C -bus serial clock
A0	B1	Address pin. Connect to SDA, SCL, V_{CC} or GND
GND	A2	Ground. To be connected to the system ground
V_{CC}	A1	Power supply
$\overline{ALERT}$	C1	Alert open-drain output

7 Functional description

7.1 General operation

P3T1085UK uses the on-chip band gap sensor to measure the device temperature with the resolution of 0.0625 °C and stores the 12-bit two's complement digital data, resulting from 12-bit A-to-D conversion, into the device Temp register. This Temp register can be read at any time by a controller on the I3C/I²C -bus. Reading temperature data does not affect the conversion in progress during the read operation. The temperature range is from -40 °C to 125 °C.

P3T1085UK can be set to operate in three modes: one-shot, continuous conversion, or shutdown mode through mode bits M1 and M0, allowing the user flexibility for different mode operations.

7.2 I²C-bus serial interface

The device can be connected to a compatible 2-wire serial interface Fast-mode and High-speed mode I²C-bus as a target device under the control of a controller or controller device, using two device terminals: SCL and SDA. The controller must provide the SCL clock signal and write/read data to/from the device through the SDA terminal. Note that if the I²C-bus common pull-up resistors have not been installed as required for I²C-bus, an external pull-up resistor, about 5 kΩ, is needed for each of these two terminals. The bus communication protocols are described in Section 7.7.

7.3 Target and mode description

7.3.1 Target address

To communicate with the device, the controller must first address target devices via a target address byte. The target address byte consists of seven address bits, and a direction bit indicating the intent of executing a read or write operation. The device features one address pin to allow up to four devices to be addressed on a single bus interface (see Table 4). The P3T1085UK requires 20 ms (max) after V_{CC} ≥ VPOR (1.2 V(max)) to recognize I²C/I3C command. After that, pin A0 state is sampled with the first legit START condition. Once it is finished, the address is latched to minimize power dissipation associated with detection.

Table 4. P3T1085UK address table

No.	Address pin coding	Target address
	A0	
1	GND	1001 000
2	V_{CC}	1001 001
3	SDA	1001 010
4	SCL	1001 011

7.3.2 Alert function: I²C only

The alert function is for I²C-bus interface only. In interrupt mode (TM = 1), the ALERT pin can be connected as an SMBus alert signal. When a controller detects an alert condition on the ALERT line, the controller sends an SMBus alert command (00011001) to the bus.

The device acknowledges the SMBus alert command and responds by sending its target address if the ALERT pin is active. The 8th bit (LSB) of the target address byte indicates whether the alert condition is caused by the temperature above T_{HIGH} or below T_{LOW}. The LSB bit is 1 if the temperature is higher than T_{HIGH}. The LSB bit is 0 if the temperature is lower than T_{LOW}. See Figure 15 and Figure 16 for details of this sequence.

If multiple devices respond to alert command, arbitration during the target address portion of alert command determines which device wins the arbitration to clear alert status first. The ALERT pin stays active if P3T1085UK loses the arbitration.

7.3.3 General call

The general call address is (0000000) if the eighth bit is 0. The device acknowledges the general call and responds to commands in the second byte. The device latches the status of the address pin if the second byte is 00000100. If the second byte is 00000110, the device internal registers are reset to power-up values.

7.3.4 High-Speed (Hs) Mode

The controller device must send an SMBus Hs-mode controller code (00001xxx) as the first byte after a start condition to enable the bus to high-speed operation. After receiving the Hs-mode code, P3T1085UK allows SMBus speed up to 3.4 MHz.

7.3.5 Timeout function

If the SDA or SCL line is held LOW for longer than t_{to} (15 ms minimum; guaranteed at 45 ms maximum), the device resets to the idle state (SDA released) and waits for a new START condition. This ensures that the device never hangs up the bus if there are conflicts in the transmission sequence.

7.4 I3C-bus serial interface

P3T1085UK interface includes a MIPI I3C (up to 12.5 MHz) SDR only target interface. The I3C controller controller can assign a dynamic address to P3T1085UK by issuing a Set Dynamic Address from Static Address (SETDASA) CCC command.

7.4.1 Dynamic address assigning flow

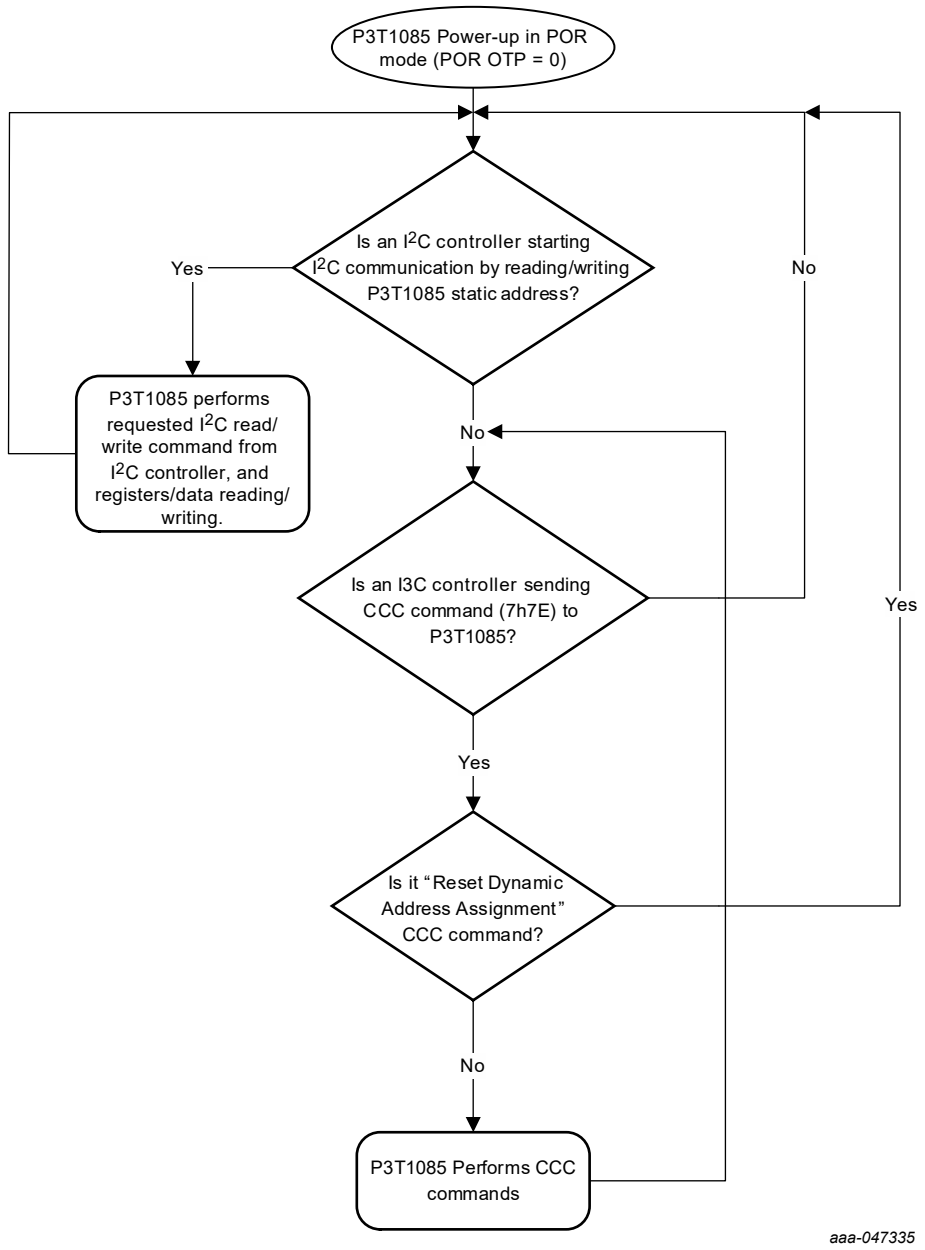


Figure 3. Dynamic address assignment flowchart

7.4.2 I3C provisional-ID

The I3C provisional-ID field is a 6-byte read-only (48 bits) word giving the following information:

- 15 bits with the manufacturer name, unique per manufacturer (for example, NXP).
- 1 bit indicating whether the device has a random ID or a structured provisional-ID.
- 16 bits with the device identification, assigned by manufacturer.
- 4 bits providing the device instantiation information, e.g. the address pin binary input.
- 12 bits with the device revision, assigned by manufacturer.

The exact Mipi-I3C provisional-ID composition is shown in Table 5 with detailed data content.

Table 5. I3C provisional-ID composition

Manufacturer ID	Non-Random part number	Device ID	Instance ID	Version
BITS[47:33]	BITS[32]	BITS[31:16]	BITS[15:12]	BITS[11:0]
15'h011B 0000 0010 0011 011	0	0001 0101 0010 1001	0000	Refer to Table 6

Table 6. I3C Provisional-ID BITS[11:0] vs I2C Address

I2C target address BITS[7:1]	I3C PID BITS[11:0]
1001 000	0000 1001 0000
1001 001	0000 1001 0010
1001 010	0000 1001 0100
1001 011	0000 1001 0110

7.4.3 BCR and DCR

The I3C devices shall have a read-only Bus Characterization Register (BCR) and a Device Characterization Register (DCR). These can be read using the GETCBCR and GETDCR CCC.

The BCR contains information describing the device's role and capabilities related to the I3C bus. The content of P3T1085UK is listed in Table 7.

Table 7. Bus Characterization Register (BCR)

Bit	Function	Description
BCR[7]	Device role	2'b00: I3C target
BCR[6]		
BCR[5]	Advanced Capabilities	0: Does not support optional advanced capabilities
BCR[4]	Virtual Target Support	0: Is not a Virtual Target and does not expose other downstream Device(s)
BCR[3]	Offline capable	0: device will always react to I3C bus commands
BCR[2]	IBI Payload	0: No data bytes follow the accepted IBI
BCR[1]	IBI Request capable	1: capable
BCR[0]	Maximum data speed limitation	1: Limitation

The DCR describes the device type for the bus controller to assess and assign the dynamic address and use common command codes as listed in Table 8

Table 8. Device Characterization Register (DCR)

Bit [7:0]	Description
0110 0011	Temperature sensor

7.4.4 I3C Common Command Codes (CCC)

MIPI I3C devices listen to and support a number of the Common Command Codes (CCC) to control certain features and behaviors, such as resetting the device, enabling/disabling in-band interrupts or renewing the device dynamic address.

P3T1085UK supports CCCs that allow the controller to control multiple targets through a broadcast command at once or individual targets through direct commands listed in Table 9

Table 9. Bus Characterization Register (BCR)

Common Command Code	CCC type	Command Name	Default setting	Description
0x00	Broadcast	ENEC[1] Enable Events Command	Enabled	Enable Target event driven interrupts
0x06	Broadcast	RSTDAA[1] Reset Dynamic Address Assignment	-	Forget current Dynamic Address and wait for new assignment
0x07	Broadcast	ENTDAA[1] Enter Dynamic Address Assignment	-	Entering Controller initiation of Target Dynamic Address Assignment. Don't participate if the Target already has an Address assigned.
0x80	Direct	ENEC[1] Enable Events Command	enabled	Enable Target event driven interrupts
0x81	Direct	DISEC[1] Disable Events Command	disabled	Disable Target event driven interrupts
0x87	Direct Set	SETDASA[1] Set Dynamic Address from Static Address	-	Controller assigns a Dynamic Address to a target with a known Static Address
0x88	Direct Set	SETNEWDA[1] Set New Dynamic Address	-	Controller assigns a new Dynamic Address to any I3C Target
0x8D	Direct Get	GETPID[1] Get Provisional ID	-	Get the Target's Provisional-ID
0x8E	Direct Get	GETBCR Get Bus Characteristics Register	-	Get a Device's Bus Characteristic Register (BCR)
0x8F	Direct Get	GETDCR Get Device Characteristics Register	-	Get a Device's Device Characteristic Register (DCR)
0x90	Direct Get	GETSTATUS Get Device Status	-	Get Device's operating status
0x9A	Direct	RSTACT Target Reset Action	-	Configure and query Target Reset action and timing

7.4.5 Examples of CCC protocol

7.4.5.1 ENEC/DISEC (Enable/Disable Target Events Command)

The ENEC/DISEC CCC allows the Controller to control when Target-initiated traffic is enabled or disabled on the I3C Bus. This control governs a Target's attempts to request an IBI (ENINT/DISINT), or to request Controllership (ENMR/DISMR).

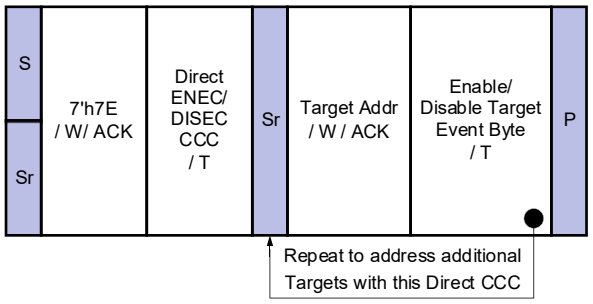


Figure 4. ENEC/DISEC Format 1: Direct

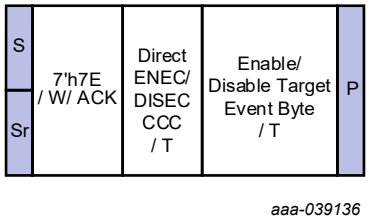


Figure 5. ENEC/DISEC Format 2: Broadcast

Table 10. Enable Target Events Command Byte Format

Bit	7	6	5	4	3	2	1	0
Symbol	reserved				ENHJ	reserved	ENMR	ENINT

Table 11. Disable Target Events Command Byte Format

Bit	7	6	5	4	3	2	1	0
Symbol	reserved				DISHJ	reserved	DISMR	DISINT

7.4.5.2 RSTDAA (Reset Dynamic Address Assignment)

The RSTDAA Broadcast CCC (Figure 6) indicates to all I3C Devices that the Controller requires them to clear/ reset their Controller-assigned Dynamic Address.

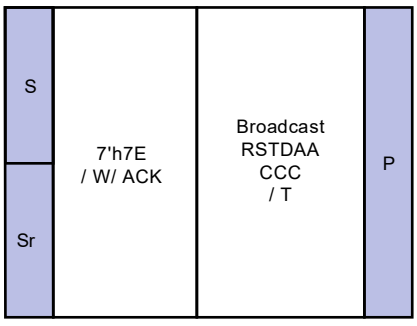


Figure 6. RSTDAA format

7.4.5.3 ENTDAA (Enter Dynamic Address Assignment)

The ENTDAA Broadcast CCC (Figure 7) indicates to all I3C Devices that the Controller requires them to enter the Dynamic Address Assignment procedure. Target Devices that already have a Dynamic Address assigned shall not respond to this command.

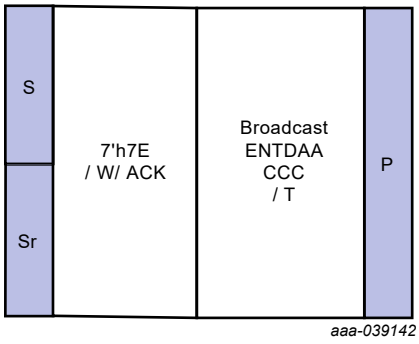


Figure 7. ENTDAA format

7.4.5.4 SETDASA (Set Dynamic Address from Static Address)

The SETDASA Direct CCC (Figure 8) allows the Controller to assign a Dynamic Address to one Target using the Target's Static Address. The SETDASA CCC should be used before the ENTDAA CCC is used.

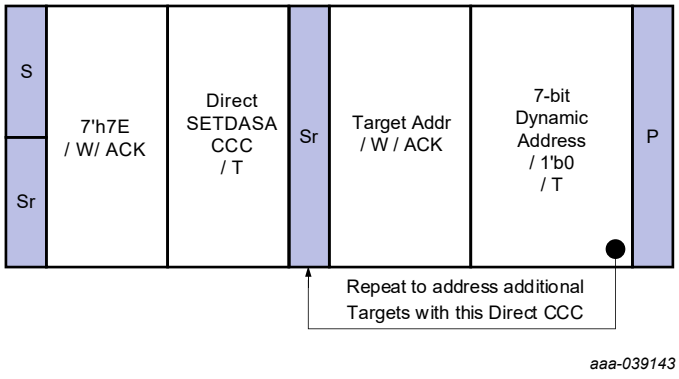


Figure 8. SETDASA format

7.4.5.5 SETNEWDA (Set New Dynamic Address)

The SETNEWDA Direct CCC (Figure 9) allows the I3C Controller to assign a new Dynamic Address to one I3C Target Device. In the Dynamic Address field, the 7 most significant bits (Bits[7:1]) contain the 7-bit Dynamic Address, and the least significant bit (Bit[0]) is filled with the value 1'b0.

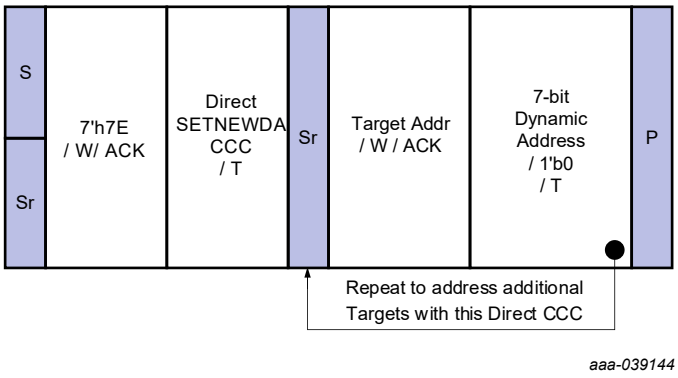


Figure 9. SETNEWDA format

7.4.5.6 GETPID (Get Provisioned ID)

The GETPID Direct CCC (Section 7.4.5.6) is a Get request for one I3C Target Device to return its 48-bit Provisioned ID to the Controller. Following transmission of the GETPID CCC, the 48-bit value is transmitted as 6 bytes, with MSB first.

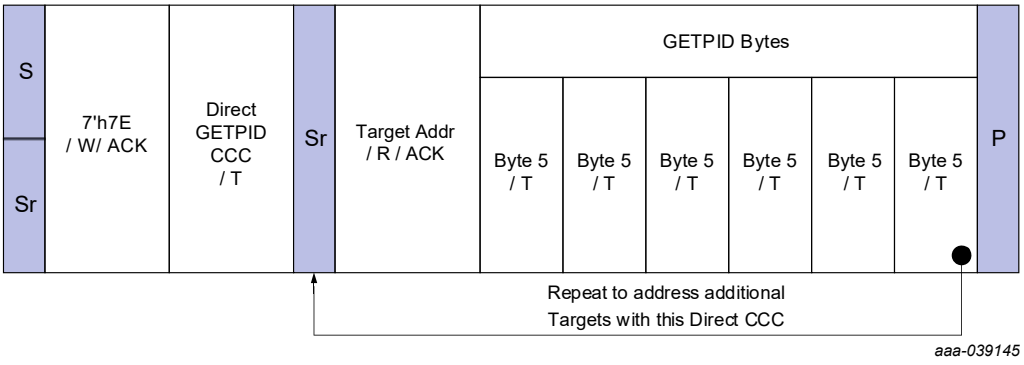


Figure 10. GETPID format

7.4.5.7 GETBCR (Get Bus Characteristics Register)

The GETBCR Direct CCC (Section 7.4.5.7) is a Get request for one I3C Target Device to return its Bus Characteristics Register (BCR) to the Controller, the BCR value is transmitted in one byte, with the MSb transmitted first.

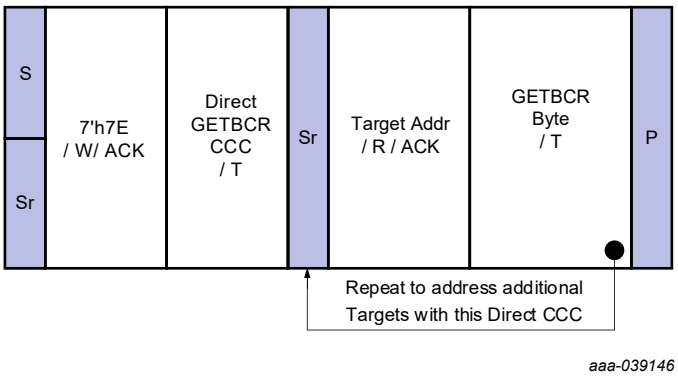


Figure 11. GETBCR format

7.4.5.8 GETDCR (Get Device Characteristics Register)

The GETDCR Direct CCC (Section 7.4.5.8) is a Get request for one I3C Target Device to return its Device Characteristics Register (DCR) to the Controller. The DCR value is transmitted in one byte, with the MSB transmitted first.

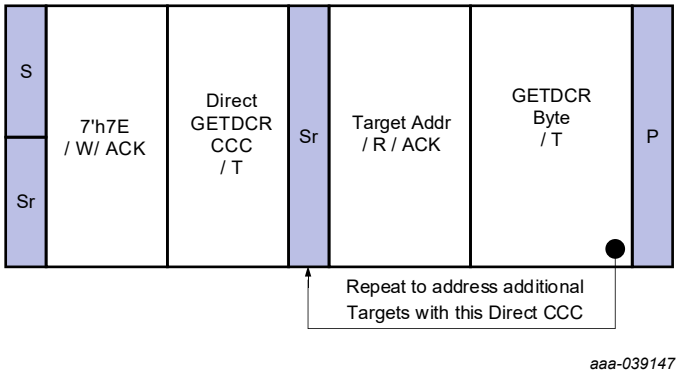


Figure 12. GETDCR format

7.4.5.9 GETSTATUS (Get Device Status)

The GETSTATUS Direct CCC (Figure 13) is a Get request for one I3C Target Device to return its current Status. It returns the two-byte format detailed in Table 12.

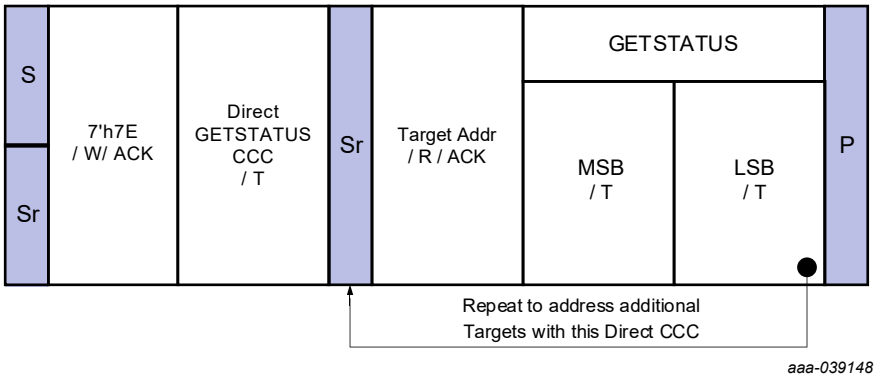


Figure 13. GETSTATUS format

Table 12. GETSTATUS MSB-LSB Format

Vendor Reserved	Activity Mode	Protocol Error	Reserved	Pending Interrupt
BITS[15:8]	BITS[7:6]	BITS[5]	BITS[4]	BITS[3:0]
0	0	0	0	0

7.4.6 In-Band-Interrupt (IBI)

MIPI I3C supports interrupts from target devices to controllers through the SCL/SDA 2-wire interface. The targets wait for a quiet period in which both SCL and SDA are idle and SDA is held high by a weak pull-up resistor.

At least one target can pull SDA low, so the controller is notified and starts SCL and enables the regular SDA pull-up resistor to enter address arbitration. The falling edge of SDA followed by a falling edge of SCL is then interpreted by all targets as a start condition.

The target(s) pulling SDA low through an open-drain driver release SDA on the falling SCL edge so it's pulled up to high through the pull-up resistor.

During the following 7 SCL pulses all eligible targets can transmit their dynamic address to the controller. The lowest dynamic address is recognized as the one with the highest priority. Once a target determines that another target is driving a lower address through its open drain output on SDA, it shall refrain from interfering with any further communication on SDA while the current communication continues.

The 7 address bits are followed by RnW = 1 and an ACK driven by the controller (if the controller acknowledges).

7.5 Register list

The P3T1085UK contains four data registers beside the pointer register as listed in Table 13. The pointer value, read/write capability and default content at power-up of the registers are also shown in Table 14 and Table 15.

Table 13. Register table

Register name	Pointer value	R/W	POR state	Description
Temp	00h	read only	0000h	Temperature register: contains two 8-bit data bytes; to store the measured Temp data.
Conf	01h	R/W	2210h	Configuration register: contains a single 16-bit data byte; to set the device operating condition.
T_{LOW}	02h	R/W	B500h	T_{LOW} register (read/write)
T_{HIGH}	03h	R/W	7FF0h	T_{HIGH} register (read/write)

7.5.1 Pointer register

The Pointer register contains an 8-bit data byte, of which the two LSB bits represent the pointer value of the other five registers, and the other five MSB bits are equal to 0, as shown in Table 14 and Table 15. The Pointer register is not accessible to the user, but is used to select the data register for write/read operation by including the pointer data byte in the bus command.

Table 14. Pointer register

B7	B6	B5	B4	B3	B2	B[1:0]
0	0	0	0	0	0	pointer value

Table 15. Pointer value

B1	B0	Selected register
0	0	Temperature register (Temp, read only)
0	1	Configuration register (read/write)
1	0	T_{LOW} register (read/write)
1	1	T_{HIGH} register (read/write)

Because the Pointer value is latched into the Pointer register when the bus command (which includes the pointer byte) is executed, a read from the device may or may not include the pointer byte in the statement. To read a register again that has been recently read and the pointer has been preset, the pointer byte does not have to be included. To read a register that is different from the one that has been recently read, the pointer byte

must be included. However, a write to the device must always include the pointer byte in the statement. The bus communication protocols are described in Section 7.7.

At power-up, the Pointer value is equal to 000b and the Temp register is selected; users can then read the Temp data without specifying the pointer byte.

Anything not shown in Table 15 is reserved and should not be used.

7.5.2 Configuration register

The Configuration register (Conf) is a write/read register and contains an 16-bit non-complement data byte that is used to configure the device for different operation conditions. Table 16 shows the bit assignments of this register.

Table 16. Conf register

Byte	D7	D6	D5	D4	D3	D2	D1	D0
1	ID	CR1	CR0	FH	FL	TM	M1	M0
	0	0	1	0	0	0	1	0
2	POL	0	HYS1	HYS0	0	0	0	0
	0	0	0	1	0	0	0	0

7.5.2.1 Hysteresis Control (HYS1 and HYS0)

HYS1 and HYS0 are the hysteresis control bits to set hysteresis for the limit comparison of P3T1085UK to 0 °C, 1 °C, 2 °C, or 4 °C. The default hysteresis value is 1 °C. shows the settings of HYS1 and HYS0.

Table 17. Hysteresis settings

HYS1	HYS0	HYSTERESIS
0	0	0 °C
0	1	1 °C (default)
1	0	2 °C
1	1	4 °C

7.5.2.2 Thermostat Mode (TM)

The thermostat mode (TM) bit shows the device whether P3T1085UK operates in interrupt mode (TM = 1) or comparator mode (TM = 0, default). For details, see Section 7.5.4.

7.5.2.3 Polarity (POL)

If POL = 0 , the ALERT is active low. For POL = 1, the ALERT pin is active high, and the state of the ALERT pin is inverted. The default value of POL = 0.

7.5.2.4 Temperature Watchdog Flags (FH and FL)

The temperature watchdog flags (FH and FL) in configuration register indicate the result of comparing the device temperature and temperature limit (T_{HIGH} and T_{LOW}) at the end of every conversion. The T_{HIGH} and T_{LOW} are stored in temperature limit registers.

- FH = 1 if device temperature is higher than T_{HIGH} register's value.
- FL = 1 if device temperature is lower than T_{LOW} register's value.

If the temperature is within the range set by T_{HIGH} and T_{LOW} in the temperature limit registers, both FH and FL will be 0. In interrupt mode, FL or FH is set by an under- or overtemperature event; the SMBus ALERT Response only clears the pin and not the flags. To clear both the flags and pin, it is required to read the configuration register

7.5.2.5 Conversion rate (CR1 and CR0)

CR1 and CR0 are the conversion rate bits to configure the conversion rates of 0.25 Hz, 1 Hz, 4 Hz, or 16 Hz.

The default rate is 1 Hz. The typical conversion time is 7.8 ms. Table 18 shows the settings for CR1 and CR0.

Table 18. Conversion rate settings

CR1	CR0	Conversion rate	I_Q (typ)
0	0	0.25 Hz	2 µA
0	1	1 Hz (default)	2.1 µA
1	0	4 Hz	2.5 µA
1	1	16 Hz	4 µA

P3T1085UK starts a conversion after power-up or a general-call rest as illustrated in Figure 14. The first result is available after 7.8 ms (typical). The typical active quiescent current during conversion at +25 °C is 15 µA at +25 °C. The typical quiescent current during delay at +25 °C is 1.95 µA.

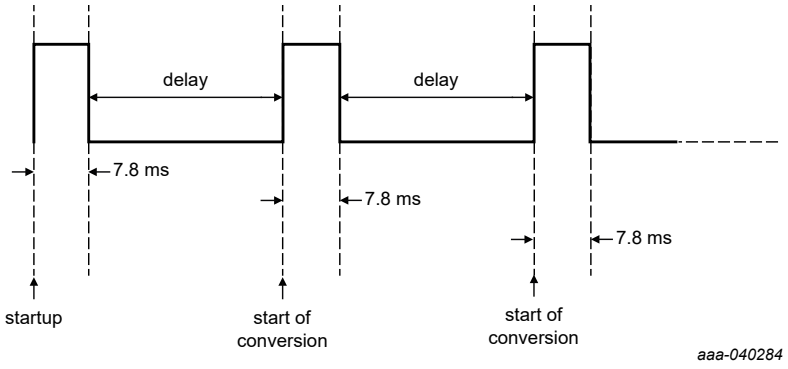


Figure 14. Conversion start

7.5.3 Temperature register

The Temperature register (Temp) holds the digital result of temperature measurement or monitor at the end of each analog-to-digital conversion. This register is read-only and contains two 8-bit data bytes consisting of one Most Significant Byte (MSByte) and one Least Significant Byte (LSByte). However, only 12 bits of those two bytes are used to store the Temp data in two's complement format with the resolution of 0.0625 °C. Table 19 and Table 20 show the bit arrangement of the Temp data in the data bytes.

Table 19. Temperature register - Byte 1

D7	D6	D5	D4	D3	D2	D1	D0
T11	T10	T9	T8	T7	T6	T5	T4

Table 20. Temperature register - Byte 2

D7	D6	D5	D4	D3	D2	D1	D0
T3	T2	T1	T0	0	0	0	0

When reading register Temp, all 16 bits of the two data bytes (MSByte and LSByte) are provided to the bus and all should be collected by the controller for a valid temperature reading. However, only the 11 most significant bits should be used, and the four least significant bits of the LS Byte are zero and should be ignored. One of the ways to calculate the Temp value in °C from the 12-bit Temp data is:

- To convert positive temperatures to a digital data format:
  Divide the temperature by the resolution. Then, convert the result to binary code with a 12-bit, left-justified format, and MSB = 0 to denote a positive sign.
  Example: (+75 °C)/(0.0625 °C/count) = 1200 = 4B0h = 0100 1011 0000.
- To convert negative temperatures to a digital data format:
  Divide the absolute value of the temperature by the resolution, and convert the result to binary code with a 12-bit, left-justified format. Then, generate the twos complement of the result by complementing the binary number and adding one. Denote a negative number with MSB = 1.
  Example: (|–25 °C|)/(0.0625 °C/count) = 400 = 190h = 0001 1001 0000. Twos complement format: 1110 0110 1111 + 1 = 1110 0111 0000

Examples of the Temp data and value are shown in Table 21.

Table 21. Temperature register value

Temperature (°C)	ADC value	
	Binary	Hex
127.9375	0111 1111 1111	7FF
127	0111 1111 0000	7F0
100	0110 0100 0000	640
80	0101 0000 0000	500
75	0100 1011 0000	4B0
50	0011 0010 0000	320
25	0001 1001 0000	190
0.25	0000 0000 0100	004
0	0000 0000 0000	000
-0.25	1111 1111 1100	FFC
-25	1110 0111 0000	E70
-40	1101 1000 0000	D80

7.5.4 High- and low-limit registers

In interrupt mode (TM = 1), the ALERT pin is active when the temperature is above the value in the T_{HIGH} register or below the value in the T_{LOW} register.

It can be cleared when a read operation of the configuration register occurs or the device responds to the SMBus alert response address successfully. The ALERT pin is also cleared by the general call reset command. The ALERT response to temperature in interrupt mode is illustrated in Figure 15.

In comparator mode (TM = 0), the ALERT pin is active when the temperature is above the value in the T_{HIGH} register or below the value in the T_{LOW} register.

It can be cleared when the temperature is within the range set by: (T_{LOW} + HYS) and (T_{HIGH} – HYS)

Where • HYS is the hysteresis set by the hysteresis control bits (HYS1 and HYS0). The ALERT response to temperature in comparator mode is illustrated in Figure 16.

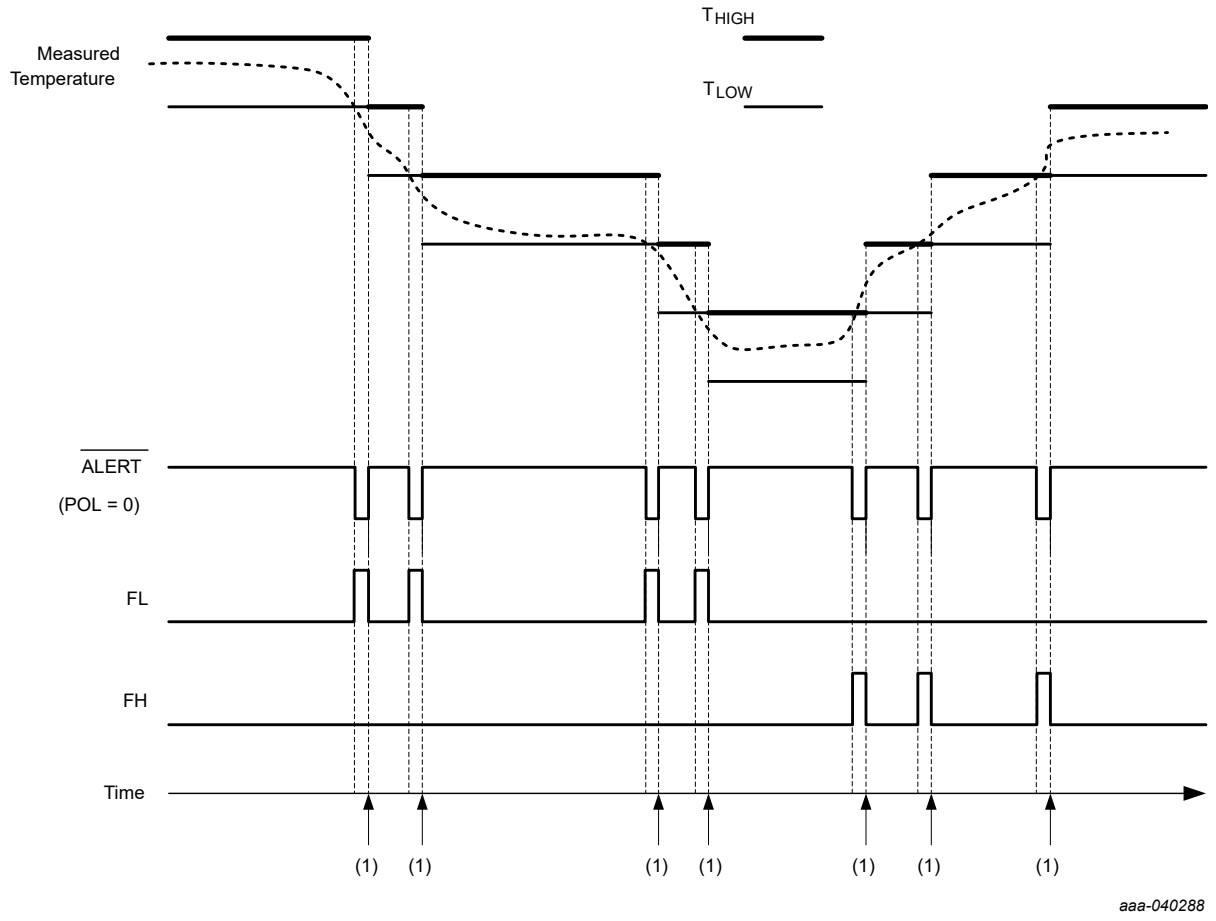
The format for the T_{HIGH} and T_{LOW} registers are described in Table 22 and Table 23. Power-up (reset) default values are set to maximum T_{HIGH} = +127.9375 °C (0x7FF8) and T_{LOW} = –75 °C (0xB500). These values ensure that the limit window is set to the maximum at power-up, and the ALERT pin will not become active until the required limit value is set in the register. The data format of T_{HIGH} and T_{LOW} is the same as that of the temperature register.

Table 22. Bytes 1 and 2 of T_{HIGH} register

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	H11	H10	H9	H8	H7	H6	H5	H4
BYTE	D7	D6	D5	D4	D3	D2	D1	D0
2	H3	H2	H1	H0	0	0	0	0

Table 23. Bytes 1 and 2 of T_{LOW} register

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	L11	L10	L9	L8	L7	L6	L5	L4
BYTE	D7	D6	D5	D4	D3	D2	D1	D0
2	L3	L2	L1	L0	0	0	0	0



(1) Update T_{HIGH} and T_{LOW} limit. Read the configuration register to clear the flags and the $\overline{ALERT}$ pin.

Figure 15. Interrupt mode

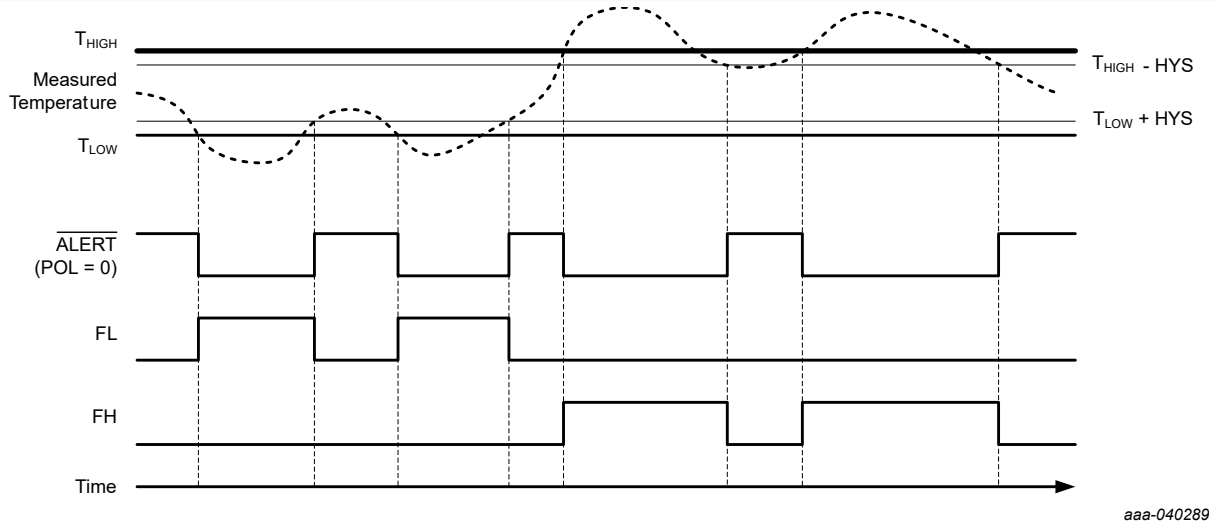


Figure 16. Comparator mode

7.6 Functional modes

There are three different modes: shutdown, one-shot, or continuous conversion set by mode bits, M0 and M1.

7.6.1 Shutdown mode (M1 = 0, M0 = 0)

In shutdown mode (M1 = 0, M0 = 0) all device circuitry is shut down other than the serial interface. It reduces current consumption to typically 0.2 µA. The device shuts down when current conversion is completed.

7.6.2 One-shot mode (M1 = 0, M0 = 1)

When P3T1085UK is in shutdown mode, writing a '01' to the M1 and M0 bits starts one-shot mode (i.e. a single temperature conversion). During the conversion, the M1 and M0 bits read 01. The device goes back to the shutdown state once the single conversion is completed. After the conversion, the M1 and M0 bits read 00. This feature can be used for reducing the power consumption when continuous temperature monitoring is not required.

Using one-shot mode, the device can have a higher conversion rate for fast temperature tracking or a lower conversion rate for power saving.

A complete one-shot period takes 20 ms (max), including active conversion and other process time. It means the temperature registers will be updated 20 ms (max) after a one-shot command is received. Reading the temperature registers can take place in less than 20 µs.

To perform the one-shot mode, the P3T1085UK must be in shutdown mode. If entering shutdown mode (i.e. writing a '00' to M1 & M0) from continuous conversion mode (M1=1), it requires a 12 ms (max) delay to acknowledge the first one-shot command.

7.6.3 Continuous conversion mode (M1 = 1)

In continuous conversion mode (M1 = 1), the conversion rate bits (CR1 and CR0 in the configuration register) determine the conversion rate. The device finishes a single conversion then goes to standby and waits for the delay set by CR1 and CR0 bit. See Table 18 for CR1 and CR0 settings.

7.7 Protocols for writing and reading the registers

The communication between the host and the device must strictly follow the rules as defined by the I²C-bus management. The protocols for device register read/write operations are illustrated in Figure 17 to Figure 22 together with the following definitions:

1. Before a communication, the I²C-bus must be free or not busy. It means that the SCL and SDA lines must both be released by all devices on the bus, and they become HIGH by the bus pull-up resistors.
2. The host must provide SCL clock pulses necessary for the communication. Data is transferred in a sequence of 9 SCL clock pulses for every 8-bit data byte followed by 1-bit status of the acknowledgment.
3. During data transfer, except the START and STOP signals, the SDA signal must be stable while the SCL signal is HIGH. It means that the SDA signal can be changed only during the LOW duration of the SCL line.
4. S: START signal, initiated by the host to start a communication, the SDA goes from HIGH to LOW while the SCL is HIGH.
5. RS: RE-START signal, same as the START signal, to start a read command that follows a write command.
6. P: STOP signal, generated by the host to stop a communication, the SDA goes from LOW to HIGH while the SCL is HIGH. The bus becomes free thereafter.
7. W: write bit, when the write/read bit = LOW in a write command.
8. R: read bit, when the write/read bit = HIGH in a read command.
9. A: device acknowledge bit, returned by the device. It is LOW if the device works properly and HIGH if not. The host must release the SDA line during this period in order to give the device the control on the SDA line.

10. A': controller acknowledge bit, not returned by the device, but set by the controller or host in reading 2-byte data. During this clock period, the host must set the SDA line to LOW in order to notify the device that the first byte has been read for the device to provide the second byte onto the bus.
11. NA: Not Acknowledge bit. During this clock period, both the device and host release the SDA line at the end of a data transfer, the host is then enabled to generate the STOP signal.
12. In a write protocol, data is sent from the host to the device and the host controls the SDA line, except during the clock period when the device sends the device acknowledgment signal to the bus.
13. In a read protocol, data is sent to the bus by the device and the host must release the SDA line during the time that the device is providing data onto the bus and controlling the SDA line, except during the clock period when the controller sends the controller acknowledgement signal to the bus.
14. For best temperature accuracy both temperature bytes should be read as shown in Figure 21 and Figure 22 but for a quick less accurate check/reduce bus transmission than only one byte, the MSByte, must be read as shown in Figure 19.

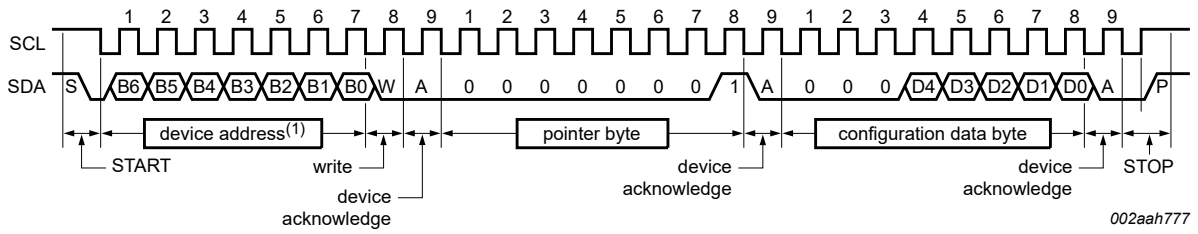


Figure 17. Write configuration register (1-byte data)

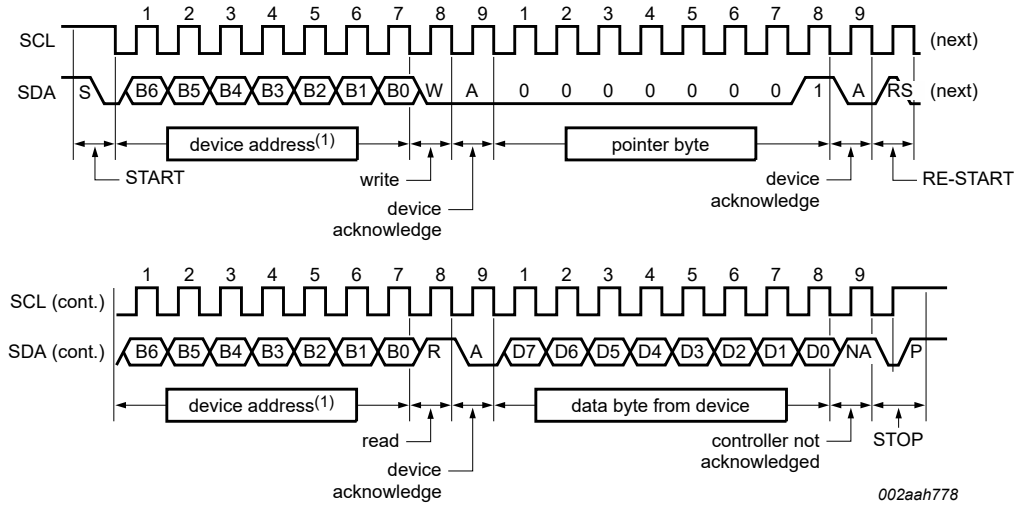


Figure 18. Read configuration register including pointer byte (1-byte data)

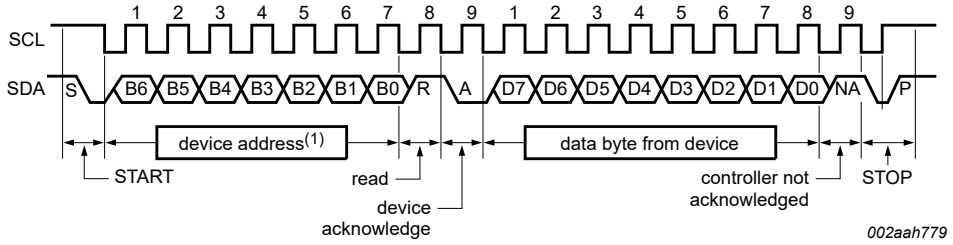


Figure 19. Read configuration or temp register with preset pointer (1-byte data)

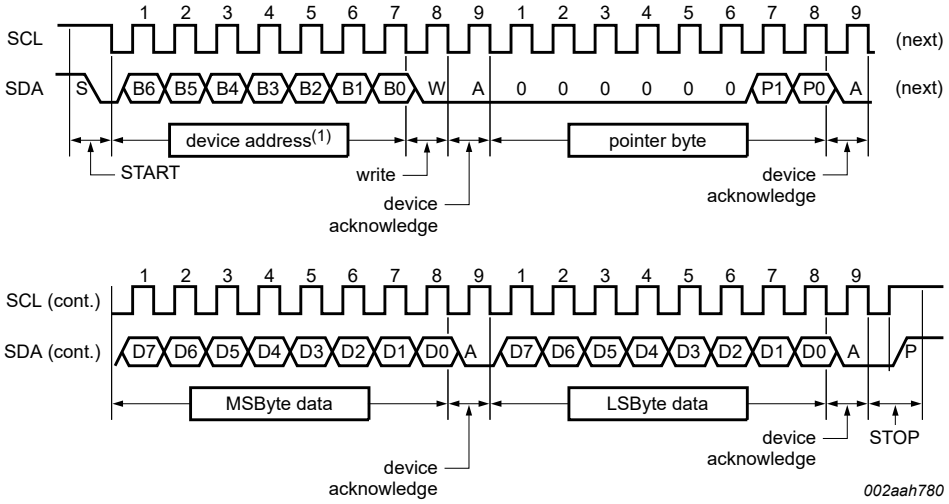


Figure 20. Write register (2-byte data)

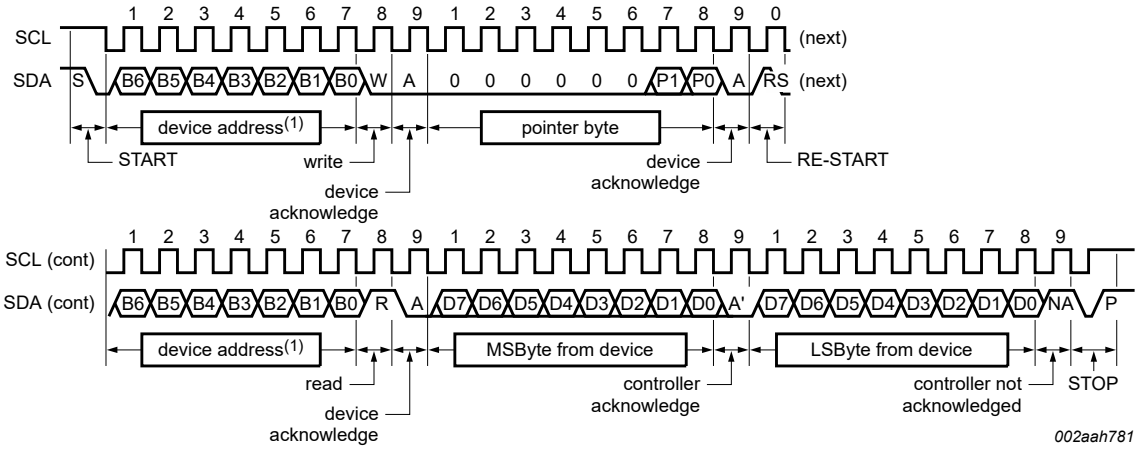


Figure 21. Read register including pointer byte (2-byte data)

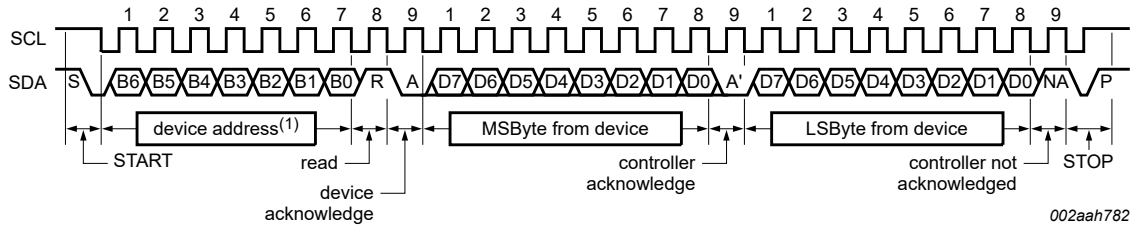


Figure 22. Read register with preset pointer (2-byte data)

8 Application design-in information

8.1 Typical application

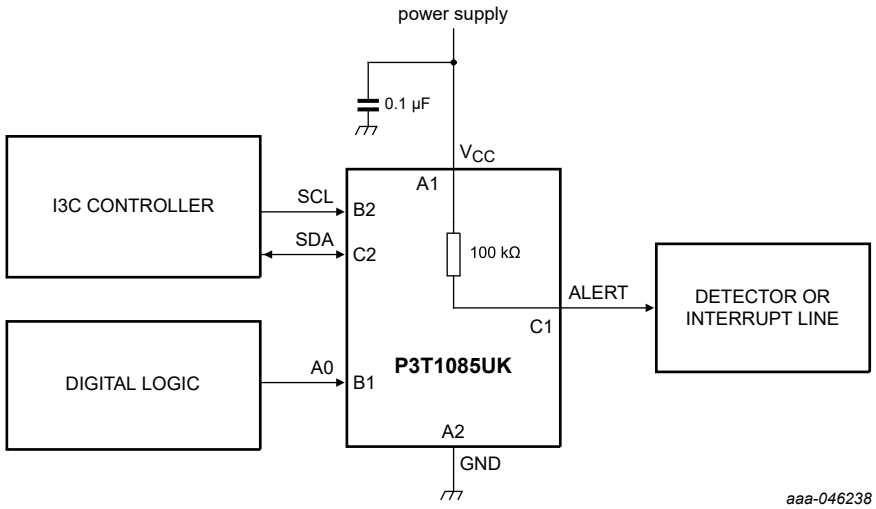


Figure 23. P3T1085UK I3C-bus typical application

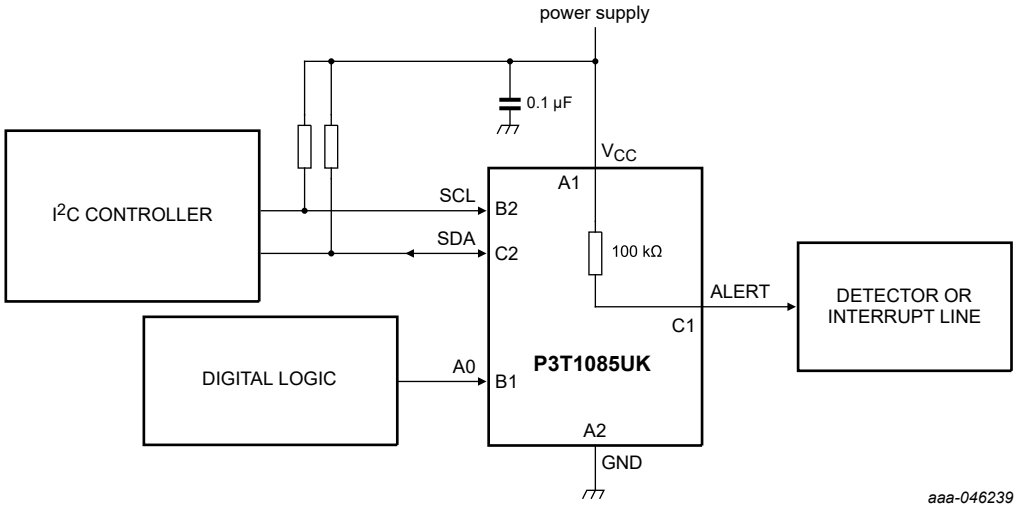


Figure 24. P3T1085UK I²C-bus typical application

8.2 Temperature accuracy

Because the local channel of the temperature sensor measures its own die temperature that is transferred from its body, the temperature of the device body must be stabilized and saturated for it to provide the stable readings. Because the device operates at a low-power level, the thermal gradient of the device package has a minor effect on the measurement.

The accuracy of the measurement is more dependent upon the definition of the environment temperature, which is affected by different factors: the printed-circuit board on which the device is mounted; the air flow contacting the device body (if the ambient air temperature and the printed-circuit board temperature are much different, then the measurement may not be stable because of the different thermal paths between the die and the environment).

The stabilized temperature liquid of a thermal bath provides the best temperature environment when the device is completely dipped into it. A thermal probe with the device mounted inside a sealed-end metal tube located in consistent temperature air also provides a good method of temperature measurement.

8.3 Noise effect

The device design includes the implementation of basic features for a good noise immunity:

- The 20 ns low-pass filter on both the bus pins SCL and SDA.
- The hysteresis of the threshold voltages to the bus input signals SCL and SDA, about 200 mV minimum.

However, good layout practices and extra noise filters are recommended when the device is used in a very noisy environment:

- Use decoupling capacitors at V_{CC} pin.
- Keep the digital traces away from switching power supplies.
- Apply proper terminations for the long board traces.
- Add capacitors to the SCL and SDA lines to increase the low-pass filter characteristics.

8.4 POR and I3C Communication

To execute the power-on reset (POR) successfully and ensure normal operation, V_{CC} requires a starting voltage that is less than 300 mV. If this is violated, the device may remain in an indeterminate state that causes I²C/I3C communication failure.

9 Limiting values

Table 24. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.3	+4.0	V
V_I	input voltage	SCL, A0 at V_{CC} = -0.3 V to +4 V	-0.3	+4.0	V
		SDA, ALERT at V_{CC} = +1.4 V to +4 V	-0.3	V_{CC} + 0.3 V & ≤ 4.0 V	V
		SDA, ALERT at V_{CC} = 0 V	-0.3	+4.0	V
V_I	input voltage	at input pins	-0.3	+4.0	V
I_I	input current	at input pins	-5.0	+5.0	mA
V_o	output voltage	at output pin	-0.3	+4.0	V
T_{oper}	operating temperature		−40	+125	°C
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	+150	°C
V_{ESD}	electrostatic discharge voltage	Human Body Model (HBM) JS-001-2017; all pins	-2000	+2000	V
		Charge Device Model (CDM) JS-002-2018; all pins	-1000	+1000	V

9.1 Thermal characteristics

Table 25. Thermal characteristics

Symbol	Parameter	Value (typ) [1]	Unit
θJA	Junction-to-ambient thermal resistance	135.5	℃/W
θJC(top)	Junction-to-case(top) thermal resistance	1.8	℃/W
θJB	Junction-to-board thermal resistance	25	℃/W
ΨJT	Junction-to-top characterization parameter	7	℃/W
ΨJB	Junction-to-board characterization parameter	20.3	℃/W

[1] P3T1085UK power dissipation is less than 1 mW. (See Table 27 for IQ vs different conditions.) The self-heating is neglectable.

10 Recommended operating conditions

Table 26. Recommended operating characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage			1.4	-	3.6	V
V_I	input voltage	SCL, A0		0	-	3.6	V
		SDA, ALERT at V_{CC} = +1.4 V to +3.6 V		0	-	V_{CC} + 0.3 & ≤ 3.6	V
		SDA, ALERT at V_{CC} = 0 V		0	-	3.6[1]	V
V_O	output voltage	digital pins		0	-	V_{CC} [2]	V
T_{amb}	ambient temperature			-40	-	+125	°C

[1] Allows the system to turn off P3T1085UK V_{CC} and keep I²C/I3C bus V_{CC} active for power management.
[2] For push-pull, the V_O max = V_{CC}. For open-drain, the pull-up V_O max = 3.6 V

11 Static characteristics

Table 27. Static characteristics

V_{CC} = 1.4 V to 3.6 V; T_{amb} = -40 °C to +125 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
T_{acc}	temperature accuracy	T = -20 °C to + 85 °C , 1.4 V ≤ V_{CC} ≤ 3.6 V	-0.5	-	+0.5	°C
		T = -40 °C to +125 °C 1.4 V ≤ V_{CC} ≤ 3.6 V	-1	-	+1	°C
T_{res}	temperature resolution	12-bit digital temp data	-	0.0625	-	°C
$t_{conv}(T)$	temperature conversion time	One-shot mode	-	7.8	12	ms
Con_{MOD}	conversion modes	CR1 = 0, CR0 = 0		0.25		Conv/s
		CR1 = 0, CR0 = 1 (default)		1		Conv/s
		CR1 = 1, CR0 = 0		4		Conv/s
		CR1 = 1, CR0 = 1		16		Conv/s
V_{POR}	power-on reset voltage	V_{CC} must ramp up from initial level < 300 mV	-	-	1.2	V
t_{act}	active time	I²C/I3C active after V_{CC} ≥ VPOR	-	-	20	ms
I_Q	Quiescent current	I²C bus inactive, CR1 = 0, CR0 = 1 (default), V_{CC} = 1.8 V, T_{amb} = 25 °C		2.1	3.5	µA
		I²C bus inactive, CR1 = 0, CR0 = 1 (default), V_{CC} = 1.8 V, –40°C to +85 °C			5.5	µA
		I²C bus inactive, CR1 = 0, CR0 = 1 (default), V_{CC} = 1.8 V, –40°C to +125 °C			13	µA
		I²C bus active, SCL frequency = 400 kHz, CR1 = 0, CR0 = 1 (default)		10		µA
		I²C bus active, SCL frequency = 3.4 MHz, CR1 = 0, CR0 = 1 (default)		80		µA
I_{SD}	Shutdown current	I²C bus inactive, V_{CC} = 1.8 V, T_{amb} = 25 °C		0.2	1.0	µA
		I²C bus active, SCL frequency = 400 kHz		8		µA
		I²C bus active, SCL frequency = 3.4MHz		75		µA
V_{IH}	HIGH-level input voltage	digital pins (SCL, SDA and A0)	0.7 x V_{CC}	-		V
V_{IL}	LOW-level input voltage	digital pins		-	0.3 xV_{CC}	V
I_{in}	input current	digital pins; 0V < V_{IN}< V_{CC} + 0.3 at T_{amb} = 25 °C	-		1	µA
V_{OL}	LOW-level output voltage	V_{CC} > 2 V ; I_{OL} = 3 mA	-	-	0.4	V

Table 27. Static characteristics...*continued*

V_{CC} = 1.4 V to 3.6 V; T_{amb} = -40 °C to +125 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
		V_{CC} < 2 V ; I_{OL} = 3 mA	-	-	0.2 x V_{CC}	V
R_{ALERT}	ALERT internal pullup resistor	ALERT to V_{CC}		100	130	kΩ
C_I	input capacitance	digital pins	-	-	10	pF

[1] Typical values are at V_{CC} = 1.8 V and T_{amb} = 25 °C, or values as specified for custom part number

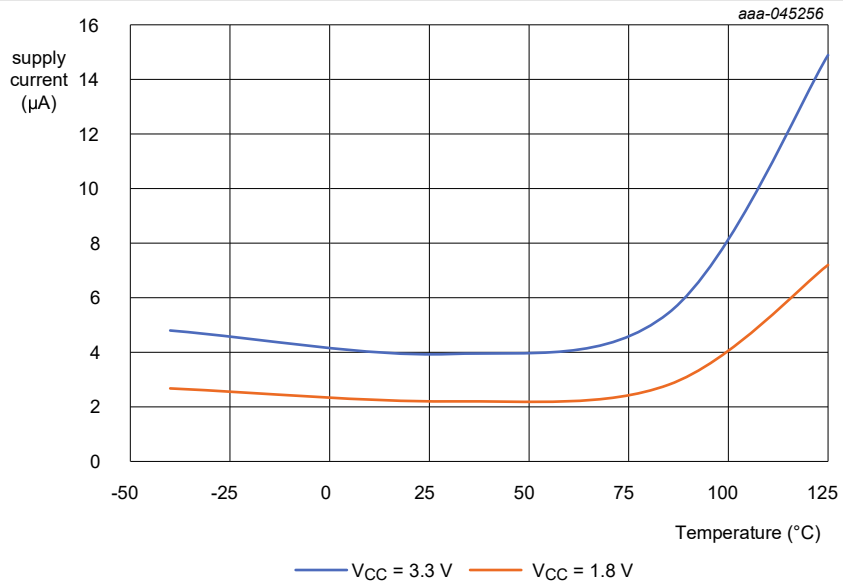


Figure 25. Supply current versus temperature (bus inactive; one conversion per second)

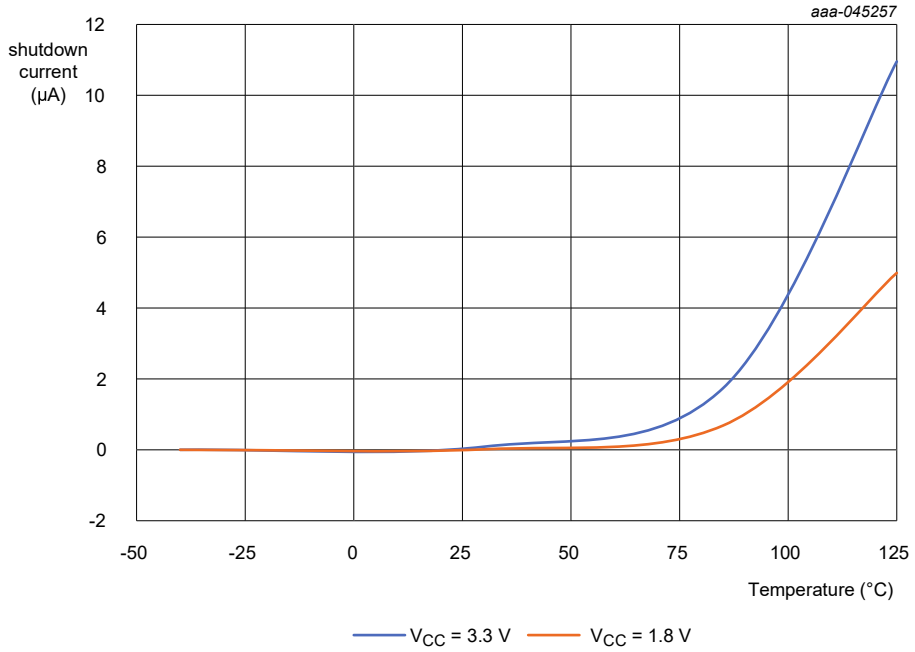


Figure 26. Shutdown current versus temperature

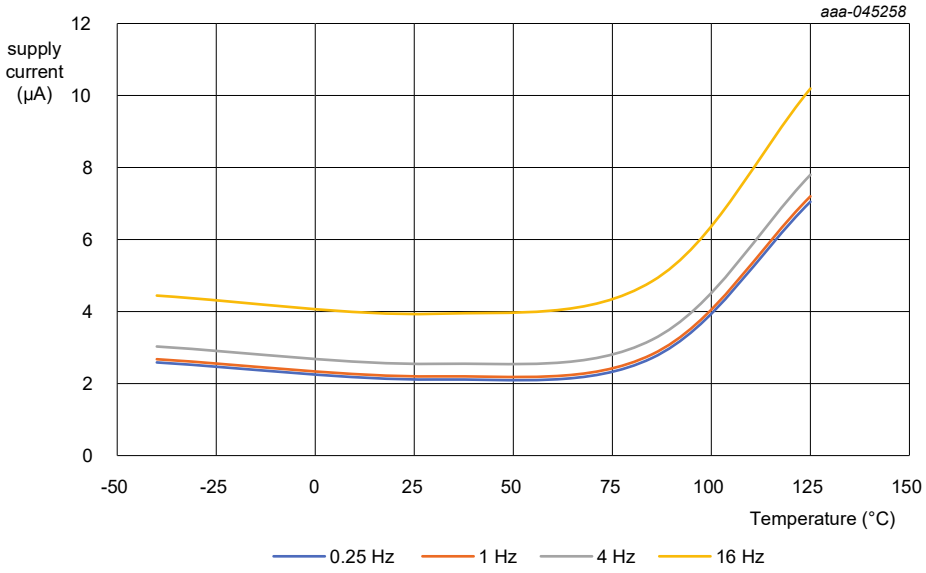


Figure 27. Supply current versus conversion rates and temperature (V_{CC}=1.8V, bus inactive)

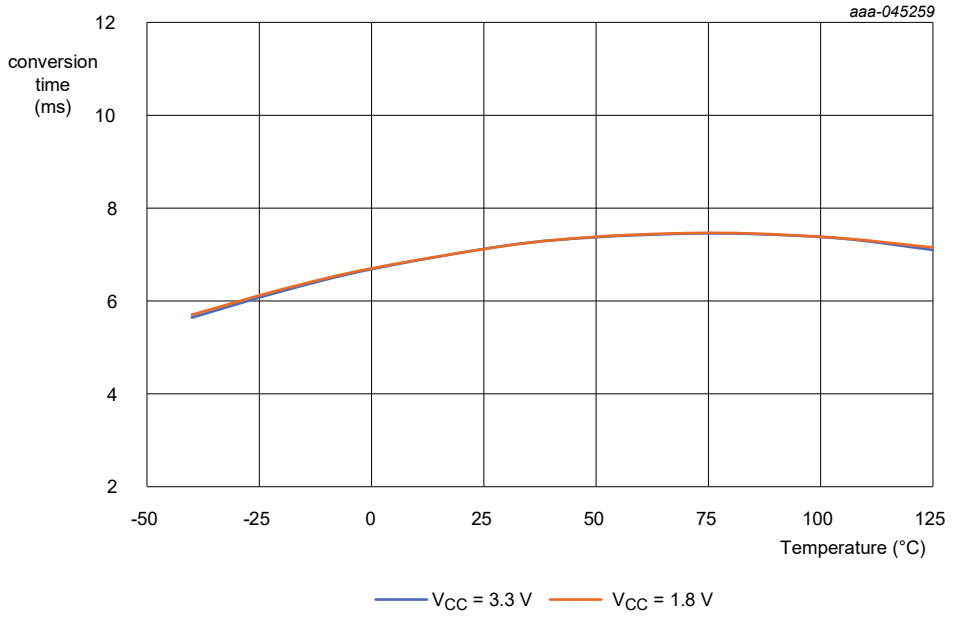


Figure 28. One-shot conversion time vs temperature

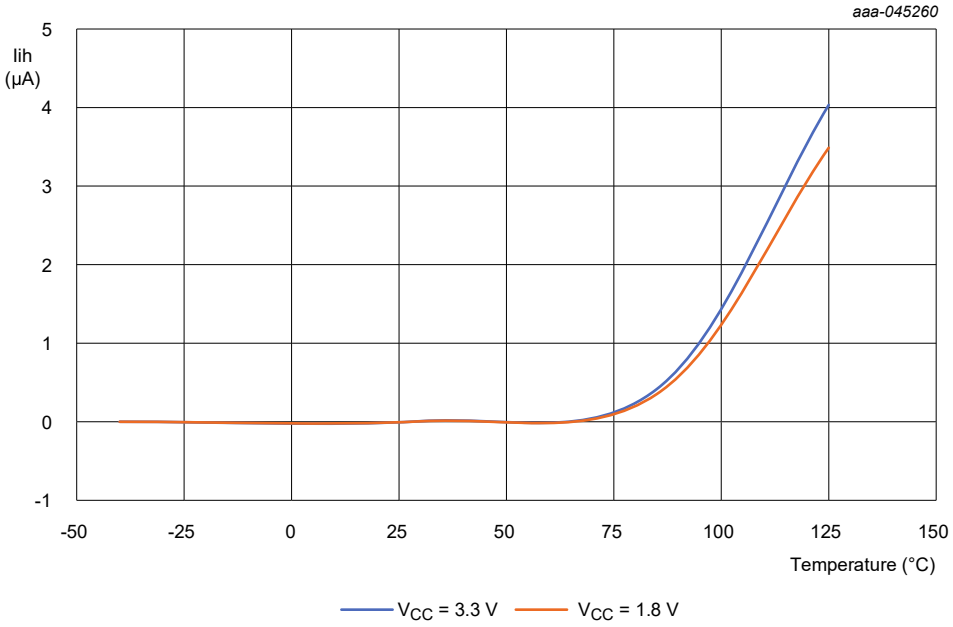


Figure 29. HIGH-level input current versus temperature; digital pins

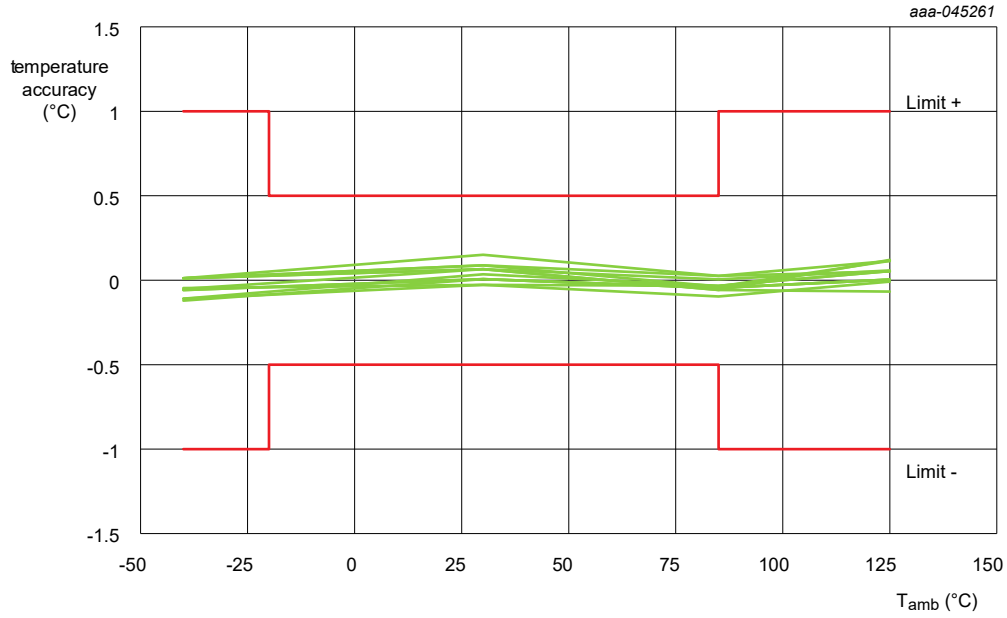


Figure 30. Accuracy vs temperature (V_{CC} = 1.4 V to 3.6 V)

12 Dynamic characteristics

Table 28. I²C-bus interface dynamic characteristics

V_{CC} = 1.4 V to 3.6 V; T_{amb} = −40 °C to +125 °C, unless otherwise specified. These specifications are guaranteed by design and not tested in production.

Symbol	Parameter	Conditions	Fast Mode		High speed mode		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency, $V_{CC} \geq$ 1.8 V	see Figure 31	0.001	0.4	0.001	3.4	MHz
	SCL clock frequency, V_{CC} < 1.8 V		0.001	0.4	0.001	2.5	MHz
t_{HIGH}	HIGH period of the SCL clock,		600	-	60	-	ns
t_{LOW}	LOW period of the SCL clock, $V_{CC} \geq$ 1.8 V		1300	-	160	-	ns
	LOW period of the SCL clock, V_{CC} < 1.8 V		1300	-	260	-	ns
$t_{HD;STA}$	hold time (repeated) START condition		600	-	160	-	ns
$t_{SU;DAT}$	data set-up time, $V_{CC} \geq$ 1.8 V		100	-	10	-	ns
	data set-up time, V_{CC} < 1.8 V		100	-	45	-	ns
$t_{HD;DAT}$	data hold time, $V_{CC} \geq$ 1.8 V		-	900	-	70	ns
	data hold time, V_{CC} < 1.8 V		-	900	-	130	ns
$t_{SU;STO}$	set-up time for STOP condition		0.6	-	0.16	-	µs
t_r,$t_{f(SCL)}$	Clock Rise/fall time		-	300	-	40	ns
t_r,$t_{f(SDA)}$	Data Rise/fall time		-	300	-	80	ns
t_r	Clock/data rise time	SCL ≤ 100 kHz	-	1000	-	-	ns

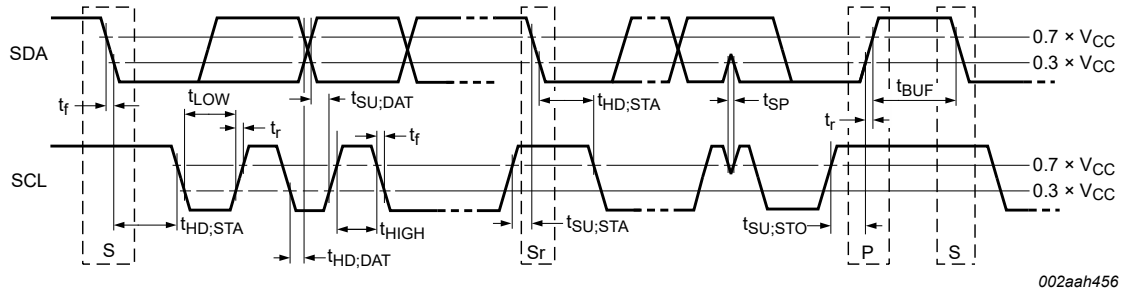


Figure 31. Timing diagram

Table 29. I3C-bus interface dynamic characteristics

V_{CC} = 1.4 V; T_{amb} = −40 °C to +125 °C, unless otherwise specified. These specifications are guaranteed by design and not tested in production.

Symbol	Parameter	Min	Typ	Max	Unit
I3C Open Drain Timing Parameters					
t_{HIGH}	HIGH period of the SCL clock			41	ns
t_{LOW_OD}	LOW period of the SCL clock	200		-	ns
t_{DIG_H}	Logic HIGH period of the SCL clock	32		t_{HIGH} + t_{CF}	ns

Table 29. I3C-bus interface dynamic characteristics...*continued*

V_{CC} = 1.4 V; T_{amb} = −40 °C to +125 °C, unless otherwise specified. These specifications are guaranteed by design and not tested in production.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{DIG\_OD\_L}$	Logic LOW period of the SCL clock	t_{LOW_ODmin} + t_{fDA_ODmin}			ns
t_{fDA_OD}	Fall time of SDA	t_{CF}		21	ns
t_{SU_OD}	SDA setup time during Open-Drain mode	3			ns
t_{CAS}	Clock after Start condition	38.4n			s
t_{CBP}	Clock before Stop condition	$t_{CASmin/2}$			s
$t_{MMoverlap}$	Current Controller to Secondary Controller Overlap time during handoff	$t_{DIG\_OD\_Lmin}$			ns
t_{AVAL}	Bus available condition	20			µs
t_{IDLE}	Bus idle condition	1			ms
t_{MMLock}	Time Internal Where New Controller Not Driving SDA Low	$t_{AVALmin}$			µs
I3C Push_Pull Timing Parameters					
f_{SCL}	SCL clock frequency	0.01	9.8	10	MHz
t_{HIGH}	HIGH period of the SCL clock	24		-	ns
t_{LOW}	LOW period of the SCL clock	57		-	ns
t_{DIG_H}	Logic HIGH period of the SCL clock	32		-	ns
t_{DIG_L}	Logic LOW period of the SCL clock	65		-	ns
$t_{DIG\_H\_MIXED}$	Logic HIGH period of the SCL clock for mixed bus	32		-	ns
t_{HIGH_MIXED}	HIGH period of the SCL clock for mixed bus	24		-	ns
t_{SCO}	Clock in to Data Out for Target			42	ns
t_{CR}	fall time of SCL signal	-	$150/f_{SCL}$		ns
t_{CF}	fall time of SCL signal	-	$150/f_{SCL}$		ns
t_{HD_PP}	SDA signal Data Hold in Push-Pull mode	0		-	ns
t_{SU_PP}	SDA signal Data setup in Push-Pull mode	3		-	ns
t_{CASr}	Clock after repeated Start(Sr)	t_{CASmin}		-	ns
t_{CBSr}	Clock before repeated Start(Sr)	$t_{CASmin}/2$		-	ns
C_b	Capacitive load per Bus Line(SCL/SDA)	-		50	pF

Table 30. I3C-bus interface dynamic characteristics

V_{CC} = 1.8 V; T_{amb} = −40 °C to +125 °C, unless otherwise specified. These specifications are guaranteed by design and not tested in production.

Symbol	Parameter	Min	Typ	Max	Unit
I3C Open Drain Timing Parameters					
t_{HIGH}	HIGH period of the SCL clock			41	ns
t_{LOW_OD}	LOW period of the SCL clock	200		-	ns

Table 30. I3C-bus interface dynamic characteristics...*continued*

V_{CC} = 1.8 V; T_{amb} = −40 °C to +125 °C, unless otherwise specified. These specifications are guaranteed by design and not tested in production.

Symbol	Parameter	Min	Typ	Max	Unit
t_{DIG_H}	Logic HIGH period of the SCL clock	32		t_{HIGH} + t_{CF}	ns
$t_{DIG\_OD\_L}$	Logic LOW period of the SCL clock	t_{LOW_ODmin} + t_{fDA_ODmin}			ns
t_{fDA_OD}	Fall time of SDA	t_{CF}		16	ns
t_{SU_OD}	SDA setup time during Open-Drain mode	3			ns
t_{CAS}	Clock after Start condition	38.4n			s
t_{CBP}	Clock before Stop condition	$t_{CASmin/2}$			s
$t_{MMoverlap}$	Current Controller to Secondary Controller Overlap time during handoff	$t_{DIG\_OD\_Lmin}$			ns
t_{AVAL}	Bus available condition	20			µs
t_{IDLE}	Bus idle condition	1			ms
t_{MMLock}	Time Internal Where New Controller Not Driving SDA Low	$t_{AVALmin}$			µs
I3C Push_Pull Timing Parameters					
f_{SCL}	SCL clock frequency	0.01	12.5	12.9	MHz
t_{HIGH}	HIGH period of the SCL clock	24		-	ns
t_{LOW}	LOW period of the SCL clock	38		-	ns
t_{DIG_H}	Logic HIGH period of the SCL clock	32		-	ns
t_{DIG_L}	Logic LOW period of the SCL clock	42		-	ns
$t_{DIG\_H\_MIXED}$	Logic HIGH period of the SCL clock for mixed bus	32		-	ns
t_{HIGH_MIXED}	HIGH period of the SCL clock for mixed bus	24		-	ns
t_{SCO}	Clock in to Data Out for Target			28	ns
t_{CR}	fall time of SCL signal	-	$150/f_{SCL}$		ns
t_{CF}	fall time of SCL signal	-	$150/f_{SCL}$		ns
t_{HD_PP}	SDA signal Data Hold in Push-Pull mode	0		-	ns
t_{SU_PP}	SDA signal Data setup in Push-Pull mode	3		-	ns
t_{CASr}	Clock after repeated Start(Sr)	t_{CASmin}		-	ns
t_{CBSr}	Clock before repeated Start(Sr)	$t_{CASmin}/2$		-	ns
C_b	Capacitive load per Bus Line(SCL/SDA)	-		50	pF

Table 31. I3C-bus interface dynamic characteristics

V_{CC} = 3.6 V; T_{amb} = −40 °C to +125 °C, unless otherwise specified. These specifications are guaranteed by design and not tested in production.

Symbol	Parameter	Min	Typ	Max	Unit
I3C Open Drain Timing Parameters					
t_{HIGH}	HIGH period of the SCL clock			41	ns

Table 31. I3C-bus interface dynamic characteristics...*continued*

V_{CC} = 3.6 V; T_{amb} = −40 °C to +125 °C, unless otherwise specified. These specifications are guaranteed by design and not tested in production.

Symbol	Parameter	Min	Typ	Max	Unit
t_{LOW_OD}	LOW period of the SCL clock	200		-	ns
t_{DIG_H}	Logic HIGH period of the SCL clock	32		t_{HIGH} + t_{CF}	ns
$t_{DIG\_OD\_L}$	Logic LOW period of the SCL clock	t_{LOW_ODmin} + t_{fDA_ODmin}			ns
t_{fDA_OD}	Fall time of SDA	t_{CF}		12	ns
t_{SU_OD}	SDA setup time during Open-Drain mode	3			ns
t_{CAS}	Clock after Start condition	38.4n			s
t_{CBP}	Clock before Stop condition	$t_{CASmin/2}$			s
$t_{MMoverlap}$	Current Controller to Secondary Controller Overlap time during handoff	$t_{DIG\_OD\_Lmin}$			ns
t_{AVAL}	Bus available condition	20			µs
t_{IDLE}	Bus idle condition	1			ms
t_{MMLock}	Time Internal Where New Controller Not Driving SDA Low	$t_{AVALmin}$			µs
I3C Push_Pull Timing Parameters					
f_{SCL}	SCL clock frequency	0.01	12.5	12.9	MHz
t_{HIGH}	HIGH period of the SCL clock	24		-	ns
t_{LOW}	LOW period of the SCL clock	24		-	ns
t_{DIG_H}	Logic HIGH period of the SCL clock	32		-	ns
t_{DIG_L}	Logic LOW period of the SCL clock	32		-	ns
$t_{DIG\_H\_MIXED}$	Logic HIGH period of the SCL clock for mixed bus	32		-	ns
t_{HIGH_MIXED}	HIGH period of the SCL clock for mixed bus	24		-	ns
t_{SCO}	Clock in to Data Out for Target			12	ns
t_{CR}	fall time of SCL signal	-	$150/f_{SCL}$		ns
t_{CF}	fall time of SCL signal	-	$150/f_{SCL}$		ns
t_{HD_PP}	SDA signal Data Hold in Push-Pull mode	0		-	ns
t_{SU_PP}	SDA signal Data setup in Push-Pull mode	3		-	ns
t_{CASr}	Clock after repeated Start(Sr)	t_{CASmin}		-	ns
t_{CBSr}	Clock before repeated Start(Sr)	$t_{CASmin}/2$		-	ns
C_b	Capacitive load per Bus Line(SCL/SDA)	-		50	pF

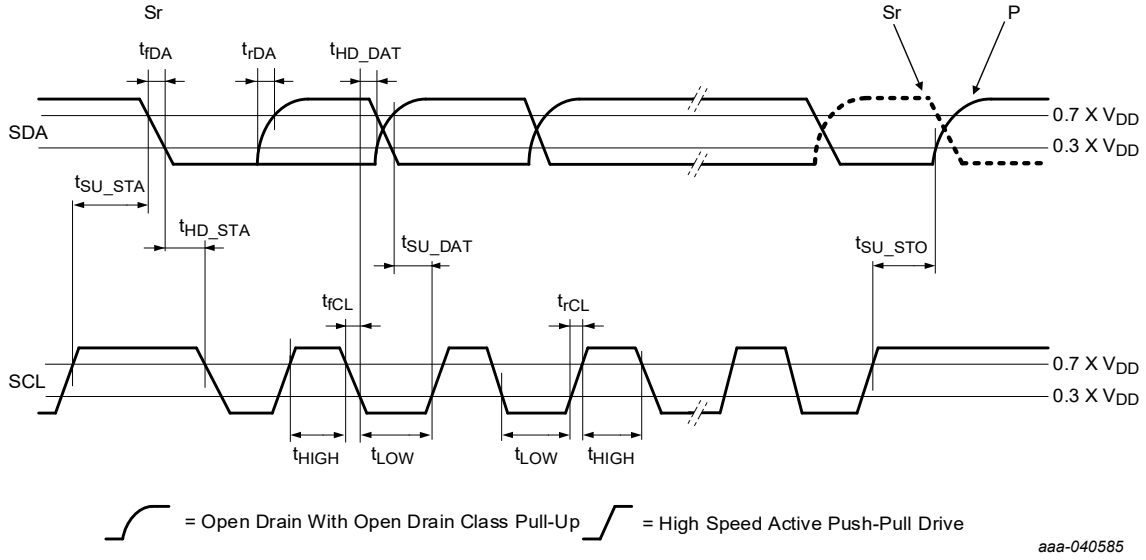


Figure 32. I3C timing diagram

13 Package outline

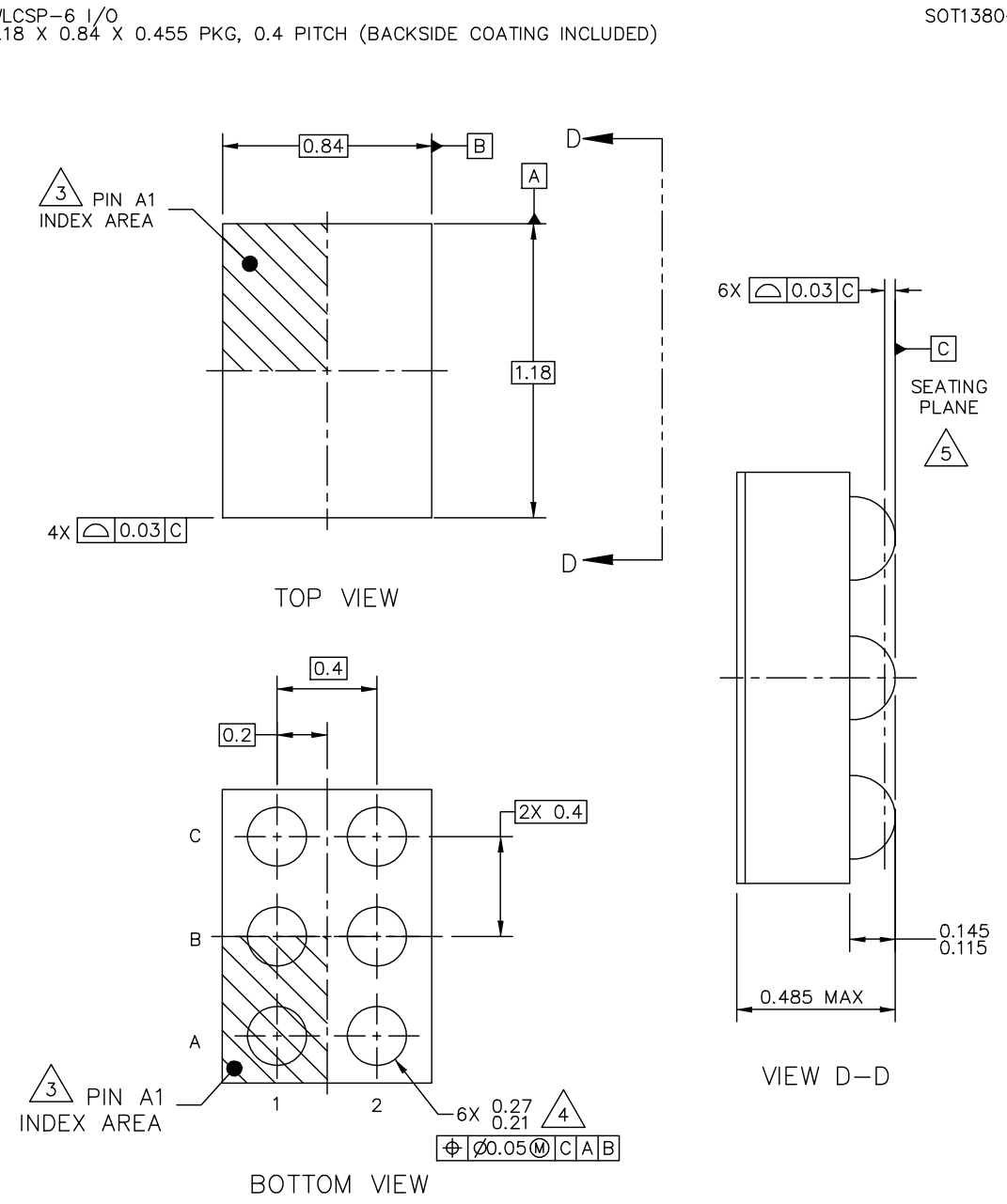


Figure 33. SOT1380-6 (WLCSP6) package outline

14 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 34) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board

- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 32 and Table 33

Table 32. SnPb eutectic process (from J-STD-020D)

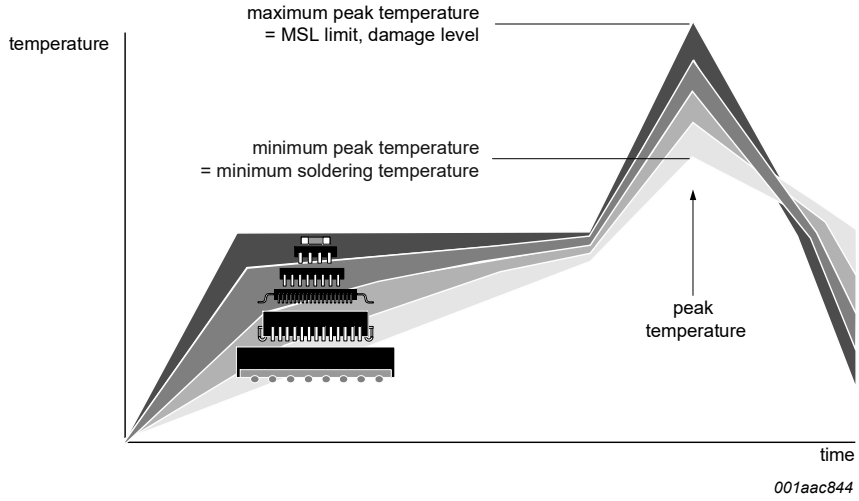
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 33. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 34.



MSL: Moisture Sensitivity Level

Figure 34. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

15 Soldering: PCB footprint

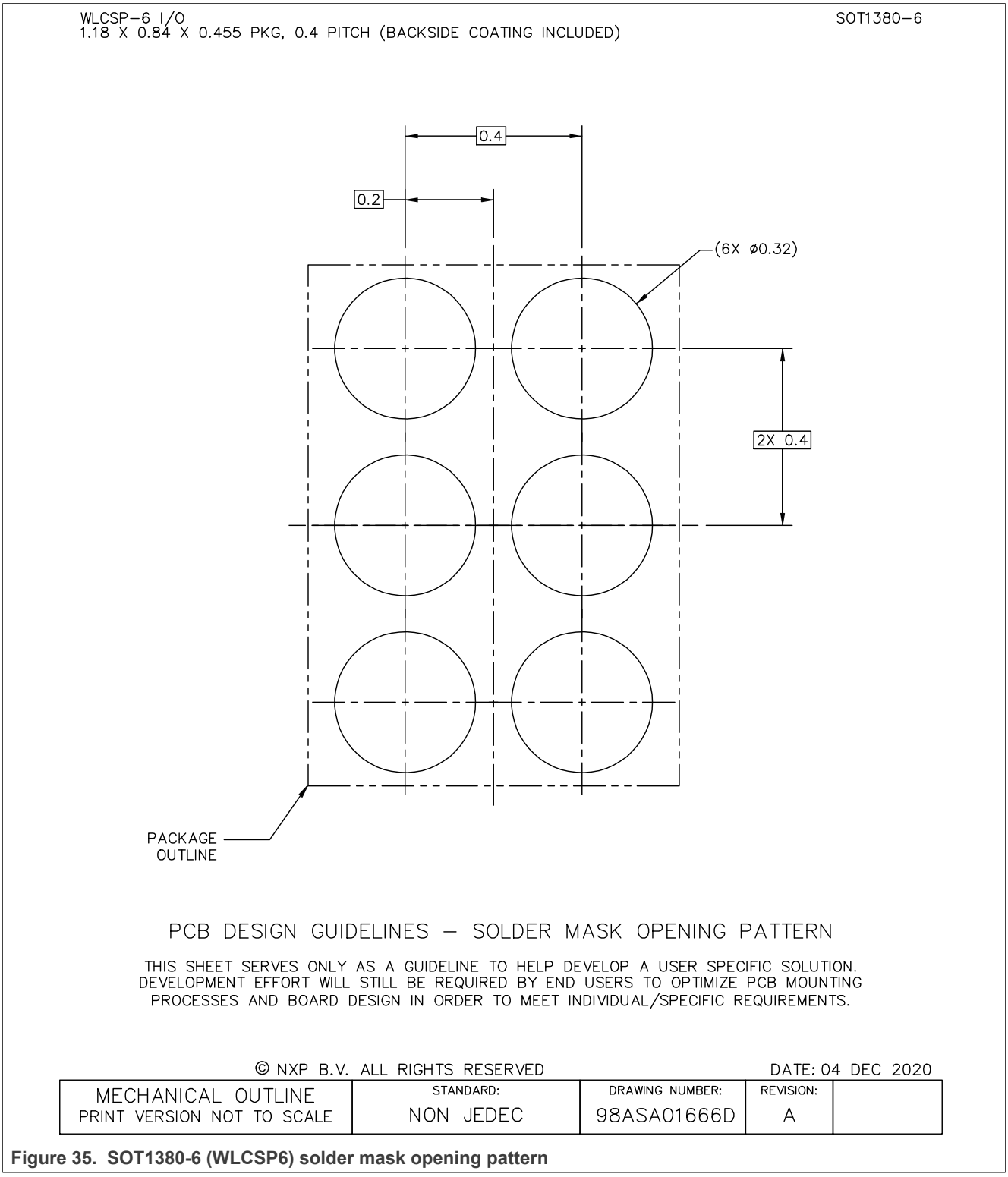
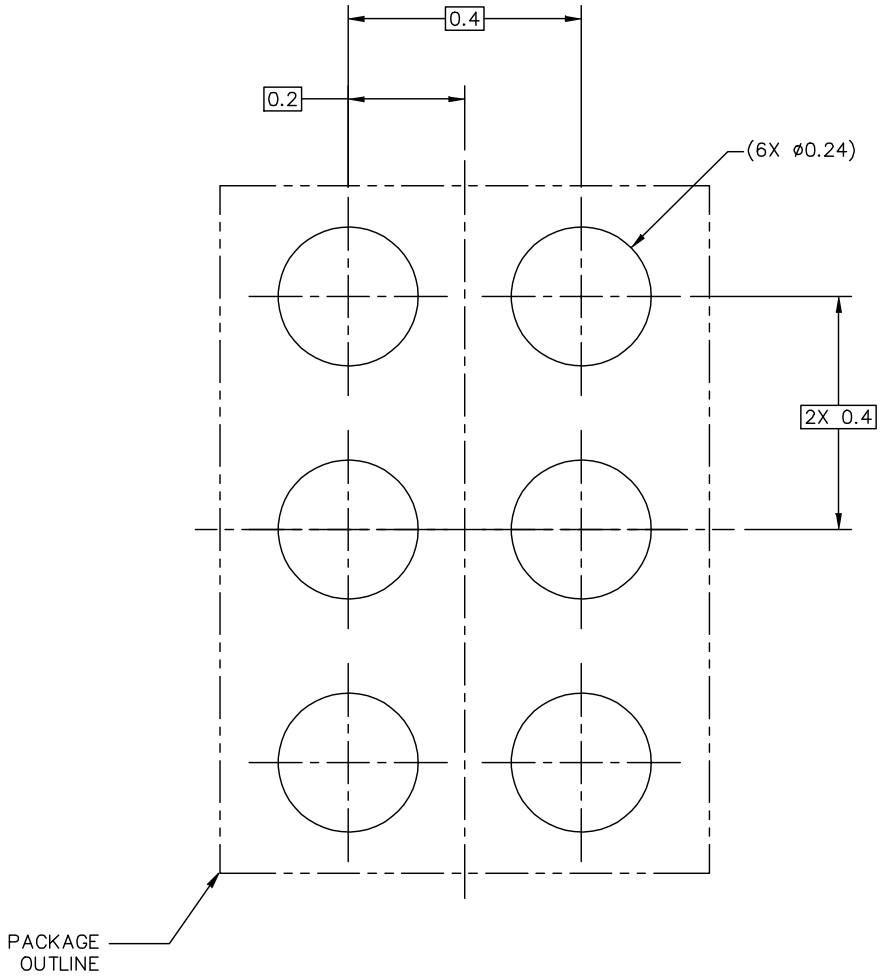


Figure 35. SOT1380-6 (WLCSP6) solder mask opening pattern

WLCSP−6 I/O
1.18 X 0.84 X 0.455 PKG, 0.4 PITCH (BACKSIDE COATING INCLUDED)

SOT1380−6



PCB DESIGN GUIDELINES − I/O PADS AND SOLDERABLE AREA

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Figure 36. SOT1380-6 (WLCSP6) I/O pads and solderable area

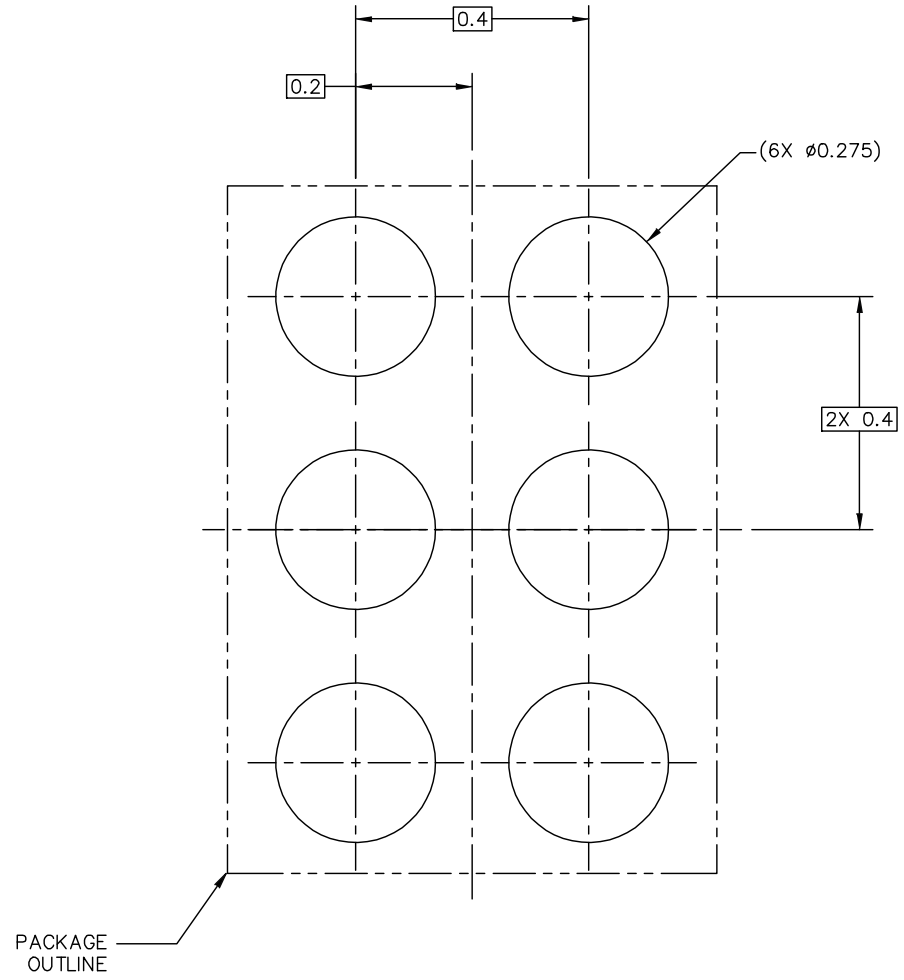

Figure 37. SOT1380-6 (WLCSP6) solder paste stencil

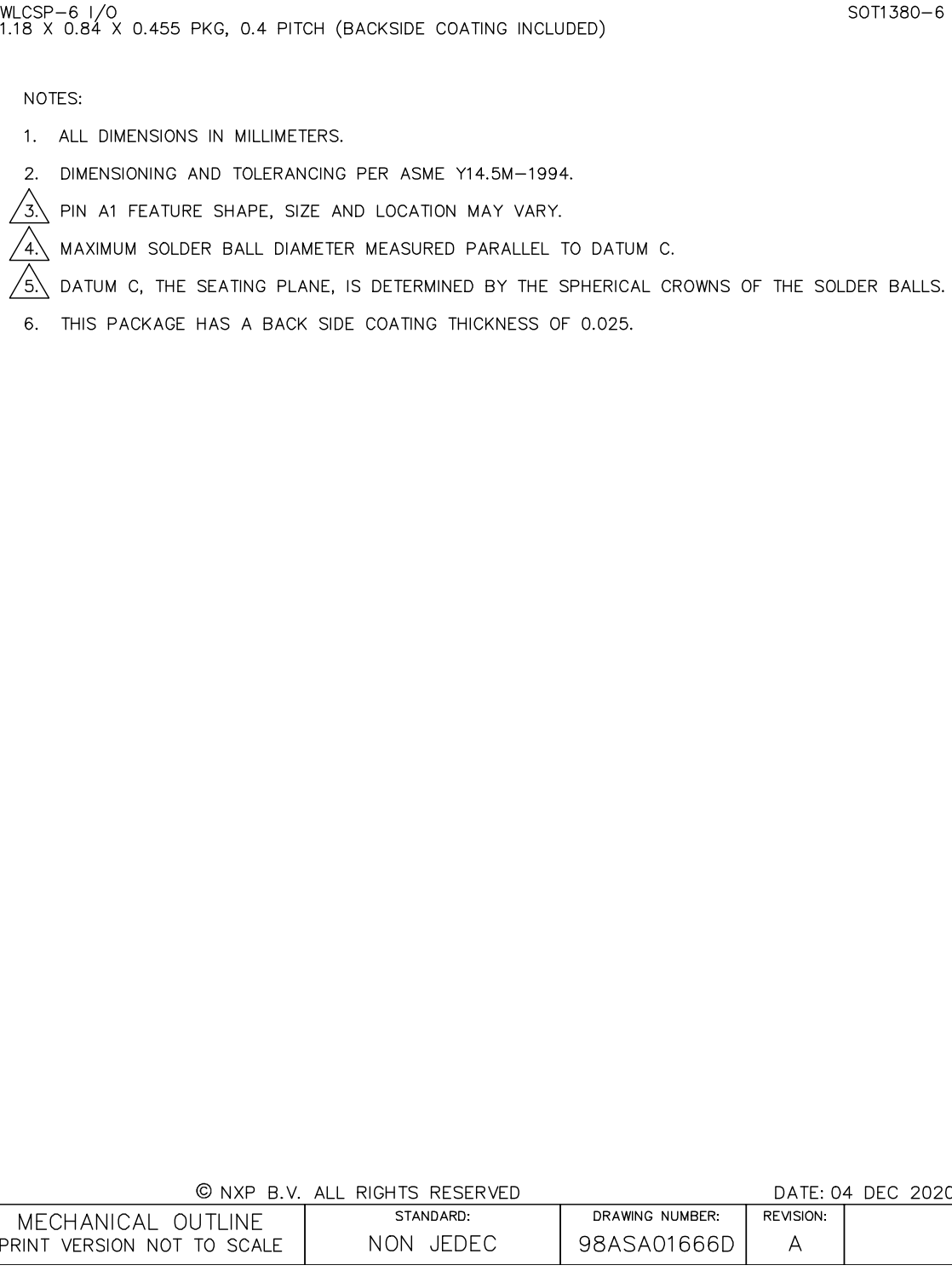

Figure 38. SOT1380-6 (WLCSP6) soldering notes

16 Abbreviations

Table 34. Abbreviations

Acronym	Description
A-to-D	Analog-to-Digital
CDM	Charged Device Model
ESD	ElectroStatic Discharge
HBM	Human Body Model
I^2C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
LSB	Least Significant Bit
LSByte	Least Significant Byte
MSB	Most Significant Bit
MSByte	Most Significant Byte
PCB	Printed-Circuit Board
POR	Power-On Reset
SMD	Solder Mask Defined

17 Revision history

Table 35. Revision history

Document ID	Release date	Supersedes
P3T1085UK v.1.2	10 September 2024	• Section 7.4.5.1: Removed "..., or to signify a Hot-Join event (ENHJ/DISHJ)."
P3T1085UK v.1.1	3 June 2024	• Added Section 8.4 • Table 27: Updated conditions for V_{POR}
P3T1085UK v.1.0	13 December 2022	Initial version

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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