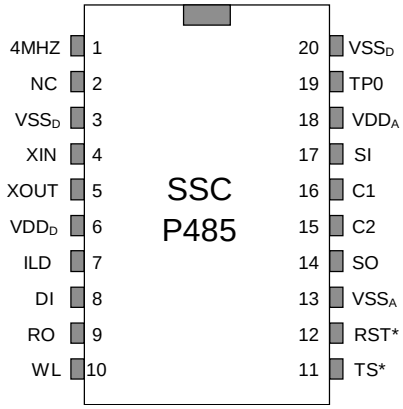
Technical Data Sheet **SSC P485 PL Transceiver IC**

Features

- Enables low-cost networking products
- Spread Spectrum Carrier™ communication technology
- 9600 baud data rate
- Simple interface
- Single +5 Volt power supply requirement
- 20 pin SOIC package

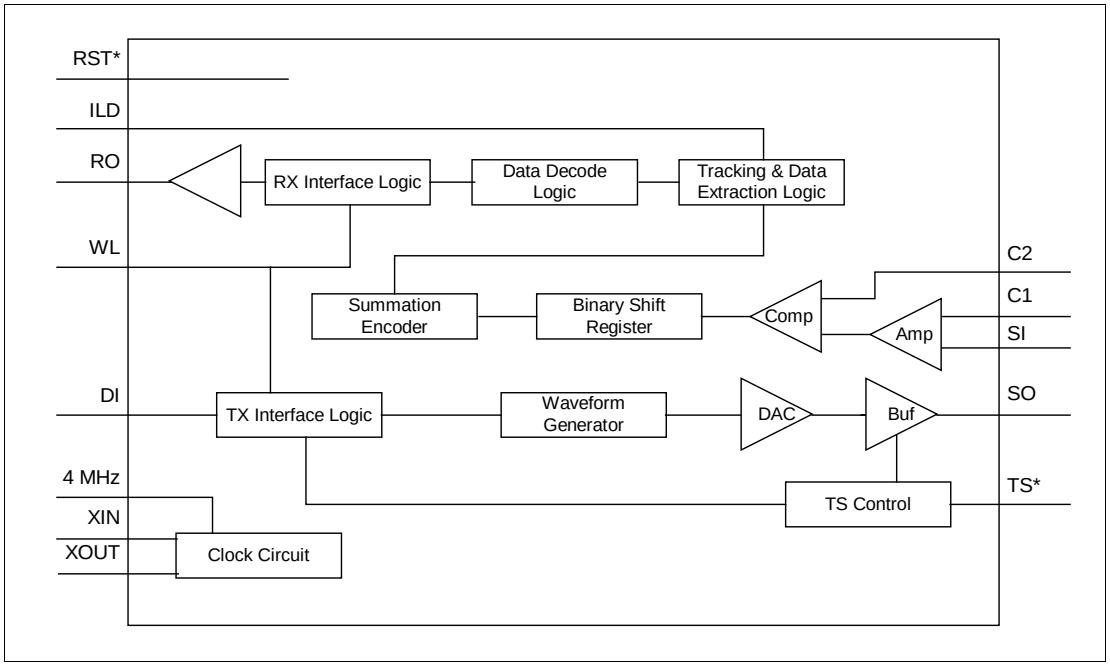


Introduction

The Intellon SSC P485 PL Transceiver IC is a highly integrated spread spectrum communication transceiver for implementing low-cost networking products. The SSC P485 contains a Spread Spectrum Carrier™ (SSC) transceiver, signal conditioning circuitry, and a simple host interface. A minimum of external circuitry is required to connect the SSC P485 to the DC power line, twisted pair cable, or other communication medium.

The inherent reliability of SSC signaling technology provides substantial improvement in network and communication performance over other low-cost communication methods. The SSC P485 is the ideal basic communications element for a wide variety of low-cost networking applications.

SSC P485 Block Diagram



Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
V_{DDMAX}	DC Supply Voltage	-0.3 to 7.0	V
V_{IN}	Input Voltage at any Pin	V_{SS}-0.3 to V_{DD}+0.3	V
T_{STG}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (Soldering, 10 seconds)	300	°C

Notes:
1. Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Recommended Operating Conditions

Symbol	Parameter	Min	Typical	Max	Unit
V_{DD}	DC Supply Voltage	4.5	5.0	5.5	V
F_{OSC}	Oscillator Frequency		12 ± 0.05%		MHz
T_A	Operating Temperature	-40	+25	+85	°C
	Humidity (non-condensing)			95	%

Electrical Characteristics

Conditions: V_{DD} = 4.5 to 5.5 V T= -40 to +85°C

Symbol	Parameter	Min	Typical	Max	Units
V_{OH}	Minimum High-level Output Voltage	2.4			V
V_{OL}	Maximum Low-level Output Voltage (1)			0.4	V
V_{IH}	Minimum High-level Input Voltage	2.0			V
V_{IL}	Maximum Low-level Input Voltage			0.8	V
I_{IL}	Maximum Input Leakage Current			±10	µA
v_{SO}	SSC Signal Output Voltage (2)		4		V_{P-P}
I_{DD}	Total Power Supply Current		15		mA

Notes:
1. TS* pin I_{OL} = 4 mA, all other outputs I_{OL} = 2 mA
2. Z_L = 2K Ω || 10 pF

SSC P485 Pin Assignments

Pin	Mnemonic	Name	Description
1	4MHZ	4 MHz Clock Out	4 MHz clock output available for host microcontroller.
2	NC	No Connect	
3	VSS_D	Digital Ground	Digital ground reference.
4	XIN	Crystal Input	Connected to external crystal to excite the IC's internal oscillator and digital clock.
5	XOUT	Crystal Output	Connected to external crystal to excite the IC's internal oscillator and digital clock.
6	VDD_D	Digital Supply	5.0 VDC ± 10% digital supply voltage with respect to VSS_D.
7	ILD	Idle Line Detect	Digital output, active high. Logic 1 state indicates 10 bit times of idle line, logic 0 indicates detection of carrier or non-idle line.
8	DI	Driver Input	Digital input. After the preamble, a low on DI (SPACE) transmits a superior2 state on SO, a high on DI (MARK) transmits a superior1 state on SO.
9	RO	Receiver Output	Digital output. After the preamble and assuming standard polarity: if superior1 state is detected on SI, RO will be high (MARK), if superior2 state is detected on SI, RO will be low (SPACE).
10	WL	Word Length	Digital input. Logic 1 (default, internal pullup) selects 10-bit frame (START, eight data bits, STOP), logic 0 selects 11-bit frame (START, nine data bits, STOP).
11	TS*	Tristate	Active low digital output. Enables the external output amplifier when driven high. Tri-states the external output amplifier when driven low.
12	RST*	Reset	Active low digital input. RST* asynchronously forces RO and ILD outputs to a high state and TS* to a low state. RST* can be asserted anytime during normal operation to force the reset state. RST* must be active (low) for 1 µsec after VDD_D and VDD_A stabilize and the crystal oscillator stabilizes to guarantee the internal reset state. See Figure 10.
13	VSS_A	Analog Ground	Analog ground reference.
14	SO	Signal Output	Analog signal output. Tri-state enabled with internal signal.
15	C2	Capacitor 2	Connection for 680pF capacitor to ground.
16	C1	Capacitor 1	Connection for 680pF capacitor to ground.
17	SI	Signal Input	Analog signal input.
18	VDD_A	Analog Supply	5.0 VDC ± 10% analog supply voltage with respect to VSS_A.
19	TP0	Test Point 0	Reserved pin for testing.
20	VSS_D	Digital Ground	Digital ground reference.

SSC P485 Application Examples

The SSC P485 may be used in a wide variety of applications. A typical node connecting to the medium is shown in Figure 1. A gateway between an RS485 twisted pair network and a DC power line network is shown in Figure 2. A multi-point network application with gateways using the SSC P485 is illustrated in Figure 3. Figure 4 presents a host interface flow diagram showing the major steps necessary to transmit and receive messages using the P485 IC.

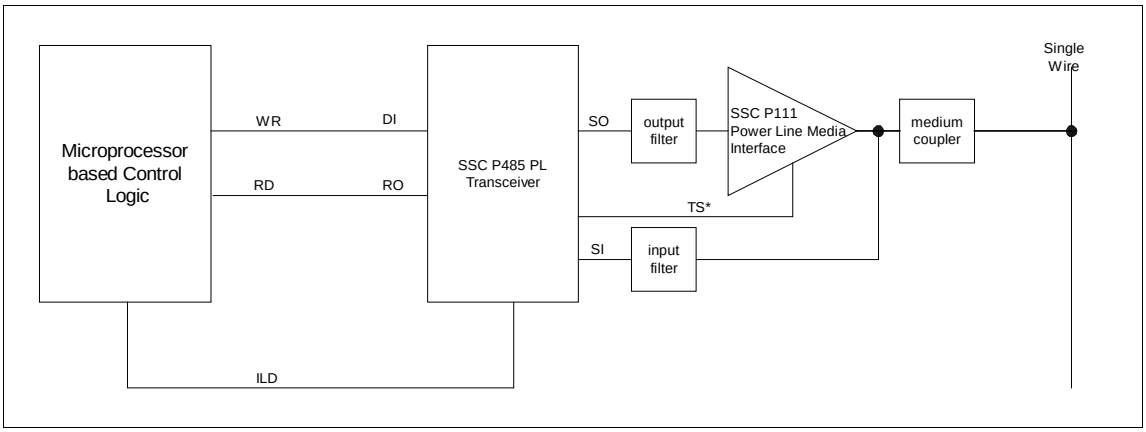


Figure 1. SSC P485 Typical Node

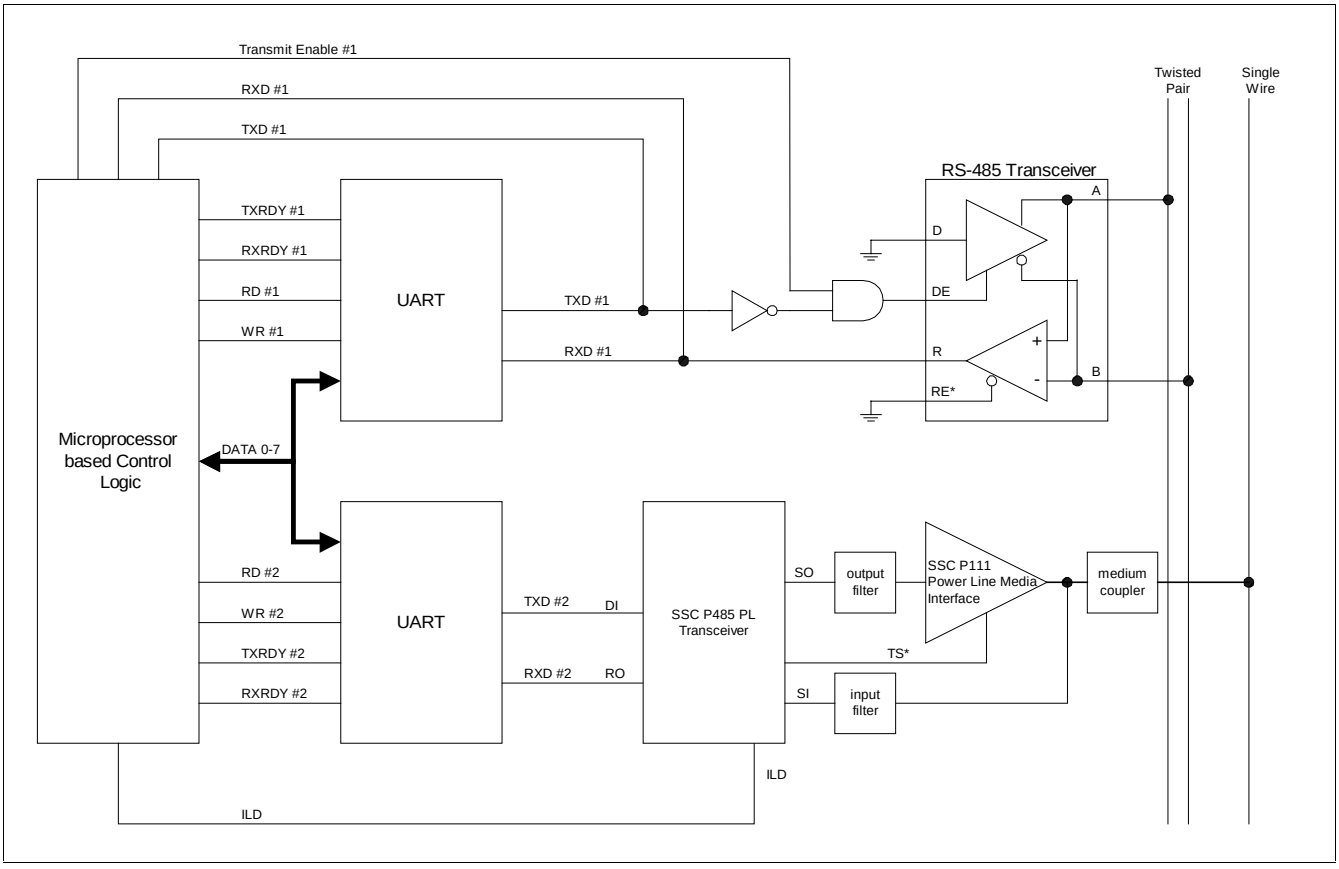


Figure 2. SSC P485 Gateway

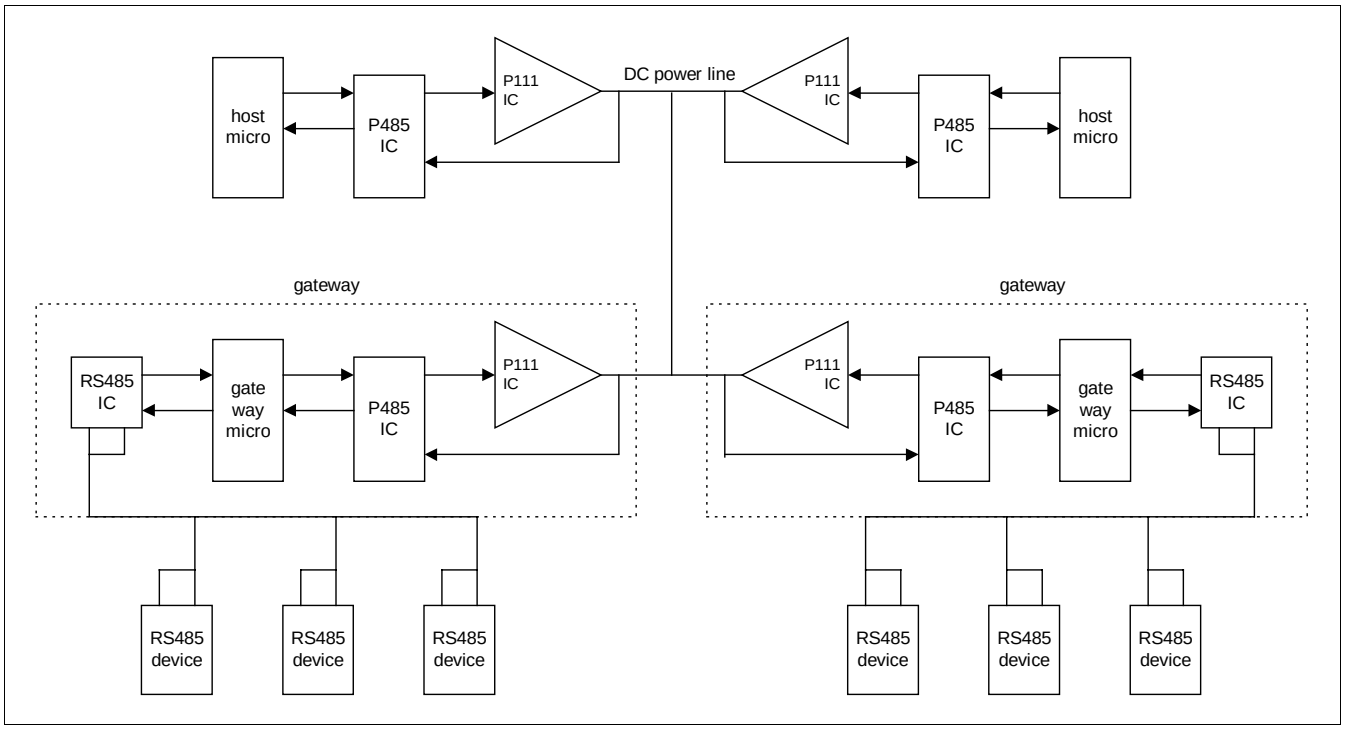


Figure 3. SSC P485 Multi-point Network Application

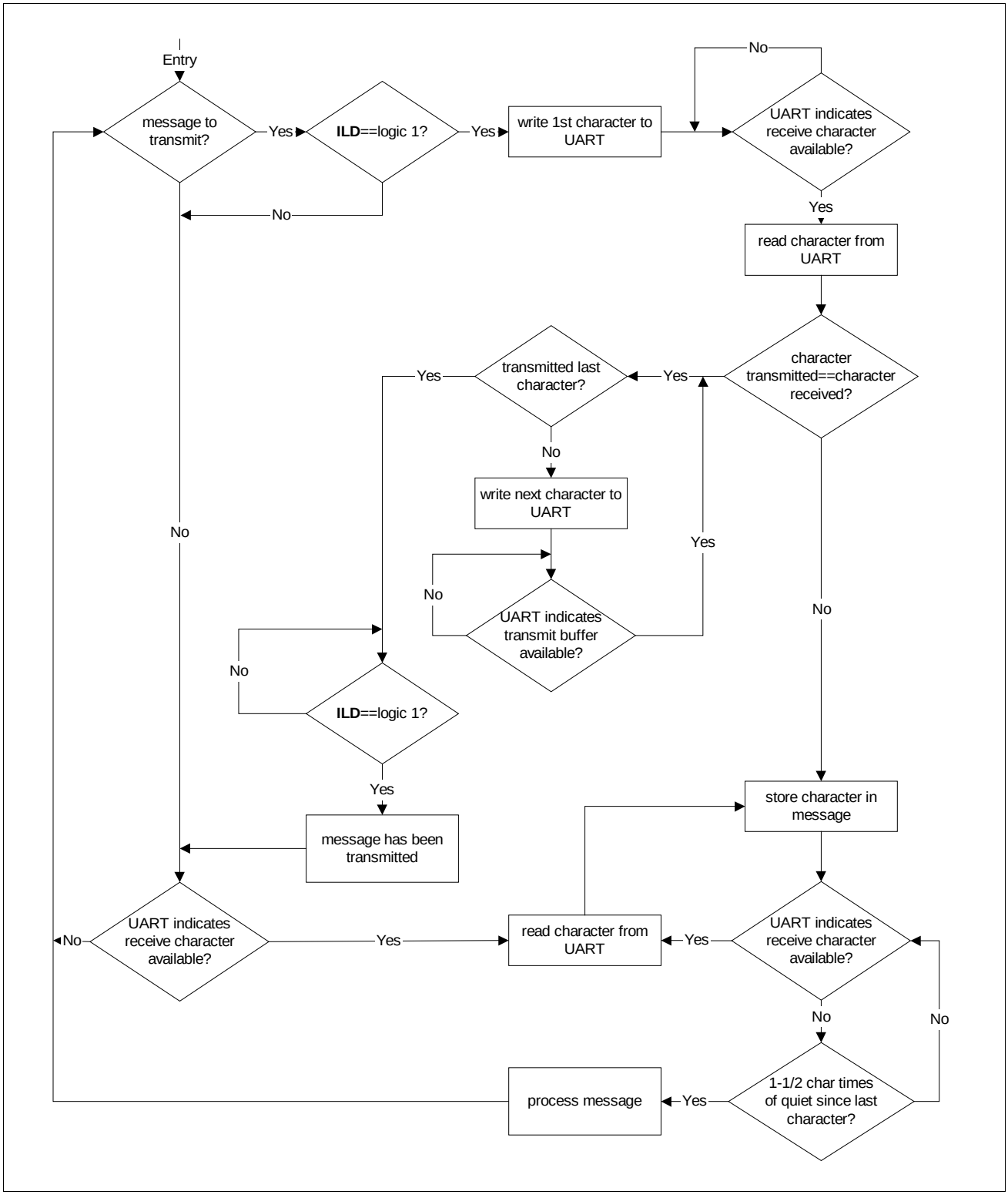


Figure 4. Host Interface Flow Diagram

SSC P485 Power Line Interface

Analog data is transferred between the communication medium and the SSC P485 over the Signal In (SI) and Signal Out (SO) pins (refer to Figure 5). When transmitting, SSC “chirps” from the SSC P485 SO pin are filtered by the output filter to remove harmonic energy (distortion) from the transmit signal and then amplified by the SSC P111 Power Line Media Interface IC. The SSC P111 is a high-efficiency amplifier and tri-state switch specifically designed for use in power line network systems. The amplifier is powered down and its output set to a high impedance condition when the SSC P485 TS* signal is logic low, isolating the amplifier from the receive circuitry and reducing node power consumption during receive operation. When the SSC P485 TS* signal is logic high, the communication signal is routed to the communication medium through the coupling circuit (capacitor or transformer). When receiving, the communication signal passes through the coupling circuit and is filtered by the bandpass input filter. The resulting signal is then applied to the SSC P485 SI pin for processing. Refer to the application reference shown in Figure 14.

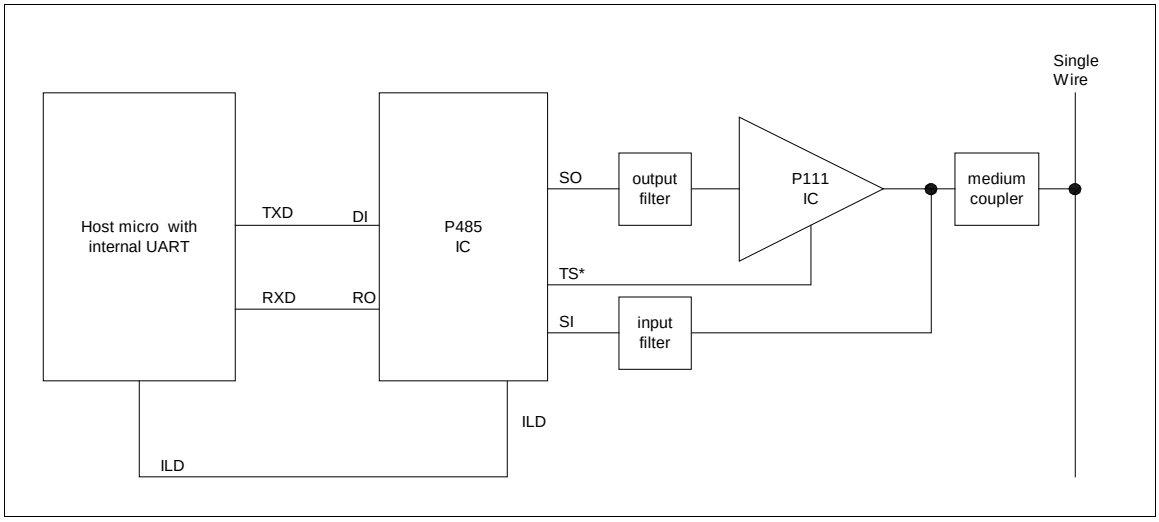


Figure 5. SSC P485 Medium Coupling

SSC P485 Message Format

The P485 requires the following message formatting:

Start bits	1, logic low
Data bits	8 or 9 (default 8)
Stop bits	1, logic high
Character gap	0-4 bit times
Message gap	12 bit times minimum
Message length	1 character minimum

Transmit/Receive Timing

The SSC P485 timing with contention resolution is shown below. The P485 generates a preamble based on the first character of the message. Contention resolution requires that the first character of the message be unique among all possible transmitters in the network. If the channel is available and the transmitter wins contention, a tracking sync sequence followed by a retransmission of the first character occurs. The P485 also echoes the first character back to the host allowing the host to determine that the channel was available and to continue transmitting the message. If the channel was unavailable (the transmitter lost contention), the SO line is tri-stated and the first character of the received message is passed to the host. The host determines that the channel was not available (transmitted first character does not match received first character), and the host enters the receive message mode. Once the end of message is detected, the P485 drives ILD high after 10 bit times to allow all nodes to arbitrate properly. The end of packet condition is true when 5 consecutive ones are detected on DI following a stop bit. Figure 6 shows a contention resolution example for two contending transmitters, and Figure 7 shows the end of message sequence and the assertion of ILD. Refer to Figure 9 for preamble and data encoding.

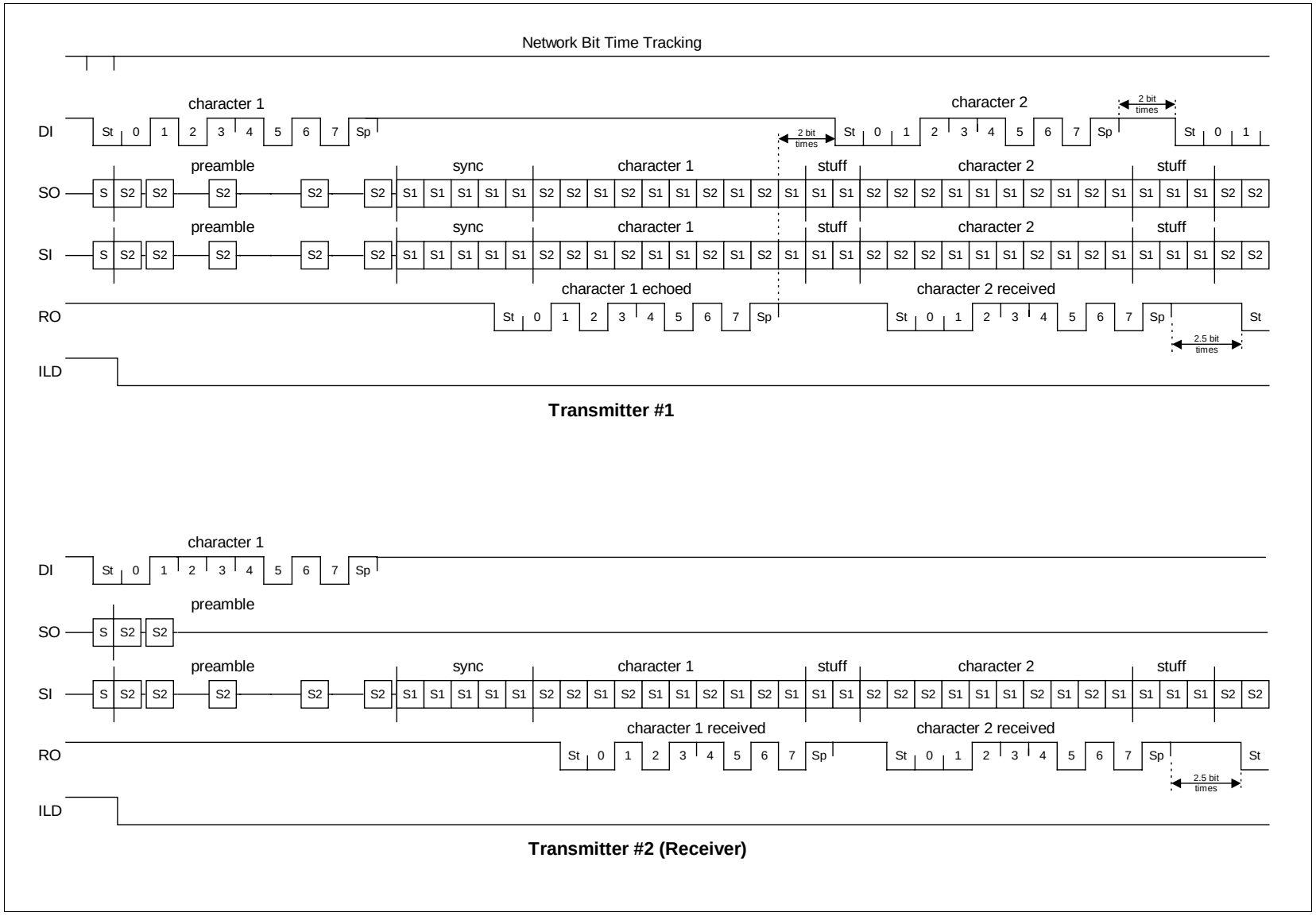


Figure 6. Contention Resolution Timing

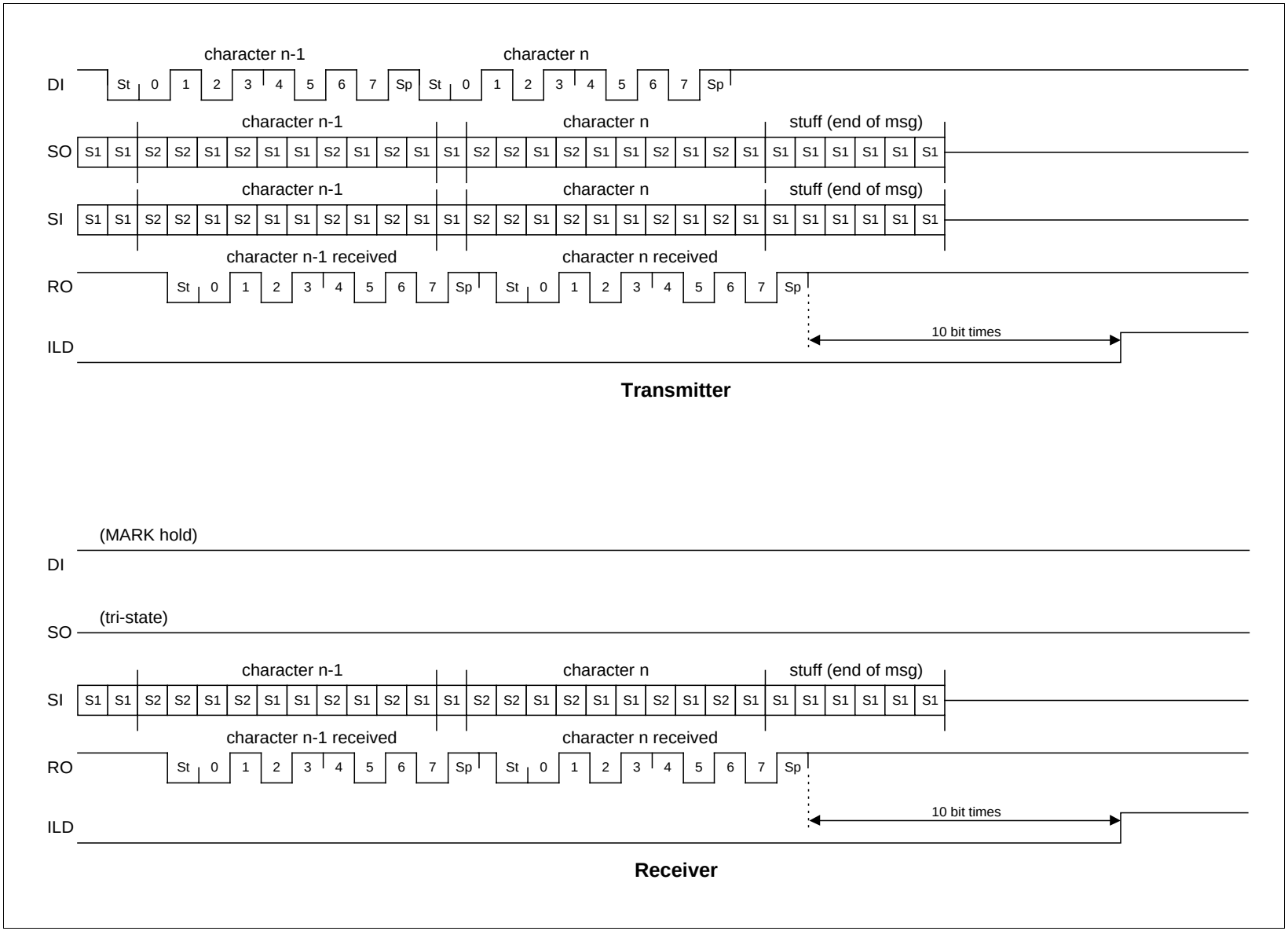


Figure 7. End of Message Timing

Spread Spectrum Carrier™ Technology

Spread Spectrum Carrier™ (SSC) Technology is a method of spread spectrum communications suitable for both point-to-point or carrier sense multiple access (CSMA) networks. Historically, spread spectrum communication systems have been used for secure communications and/or to overcome narrow-band impairments in the communications medium. Spread spectrum receivers generally require an initial period of time to synchronize with the carrier, so they have not been appropriate for CSMA networks. Spread Spectrum Carrier Technology is a method by which a series of short, self-synchronizing, frequency swept "chirps" act as a carrier. The chirps are always of the same known pattern and detectable by all of the nodes on the network. The chirp ranges in frequency from 100 to 400 kHz over a duration of 100 µs. The chirp is swept from approximately 200 kHz to 400 kHz and then from 100 kHz to 200 kHz. Figure 8 illustrates the SSC power line chirp.

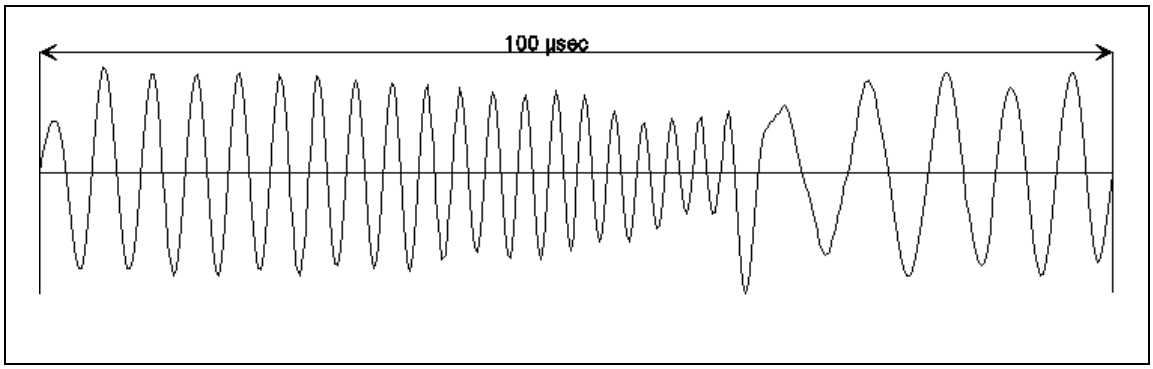


Figure 8. Spread Spectrum Carrier Chirp

Preamble Encoding

Two modulation schemes are used for symbol transmission by the physical layer. Amplitude Shift Keying (ASK) is used in the preamble of the message packet. ASK modulation uses SUPERIOR and INFERIOR states to encode symbols. A SUPERIOR state is represented by the presence of a chirp and an inferior state by the absence of a chirp. Because the transmitter is quiet during inferior states, superior states transmitted by other devices contending for the channel can be detected during the preamble of the packet. An example of ASK modulation is shown in Figure 9. Note that in the preamble, the duration of a symbol is slightly longer than in the body of the packet. A preamble symbol is 114 µs in length. Symbols in the sync sequence and the Packet Body are 100 µs in length. Please note the “Chirp” is ALWAYS 100µs in length and is followed by 14 µs of quiet time during the preamble.

Data Encoding

Phase Reversal Keying (PRK) utilizes two phases of the SUPERIOR state, SUPERIOR S1 and SUPERIOR S2, which are 180° out of phase with one another, to modulate the encoded data. This modulation technique is more robust than the ASK technique, because it allows the P485 to correlate and track each symbol rather than just those encoded as SUPERIOR states. Figure 9 shows an example of PRK.

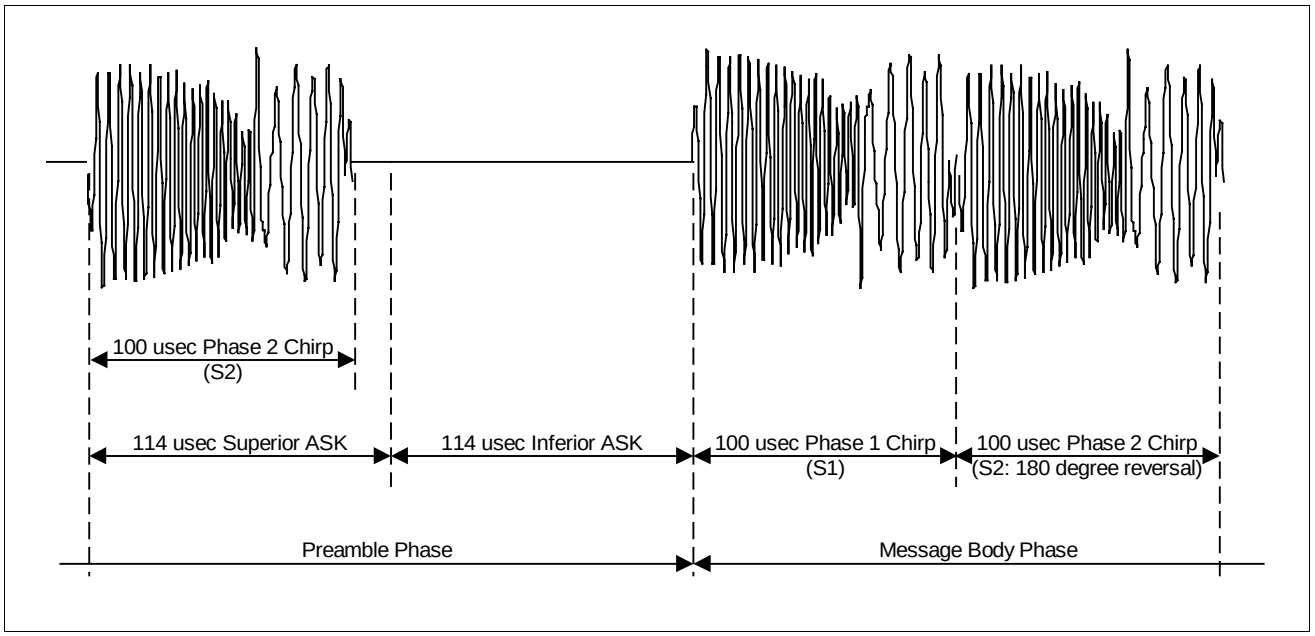


Figure 9. ASK and PRK Data Patterns

Timing Diagrams

All timing values are referenced from the 50% mid-point between VDD and VSS. All output timings assume 50 pF load at the pin.

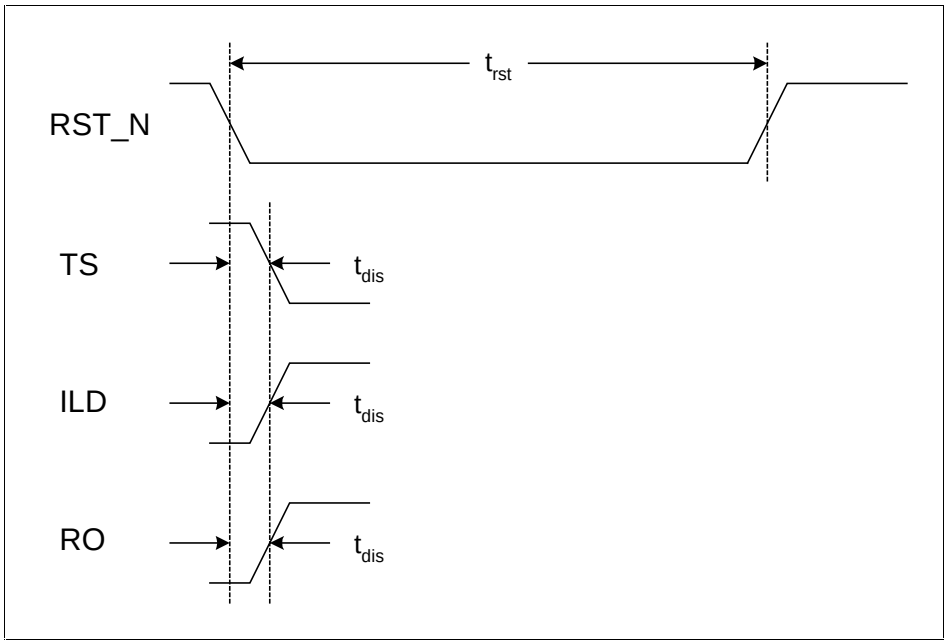


Figure 10. Reset Timing

Table 1. Reset Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units	Notes
t_{rst}	Reset Pulse Width	300	-	-	ns	
t_{dis}	Output Disable Time	3	-	20	ns	1

Notes: 1. Signals are forced asynchronously to their inactive state on reset.

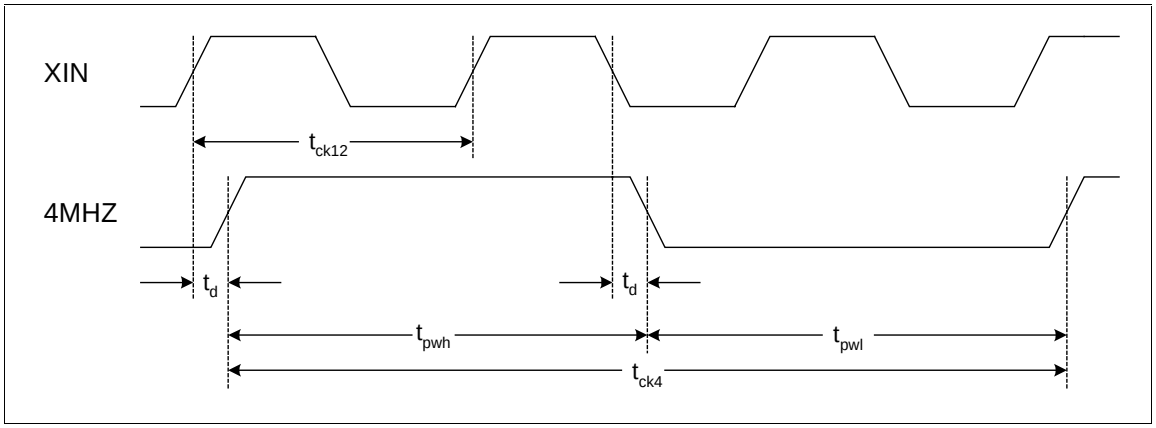


Figure 11. 4 MHz Clock Output Timing

Table 2. 4 MHz Clock Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units	Notes
t_d	Output Delay	3	-	20	ns	
t_{ck12}	Input Clock Period	83.288	83.333	83.375	ns	1
t_{ck4}	Output Clock Period	249.75	250	250. 25	ns	2
t_{pwh}	Pulse Width High	-	125	-	ns	3
t_{pwl}	Pulse Width Low	-	125	-	ns	3

Notes:
1. Oscillator frequency is 12 MHz ± 0.05%.
2. Clock frequency is 4 MHz ± 0.1%. Assumes XIN is 12 MHz ± 0.05%.
3. Actual pulse width is determined by duty cycle of the oscillator.

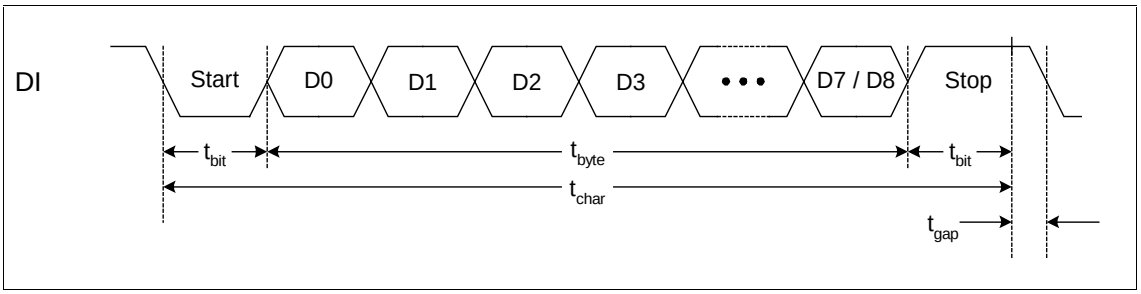


Figure 12. DI Input Timing

Table 3. DI Input Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units	Notes
t_{bit}	Bit Pulse Width	101.01	104.16	107.52	us	1
	Baud Rate	9300	9600	9900	baud	1
t_{gap}	Inter-Character Gap	0	-	430.08	us	
	Inter-Character Bits	0	< 1	4	bits	
t_{byte}	Byte Length	8	-	9	bits	
t_{char}	Character Length	10	-	11	bits	

Notes: 1. Corresponds to one bit width.

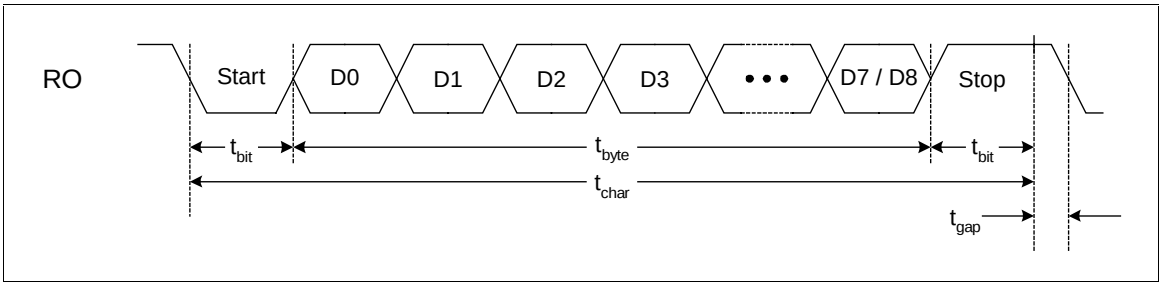


Figure 13. RO Output Timing

Table 4. RO Input Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units	Notes
t_{bit}	Bit Pulse Width	100.00	104.16	104.42	us	1
	Baud Rate	9576	9600	10000	baud	1
t_{gap}	Inter-Character Gap	0	-	469.89	us	2
	Inter-Character Bits	0	-	4.5	bits	2
t_{byte}	Byte Length	8	-	9	bits	
t_{char}	Character Length	10	-	11	bits	

Notes:
1. Corresponds to one bit width. RO output is nominally 9600 baud. If the received baud rate exceeds 9600 baud, the receiver will adjust RO's output baud rate to prevent internal buffer overflow.
2. Inter-character gap on RO's output is a function of the received character rate and transmitted inter-character gap. Transmitted baud rates of less than 9600 baud increases the inter-character gap on RO's output. Transmitted baud rates of greater than 9600 baud decreases the inter-character gap on RO's output.

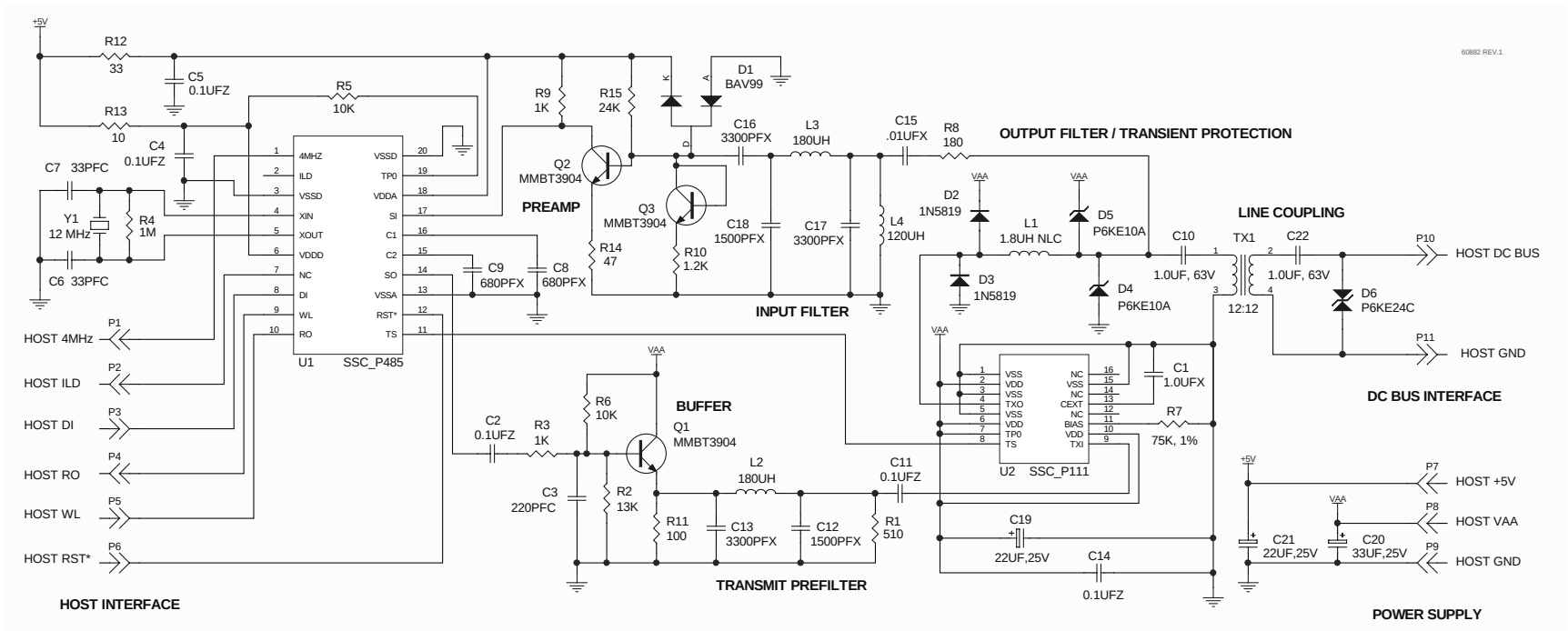


Figure 14. P485 Reference Application

SSC P485 Mechanical Specifications

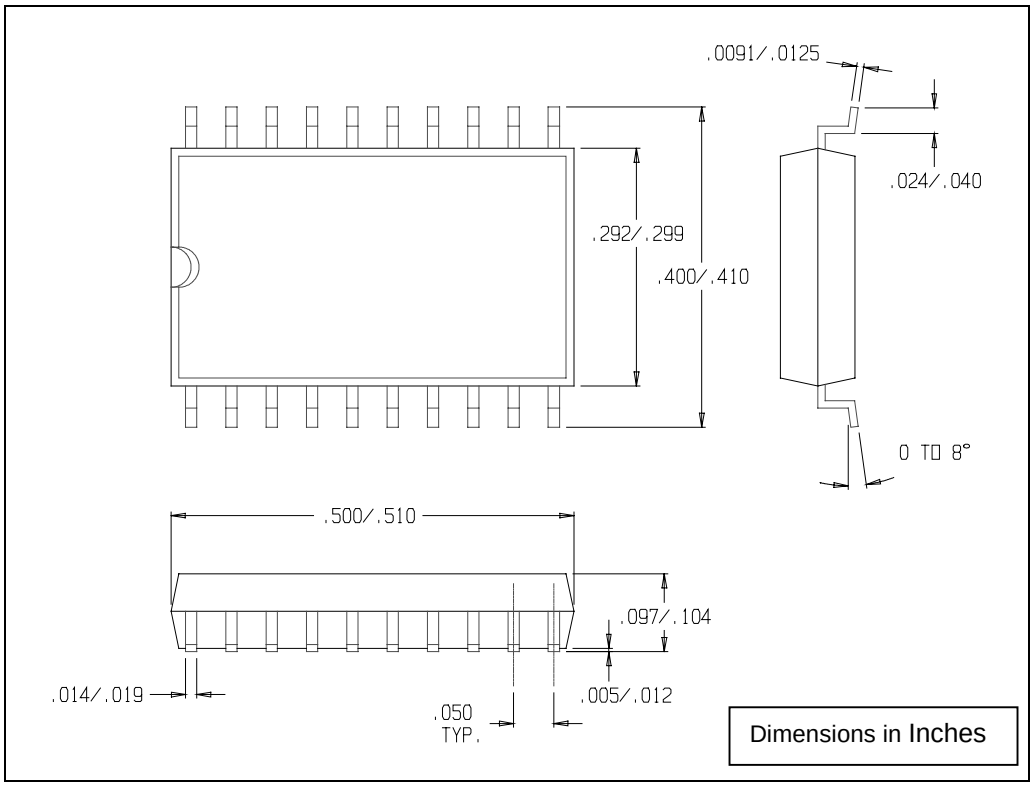


Figure 15. 20-Pin SOIC Package Outline

Ordering Information

SSC P485	PL Transceiver IC

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