

FEATURES

- Full CMOS
- High Speed (Equal Access and Cycle Times)
 - 12/15/20/25 ns (Commercial)
 - 12/15/20/25 ns (Industrial)
 - 25/35/45/55/70 ns (Military)
- Single 5V±10% Power Supply
- Data Retention with 2.0V Power Supply (P4C1257L)
- Separate Data I/O
- Three-State Output
- Fully TTL Compatible Inputs and Outputs
- Standard Pinout (JEDEC Approved)
 - 24-Pin 300 mil DIP, SOJ
 - 28-Pin 350x550 mil LCC
 - 28-Pin Flatpack



DESCRIPTION

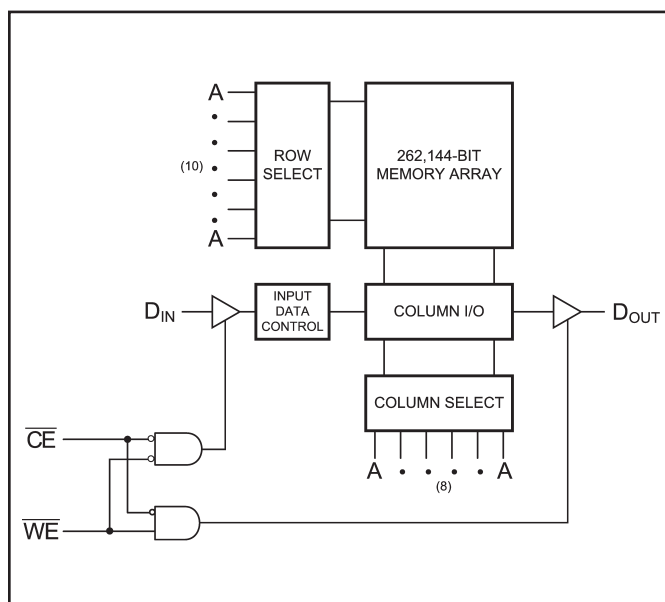
The P4C1257/P4C1257L are 256Kx1-bit ultra high-speed static RAMs. The CMOS memories require no clocks or refreshing and have equal access and cycle times. The RAMs operate from a single 5V ± 10% tolerance power supply. Data integrity is maintained for supply voltages down to 2.0V, typically drawing 10µA.

Access times as fast as 12 nanoseconds are available, greatly enhancing system speeds.

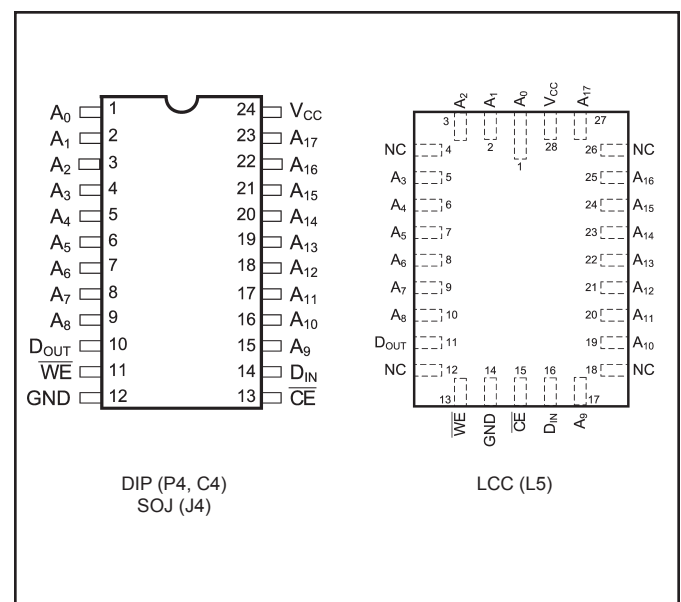
The P4C1257/P4C1257L are available in 24-pin 300 mil DIP and SOJ, 28-pin LCC and Flatpack packages, providing excellent board level densities.



FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS





MAXIMUM RATINGS⁽¹⁾

Sym	Parameter	Value	Unit
V _{CC}	Power Supply Pin with Respect to GND	-0.5 to +7	V
V _{TERM}	Terminal Voltage with Respect to GND (up to 7.0V)	-0.5 to V _{CC} + 0.5	V
T _A	Operating Temperature	-55 to +125	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-65 to +150	°C
P _T	Power Dissipation	1.0	W
I _{OUT}	DC Output Current	50	mA

RECOMMENDED OPERATING CONDITIONS

Grade ⁽²⁾	Ambient Temp	GND	V _{CC}
Commercial	0°C to 70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%
Military	-55°C to +125°C	0V	5.0V ± 10%

CAPACITANCES⁽⁴⁾

(V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz)

Sym	Parameter	Conditions	Typ	Unit
C _{IN}	Input Capacitance	V _{IN} =0V	8	pF
C _{OUT}	Output Capacitance	V _{OUT} =0V	10	pF

DC ELECTRICAL CHARACTERISTICS

(Over Recommended Operating Temperature & Supply Voltage)⁽²⁾

Sym	Parameter	Test Conditions	P4C1257		P4C1257L		Unit	
			Min	Max	Min	Max		
V _{IH}	Input High Voltage		2.2	V _{CC} + 0.5	2.2	V _{CC} + 0.5	V	
V _{IL}	Input Low Voltage		-0.5 ⁽³⁾	0.8	-0.5 ⁽³⁾	0.8	V	
V _{HC}	CMOS Input High Voltage		V _{CC} - 0.2	V _{CC} + 0.5	V _{CC} - 0.2	V _{CC} + 0.5	V	
V _{LC}	CMOS Input Low Voltage		-0.5 ⁽³⁾	0.2	-0.5 ⁽³⁾	0.2	V	
V _{CD}	Input Clamp Diode Voltage	V _{CC} = Min, I _{IN} = -18 mA		-1.2		-1.2	V	
V _{OL}	Output Low Voltage (TTL Load)	I _{OL} = +8 mA, V _{CC} = Min		0.4		0.4	V	
V _{OH}	Output High Voltage (TTL Load)	I _{OH} = -4 mA, V _{CC} = Min	2.4		2.4		V	
I _{LI}	Input Leakage Current	V _{CC} = Max, V _{IN} = GND to V _{CC}	MIL	-10	+10	-10	+10	µA
			IND/COM	-5	+5	-5	+5	
I _{LO}	Output Leakage Current	V _{CC} = Max, $\overline{CE} = V_{IH}$, V _{OUT} = GND to V _{CC}	MIL	-10	+10	-10	+10	µA
			IND/COM	-5	+5	-5	+5	
I _{CC}	Operating Supply Current	V _{CC} = Max, I _{OUT} = 0 mA, f = Max		95		85	mA	
I _{SB}	Standby Power Supply Current (TTL Input Levels)	$\overline{CE} \geq V_{IH}$, V _{CC} = Max, f = Max, Outputs Open	MIL	—	25	—	25	mA
			IND/COM	—	25	—	25	
I _{SB1}	Standby Power Supply Current (CMOS Input Levels)	$\overline{CE} \geq V_{HC}$, V _{CC} = Max, f = 0, Outputs Open V _{IN} ≤ V _{LC} or V _{IN} ≥ V _{HC}	MIL	—	20	—	3	mA
			IND/COM	—	10	—	3	

N/A = Not applicable

DATA RETENTION CHARACTERISTICS (P4C1257L)

Sym	Parameter	Test Conditions	Min	Typ* V _{CC} =		Max V _{CC} =		Unit
				2.0V	3.0V	2.0V	3.0V	
V _{DR}	V _{CC} for Data Retention		2.0					V
I _{CCDR}	Data Retention Current	$\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		10	15	600	900	μA
t _{CDR}	Chip Deselect to Data Retention Time		0					ns
t _R [†]	Operation Recovery Time		t _{RC} [§]					ns

* T_A = +25°C§ t_{RC} = Read Cycle Time

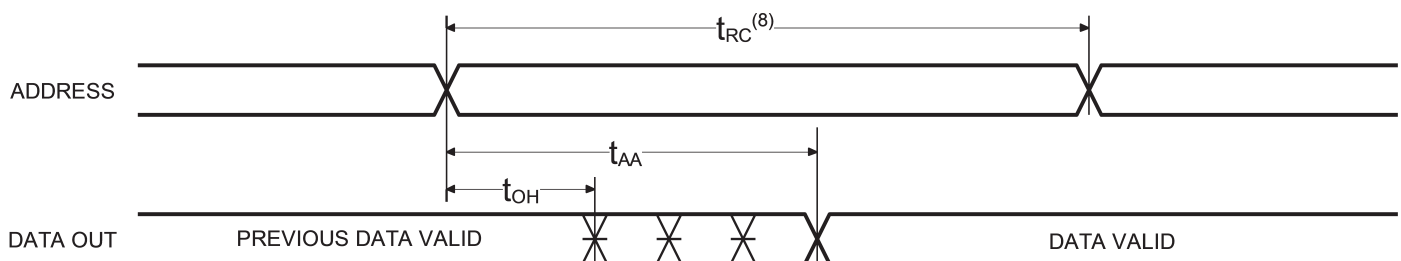
† This Parameter is guaranteed but not tested

AC ELECTRICAL CHARACTERISTICS—READ CYCLE

(V_{CC} = 5V ± 10%, All Temperature Ranges)⁽²⁾

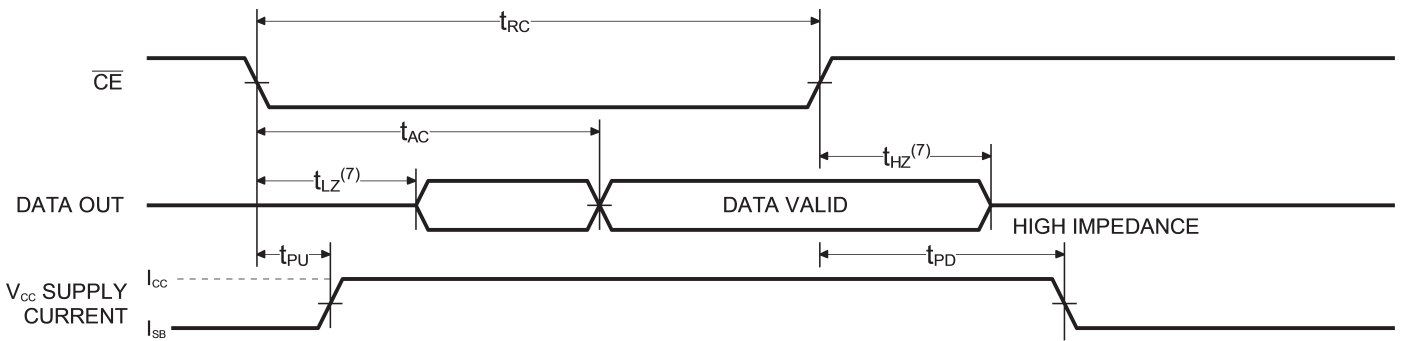
Sym	Parameter	-12		-15		-20		-25		-35		-45		-55		-70		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{RC}	Read Cycle Time	12		15		20		25		35		45		55		70		ns
t _{AA}	Address Access Time		12		15		20		25		35		45		55		70	ns
t _{AC}	Chip Enable Access Time		12		15		20		25		35		45		55		70	ns
t _{OH}	Output Hold from Address Change	2		2		2		2		2		2		2		2		ns
t _{LZ}	Chip Enable to Output in Low Z	2		2		2		2		2		2		2		2		ns
t _{HZ}	Chip Disable to Output in High Z		6		8		10		12		17		20		25		30	ns
t _{PU}	Chip Enable to Power Up Time	0		0		0		0		0		0		0		0		ns
t _{PD}	Chip Disable to Power Down		12		15		20		25		35		45		55		70	ns

TIMING WAVEFORM OF READ CYCLE NO. 1 (ADDRESS CONTROLLED)^(5,6)

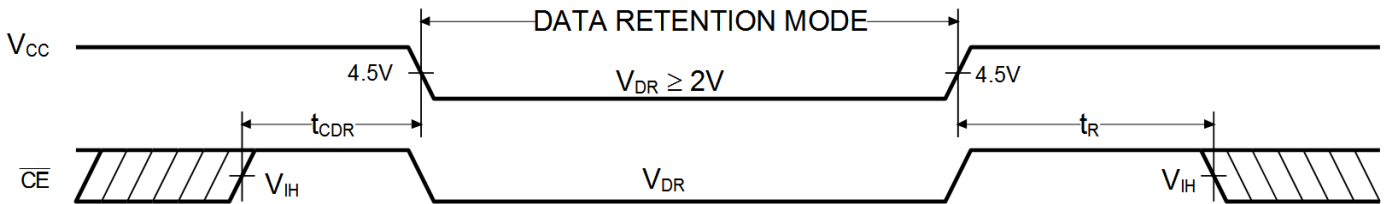




TIMING WAVEFORM OF READ CYCLE NO. 2 (\overline{CE} CONTROLLED)^(5,7,8)



DATA RETENTION WAVEFORM

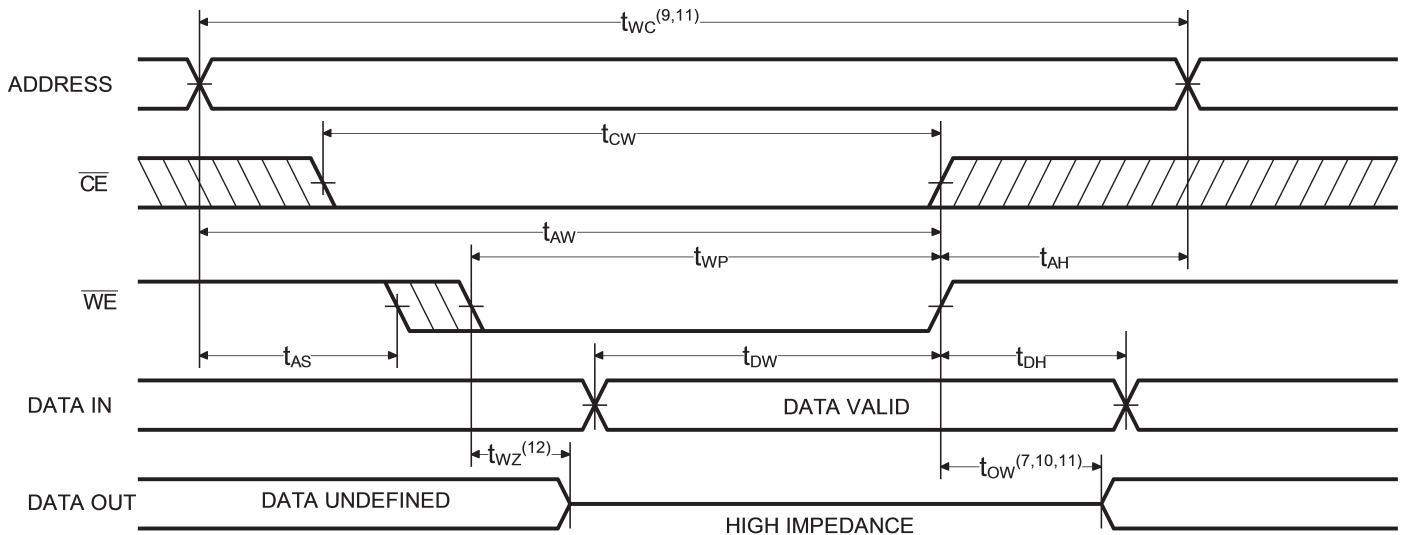


AC CHARACTERISTICS—WRITE CYCLE

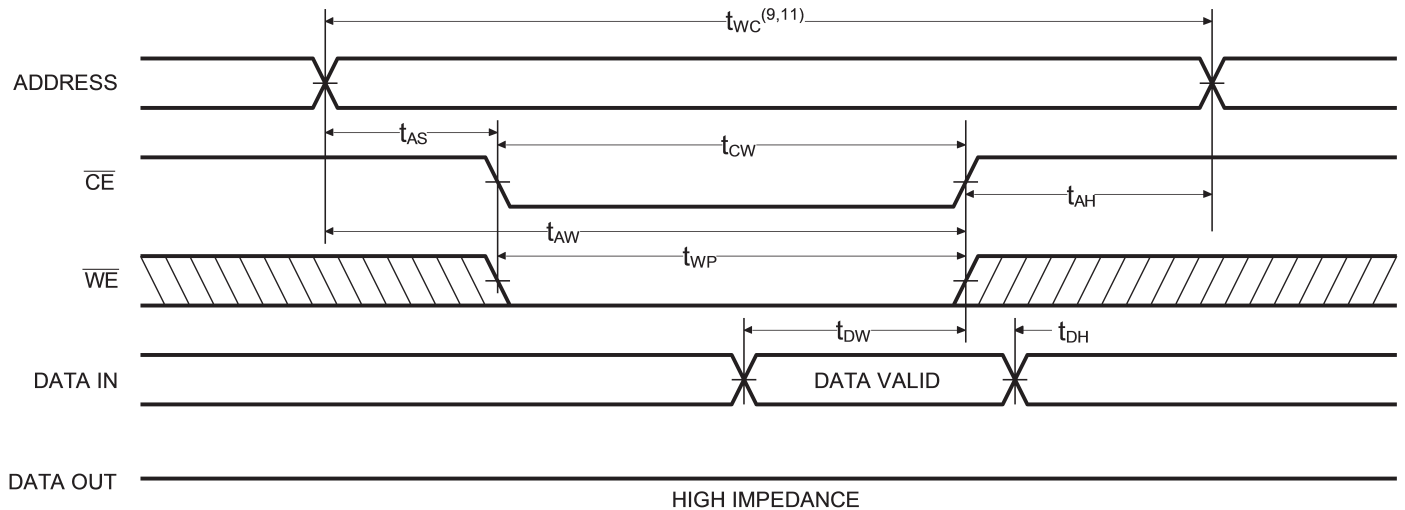
($V_{CC} = 5V \pm 10\%$, All Temperature Ranges)⁽²⁾

Sym	Parameter	-12		-15		-20		-25		-35		-45		-55		-70		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	8		10		12		15		20		25		35		45		ns
t_{CW}	Chip Enable Time to End of Write	7		8		10		12		15		18		25		30		ns
t_{AW}	Address Valid to End of Write	7		8		10		12		15		18		25		30		ns
t_{AS}	Address Setup Time	0		0		0		0		0		0		0		0		ns
t_{WP}	Write Pulse Width	7		8		10		12		15		18		20		25		ns
t_{AH}	Address Hold Time	0		0		0		0		0		0		0		0		ns
t_{DW}	Data Valid to End of Write	6		7		8		10		12		15		20		25		ns
t_{DH}	Data Hold Time	0		0		0		0		0		0		0		0		ns
t_{WZ}	Write Enable to Output in High Z		5		6		7		8		10		15		15		20	ns
t_{OW}	Output Active from End of Write	0		0		0		0		0		0		0		0		ns

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (\overline{WE} CONTROLLED)^(10,11)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 (\overline{CE} CONTROLLED)⁽¹⁰⁾



Notes:

- Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
- Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
- Transient inputs with V_{IL} and I_{IL} not more negative than $-3.0V$ and $-100mA$, respectively, are permissible for pulse widths up to 20ns.
- This parameter is sampled and not 100% tested.
- \overline{WE} is HIGH for READ cycle.
- \overline{CE} is LOW and \overline{OE} is LOW for READ cycle.
- ADDRESS must be valid prior to, or coincident with \overline{CE} transition LOW.
- Transition is measured ± 200 mV from steady state voltage prior to change, with loading as specified in Figure 1. This parameter is sampled and not 100% tested.
- Read Cycle Time is measured from the last valid address to the first transitioning address.



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1 and 2

TRUTH TABLE

Mode	\overline{CE}	\overline{WE}	I/O	Power
Standby	H	X	High Z	Standby
Read	L	H	D _{OUT}	Active
Write	L	L	High Z	Active

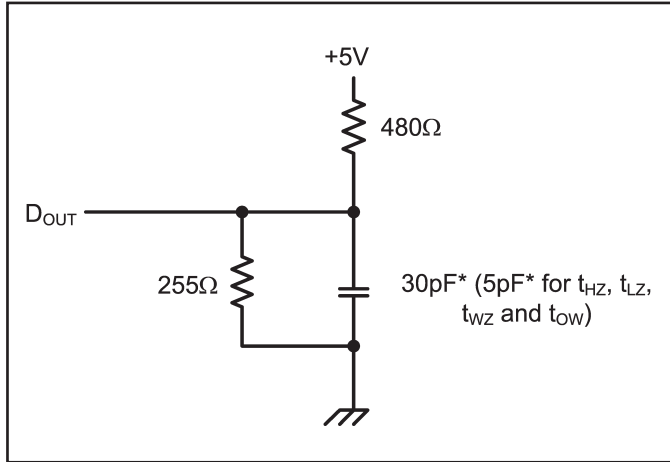


Figure 1. Output Load

* including scope and test fixture.

Note:

Because of the ultra-high speed of the P4C1257/P4C1257L, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 μF high frequency

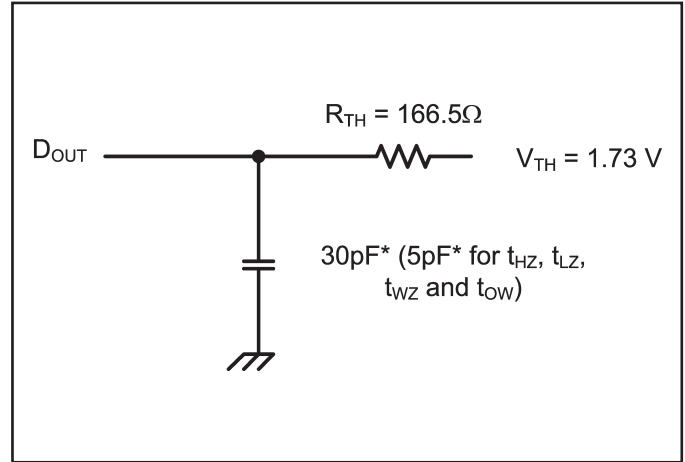


Figure 2. Thevenin Equivalent

capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with D_{OUT} to match 166Ω (Thevenin Resistance).

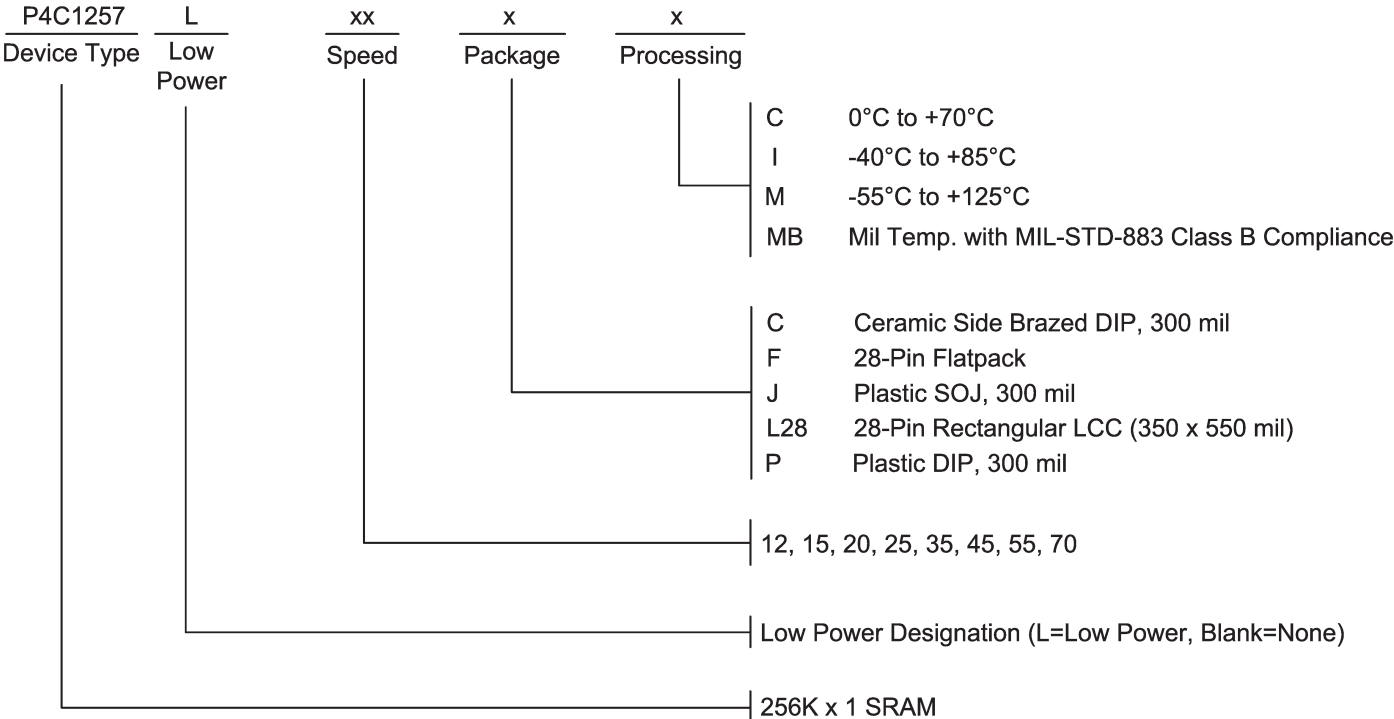
Notes:

- 10. \overline{CE} and \overline{WE} must be LOW for WRITE cycle.
- 11. \overline{OE} is LOW for this WRITE cycle to show t_{WZ} and t_{OW}.
- 12. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high impedance state

- 13. Write Cycle Time is measured from the last valid address to the first transitioning address.



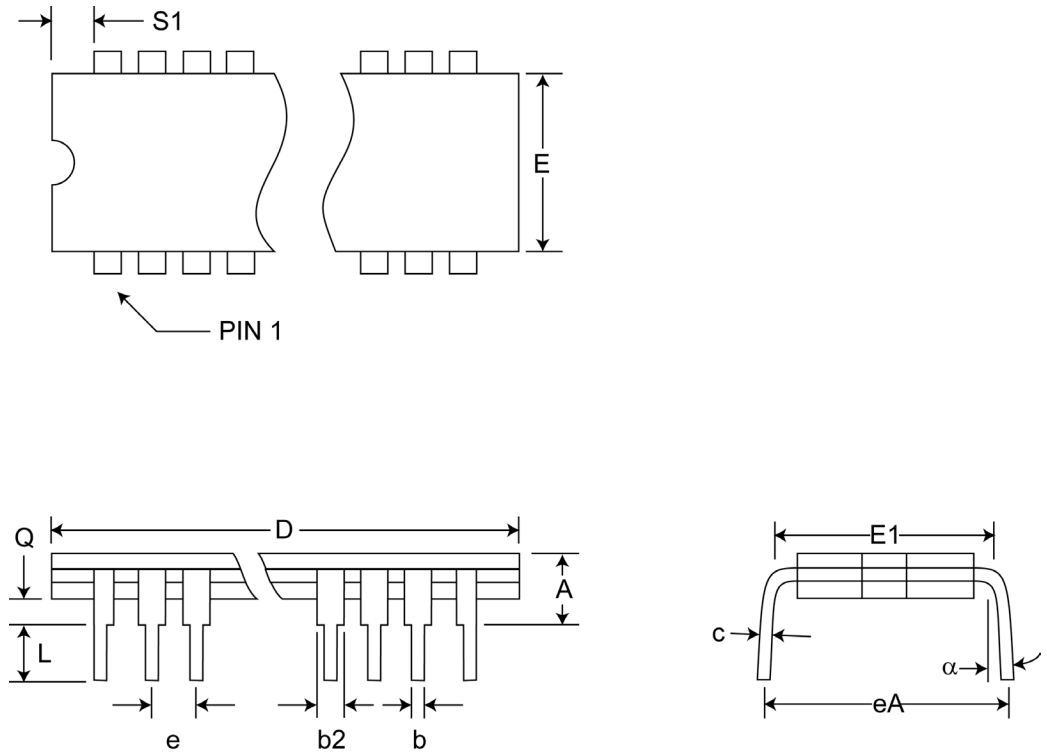
ORDERING INFORMATION





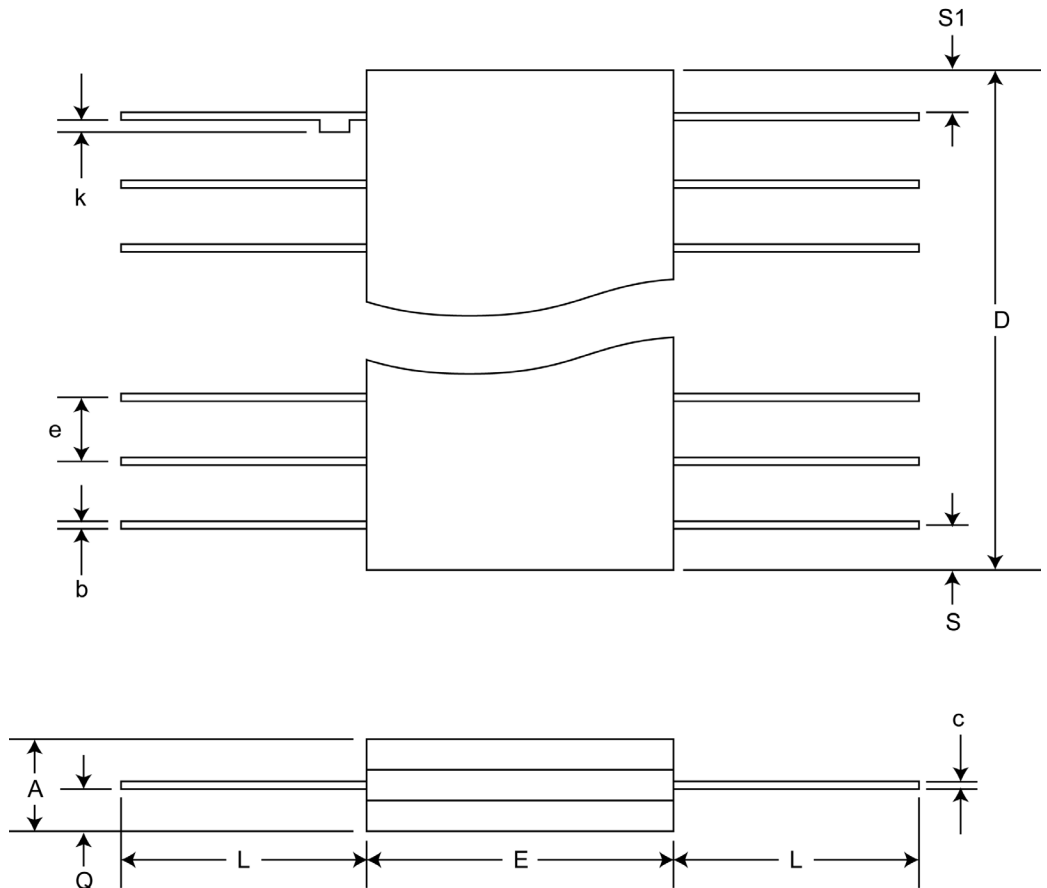
Pkg #	C4	
# Pins	24 (300 mil)	
Symbol	Min	Max
A	-	0.200
b	0.014	0.026
b2	0.045	0.065
C	0.008	0.018
D	-	1.280
E	0.220	0.310
eA	0.300 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.060
S1	0.005	-
S2	0.005	-

SIDEBRAZED DUAL IN-LINE PACKAGE



Pkg #	F4	
# Pins	28	
Symbol	Min	Max
A	0.060	0.090
b	0.015	0.022
c	0.004	0.009
D	-	0.730
E	0.330	0.380
e	0.050 BSC	
k	0.005	0.018
L	0.250	0.370
Q	0.026	0.045
S	-	0.085
S1	0.005	-

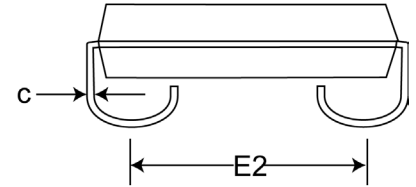
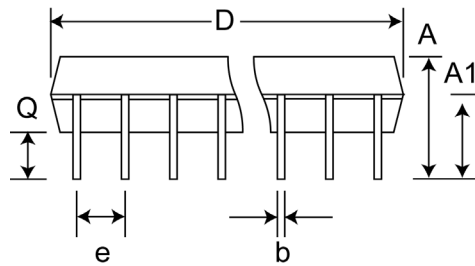
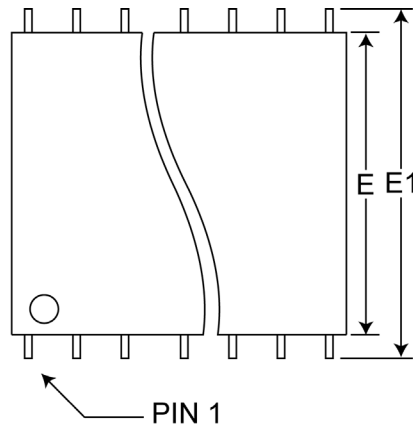
CERPACK CERAMIC FLAT PACKAGE





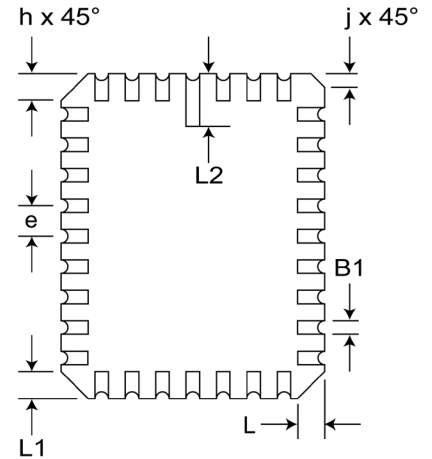
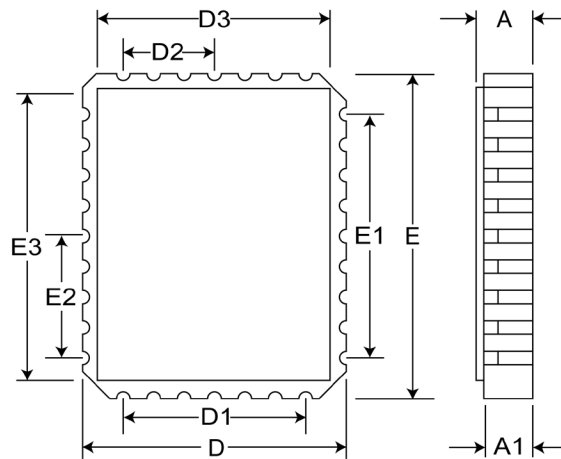
SOJ SMALL OUTLINE IC PACKAGE

Pkg #	J4	
# Pins	24 (300 mil)	
Symbol	Min	Max
A	0.128	0.148
A1	0.082	-
b	0.016	0.020
C	0.007	0.010
D	0.620	0.630
e	0.050 BSC	
E	0.335 BSC	
E1	0.292	0.300
E2	0.267 BSC	
Q	0.025	-



RECTANGULAR LEADLESS CHIP CARRIER

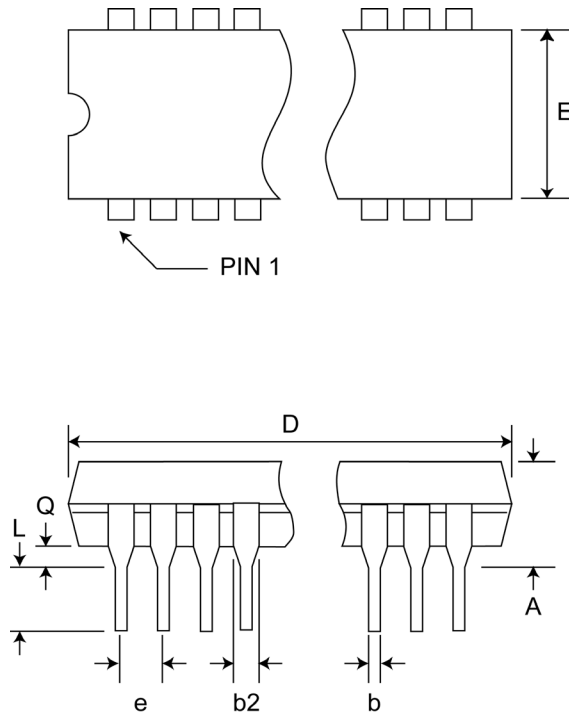
Pkg #	L5	
# Pins	28	
Symbol	Min	Max
A	0.060	0.075
A1	0.050	0.065
B1	0.022	0.028
D	0.342	0.358
D1	0.200 BSC	
D2	0.100 BSC	
D3	-	0.358
E	0.540	0.560
E1	0.400 BSC	
E2	0.200 BSC	
E3	-	0.558
e	0.050 BSC	
h	0.040 REF	
j	0.020 REF	
L	0.045	0.055
L1	0.045	0.055
L2	0.075	0.095
ND	5	
NE	9	





PLASTIC DUAL IN-LINE PACKAGE

Pkg #	P4	
# Pins	24 (300 Mil)	
Symbol	Min	Max
A	-	0.210
A1	0.015	-
b	0.014	0.022
b2	0.045	0.070
C	0.008	0.014
D	1.230	1.280
E1	0.240	0.280
E	0.280	0.325
e	0.100 BSC	
eB	-	0.430
L	0.115	0.160
α	0°	15°





REVISIONS

DOCUMENT NUMBER	SRAM137
DOCUMENT TITLE	P4C1257/P4C1257L - ULTRA HIGH SPEED 256K X 1 STATIC CMOS RAMS

REV	ISSUE DATE	ORIGINATOR	DESCRIPTION OF CHANGE
OR	Aug-2009	JDB	New Data Sheet
01	Jun-2013	JDB	