



5164SL

64K (8K x 8) CMOS SLOW STATIC RAM

■ Performance Range

| Symbol | Parameter | 5164SL-10 | Units |
|-----------|---------------------------|-----------|-------|
| t_{AA} | Address Access Time | 100 | ns |
| t_{ACS} | Chip Select Access Time | 100 | ns |
| t_{OE} | Output Enable Access Time | 55 | ns |

■ Static Operation

— No Clock/Refresh Required

■ Equal Access and Cycle Times

— Simplifies System Design

■ Single +5V Supply

■ Power Down Mode

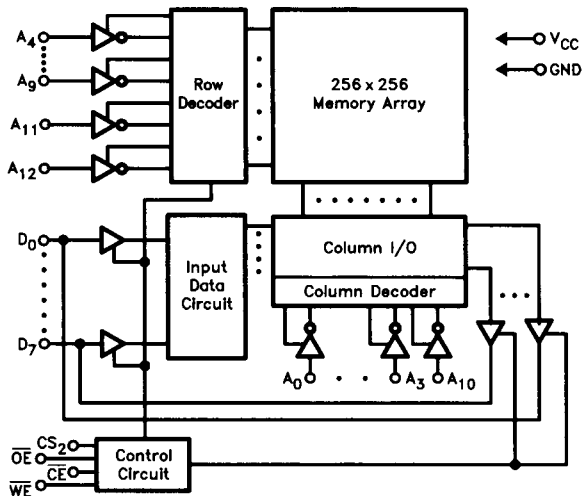
■ TTL Compatible

■ Common Data Input and Output

■ High Reliability 28-Pin 600 Mil PDIP (P) and 28-Pin SOP (PG) Package Types

Intel's 5164SL is a 8192-word by 8-bit CMOS static RAM fabricated using CMOS Silicon Gate process.

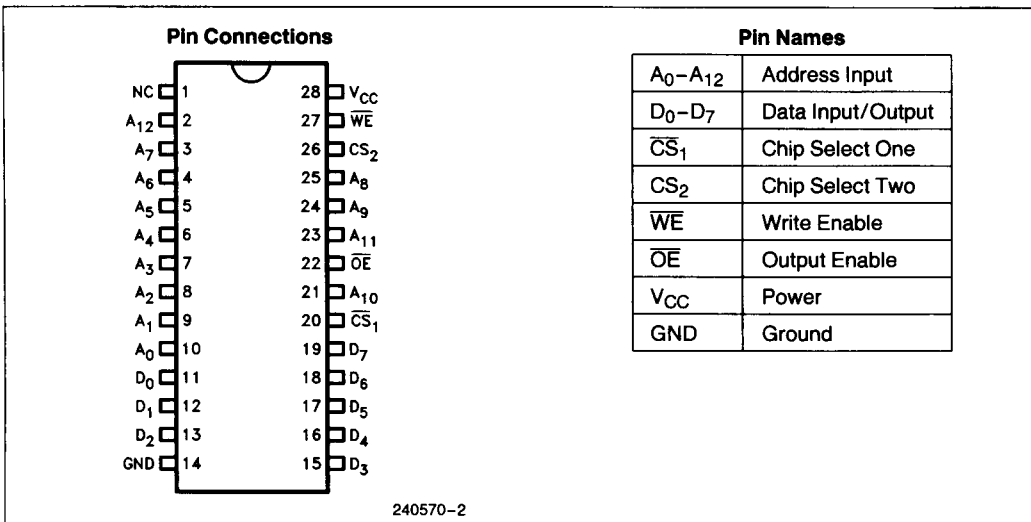
The 5164SL is placed in a standby or reduced power consumption mode by asserting either CS input (\overline{CS}_1 , \overline{CS}_2) false. When in standby mode, the device is deselected and the outputs are in a high impedance state, independent of the \overline{WE} input. When device is deselected, standby current is reduced to 2 μ A typ. @ 25°C. The device will remain in standby mode until both pins are asserted true again. The device has a data retention mode that guarantees that data will remain valid at minimum V_{CC} of 2.0V.



240570-1

Figure 1. Block Diagram

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Device Operation

The 5164SL has three control inputs: Two Chip Selects (\overline{CS}_1 , CS_2) and Write Enable (\overline{WE}). \overline{WE} is the data control pin and should be used to gate data at the I/O pins. A write cycle starts at the lowest transition of \overline{CS}_1 , low \overline{WE} or high CS_2 and ends at the

earliest transition of \overline{CS}_1 , high \overline{WE} or low CS_2 . Out Enable (OE) is used for precise control of the outputs.

The availability of active high and active low chip enable pins provides more system design flexibility than single chip enable devices.

Table 1. Mode Selection Truth Table

| \overline{CS}_1 | CS_2 | \overline{WE} | \overline{OE} | Mode | I/O | Power |
|-------------------|--------|-----------------|-----------------|---------|-----------|---------|
| H | X | X | X | Standby | High Z | Standby |
| X | L | X | X | Standby | High Z | Standby |
| L | H | L | X | Write | D_{IN} | Active |
| L | H | H | L | Read | D_{OUT} | Active |
| L | H | H | H | Read | High Z | Active |

ABSOLUTE MAXIMUM RATINGS

Voltage on Any Pin

Relative to Ground (V_{IN} , V_{OUT}) -0.3V to 7V

Storage Temperature (T_{STG}) -55°C to +150°C

Power Dissipation (P_D) 1.0W

DC Continuous Output Current (I_{OS}) 50 mA

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS

Voltage referenced to V_{SS} , $T_A = 0^\circ\text{C}$ to 70°C

| Symbol | Parameter | Min | Typ | Max | Units |
|----------|--------------------|------|-----|----------------|-------|
| V_{CC} | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| V_{SS} | Ground | 0 | 0 | 0 | V |
| V_{IH} | Input High Voltage | 2.2 | — | $V_{CC} + 0.3$ | V |
| V_{IL} | Input Low Voltage | -0.3 | — | 0.8 | V |

NOTE:

1. During transitions, the inputs may undershoot to -3.5V for periods less than 20 ns.

CAPACITANCE $T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$

| Symbol | Parameter | Min | Max | Units |
|-----------|---------------------------------------|-----|-----|-------|
| C_{IN1} | Input Capacitance ($V_{IN} = 0V$) | — | 6 | pF |
| C_{OUT} | Output Capacitance ($V_{OUT} = 0V$) | — | 8 | pF |

NOTE:

This parameter is sampled and not 100% tested.

DC AND OPERATING CHARACTERISTICS

Recommended Operating Conditions unless otherwise noted

| Symbol | Parameter | Min | Typ* | Max | Units | Test Conditions | |
|-----------|---------------------|-----|------|-----|---------------|--|---|
| I_{CC1} | Operating Current | — | 30 | 50 | mA | $\overline{CS1} = V_{IL}$, $CS2 = V_{IH}$ I/O Open, $V_{CC} = \text{Max}$ | |
| I_{CC2} | Dynamic Current | — | 40 | 70 | mA | $T_{CYC} = \text{Min}$, $V_{CC} = \text{Max}$ I/O Open | |
| I_{SB} | Standby Current | | 1 | 3 | mA | $\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$ | |
| I_{SB1} | | STD | | 0.2 | 2 | mA | $\overline{CS1} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} < 0.2V$ |
| | | L | — | 2 | 100 | μA | |
| I_{SB2} | | STD | | 0.2 | 2 | mA | $CS2 \leq V_{CC} - 0.2V$ |
| | L | — | 2 | 100 | μA | $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ | |
| I_{LI} | Input Load Current | -2 | — | 2 | μA | $V_{CC} = \text{Max}$ $V_{IN} = \text{GND to } V_{CC}$ | |
| I_{LO} | Output Leakage | -2 | — | 2 | μA | $\overline{CS1} = V_{IH}$, $CS2 = V_{IL}$ $V_{OUT} = \text{Ground to } V_{CC}$ | |
| V_{OH} | Output High Voltage | 2.4 | — | — | V | $I_{OH} = -1.0\text{ mA}$ | |
| V_{OL} | Output Low Voltage | — | — | 0.4 | V | $I_{OL} = 2.1\text{ mA}$ | |

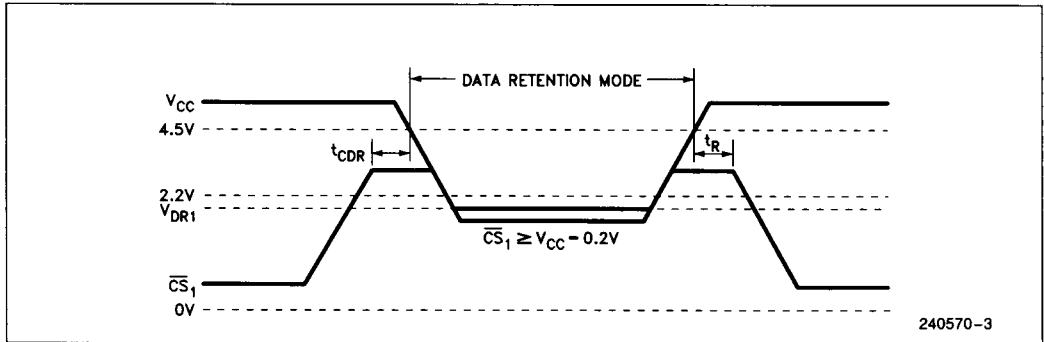
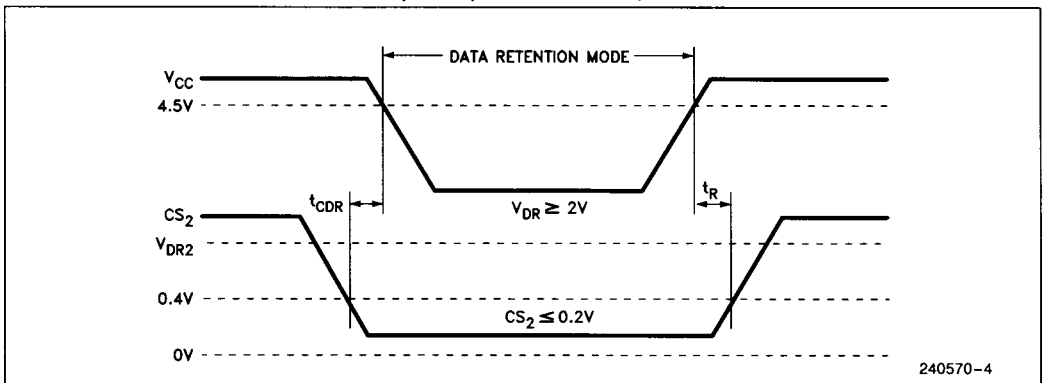
*Typ: $V_{CC} = 5V$, $T_A = 25^\circ\text{C}$

DATA RETENTION ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Min | Typ | Max | Units | Test Conditions |
|-------------------|--------------------------------------|-------------------|-----|-----|---------------|---|
| V_{CDR} | Voltage for Data Retention | 2 | | — | V | |
| I_{CCDR} | Data Retention Current | | 2 | 50 | μA | $\overline{\text{CS}}_1 \geq V_{\text{CC}} - 0.2\text{V}$, $V_{\text{CC}} = 3\text{V}$ $V_{\text{IN}} \geq V_{\text{CC}} - 0.2\text{V}$ or $V_{\text{IN}} \leq 0.2\text{V}$ |
| | | | 2 | 50 | μA | $\text{CS}_2 \leq 0.2\text{V}$, $V_{\text{CC}} = 3\text{V}$ $V_{\text{IN}} \geq V_{\text{CC}} - 0.2\text{V}$ or $V_{\text{IN}} \leq 0.2\text{V}$ |
| t_{CDR} | Chip Deselect to Data Retention Time | 0 | — | — | ns | |
| t_{R} | Operation Recovery Time | t_{RC}^* | — | — | ns | |

NOTES:

- * t_{RC} = Read Cycle Time
- Typ: $V_{\text{CC}} = 3\text{V}$, $T_{\text{A}} = 25^\circ\text{C}$

DATA RETENTION WAVEFORM (No. 1) ($\overline{\text{CS}}_1$ Controlled)

DATA RETENTION WAVEFORM (No. 2) (CS_2 Controlled)


AC TEST CONDITIONS

Input Pulse Levels 0.8V to 2.4V

Input Rise and Fall Times 5 ns

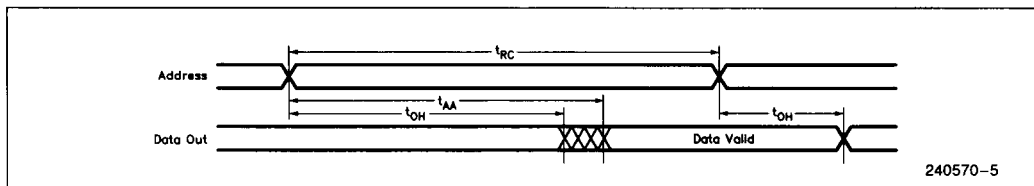
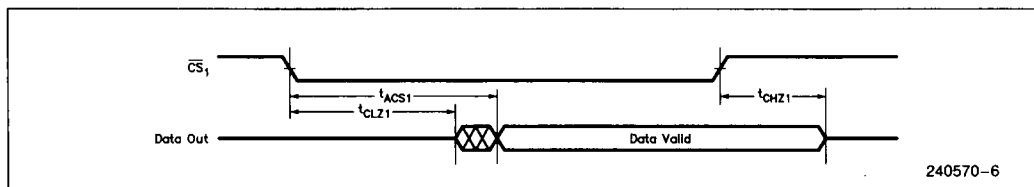
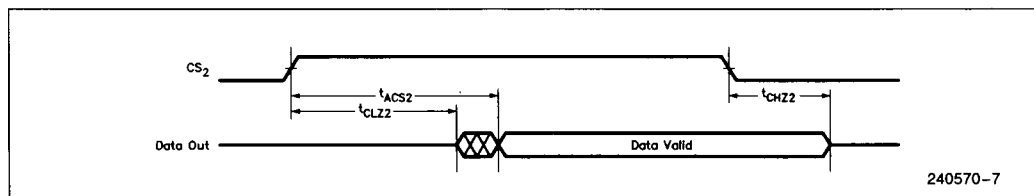
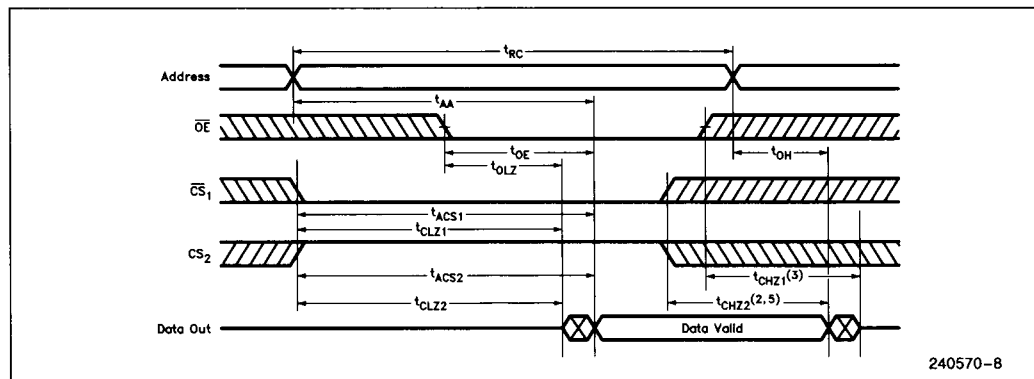
Timing Reference Level 1.5V

Output Load 1 TTL Load + 100 pF

AC CHARACTERISTICS (READ CYCLE) $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 10\%$ **READ CYCLE**

| Symbol | Parameter | 5164SL-10 | | Units |
|-----------|---------------------------------------|-----------|-----|-------|
| | | Min | Max | |
| t_{RC} | READ Cycle Time | 100 | | ns |
| t_{AA} | Address Access Time | | 100 | ns |
| t_{ACS} | Chip Select Access Time* | | 100 | ns |
| t_{OH} | Output Hold from Address Change | 10 | | ns |
| t_{CLZ} | Chip Selection to Output in Low Z* | 10 | | ns |
| t_{CHZ} | Chip Deselection to Output in High Z* | 0 | 35 | ns |
| t_{OE} | Output Enable Access Time | 55 | | ns |
| t_{OLZ} | Output Enable to Output in Low Z | 5 | | ns |
| t_{OHZ} | Output Disable to Output in High Z | 0 | 35 | ns |

*Timing parameters referenced to both $\overline{CS1}$ and CS2.

TIMING DIAGRAMS (READ CYCLE)
READ CYCLE 1(1, 2, 4)

READ CYCLE 2(1, 3, 4, 6)

READ CYCLE 3(1, 4, 7)

READ CYCLE 4(1)

NOTES:

1. \overline{WE} is high for READ cycle.
2. Device is continuously selected $\overline{CS1} = V_{IL}$ and $CS2 = V_{IH}$.
3. Address valid prior to or coincident with $\overline{CS1}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured ± 500 mV from steady state. This parameter is sampled and not 100% tested.
6. $CS2$ is high.
7. $\overline{CS1}$ is low.

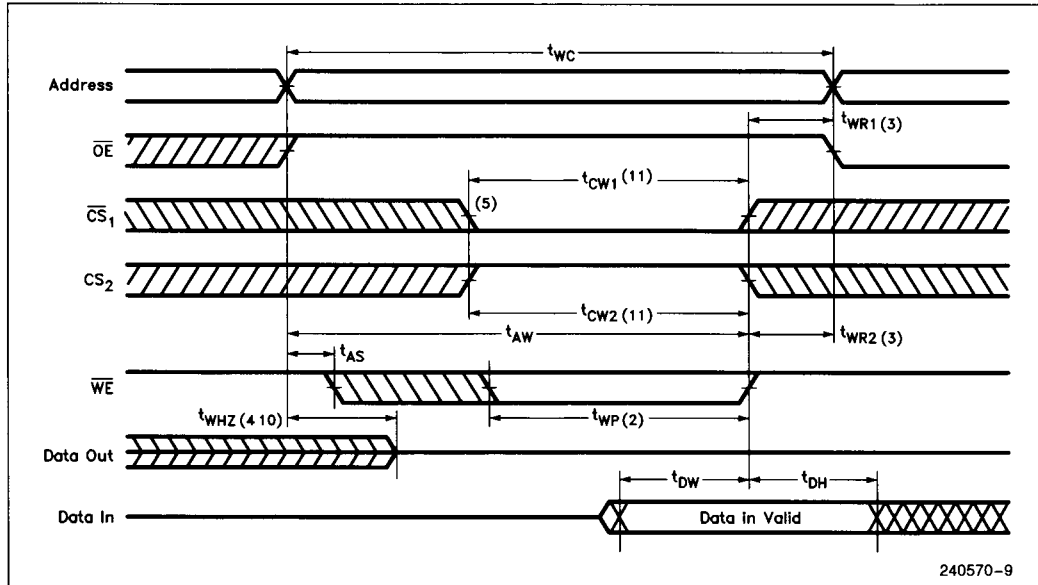
AC CHARACTERISTICS (WRITE CYCLE)

WRITE CYCLE

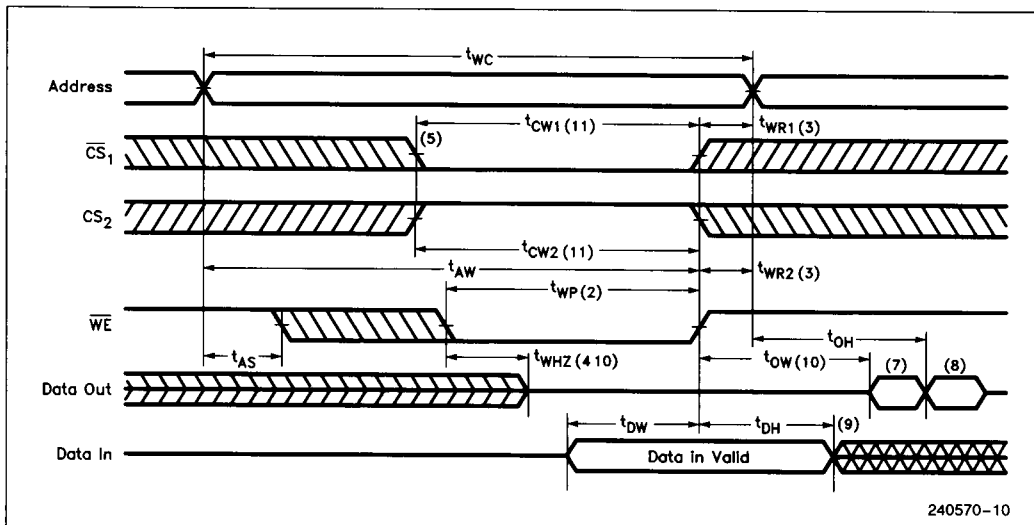
| Symbol | Parameter | 5164SL-10 | | Units |
|-----------|------------------------------------|-----------|-----|-------|
| | | Min | Max | |
| t_{WC} | Write Cycle Time | 100 | | ns |
| t_{CW} | Chip Selection to End of Write | 70 | | ns |
| t_{AW} | Address Valid to End of Write | 80 | | ns |
| t_{AS} | Address Set-Up Time | 0 | | ns |
| t_{WP} | Write Pulse Width | 60 | | ns |
| t_{WR} | Write Recovery Time | 15 | | ns |
| t_{DW} | Data Valid to End of Write | 40 | | ns |
| t_{DH} | Data Hold Time | 15 | | ns |
| t_{WHZ} | Write Enable to Output in High Z | 0 | 35 | ns |
| t_{OW} | Output Active from End of Write | 10 | | ns |
| t_{OHZ} | Output Disable to Output in High Z | 0 | 35 | ns |

TIMING DIAGRAMS (WRITE CYCLE)

WRITE CYCLE 1(1)



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TIMING DIAGRAMS (WRITE CYCLE) (Continued)
WRITE CYCLE 2(1, 6)

NOTES:

1. \overline{WE} must be high during address transitions.
2. A write occurs during the overlap (t_{WP}) of a low \overline{CS} , a high CS , and a low \overline{WE} .
3. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going high or CS going low to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the \overline{CS} low transition or the CS high transition occurs simultaneously with the \overline{WE} low transitions or after the \overline{WE} transition, outputs remain in a high impedance state.
6. \overline{OE} is continuously low ($\overline{OE} = V_{IL}$)
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If \overline{CS} is low and CS is high during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ± 500 mV from steady state. This parameter is sampled and not 100% tested.
11. t_{OW} is measured from the later of \overline{CS} going low or CS going high to the end of write.

PACKAGE OUTLINES

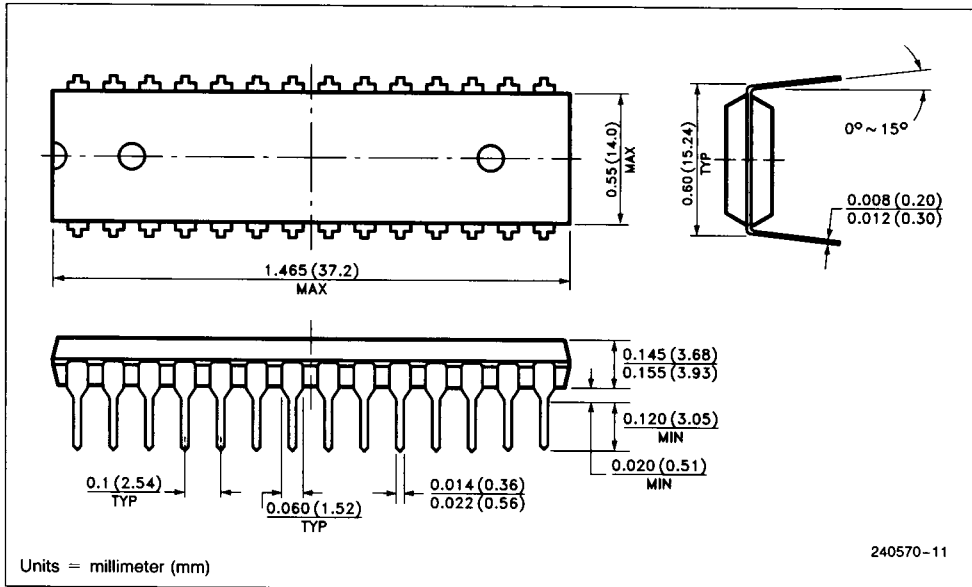


Figure 2. 28-Lead Plastic Dual In-Line Package

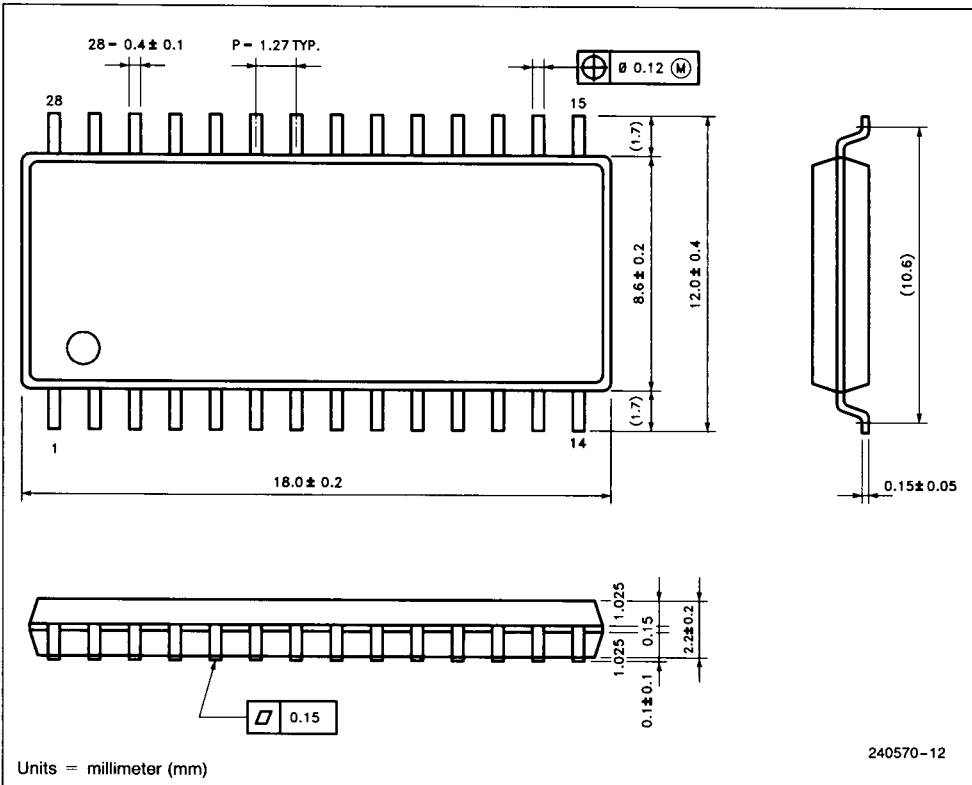


Figure 3. 28-Lead Small Out-Line Package (PG)