

General Description

These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

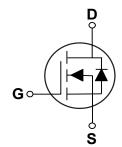
BV _{DSS}	R _{DS(ON)}	I _D
65 V	4.4 mΩ	95 A

Features

- $R_{DS(ON)} \leq \overline{4.4m\Omega} \overline{@V_{GS}} = \overline{10V}$
- · Fast switching
- · Improved dv/dt capability
- · Green Device Available

PPAK5X6 Pin Configuration





Applications

- Networking
- · Load Switch
- LED applications

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	65	V
V_{GS}	Gate-Source Voltage	±20	V
ı	Drain Current – Continuous (T _C =25°C)	95	Α
I _D	Drain Current – Continuous (T _C =100°C)	60	Α
I _{DM}	Drain Current – Pulsed (NOTE 1)	380	Α
EAS	Single Pulse Avalanche Energy (NOTE 2)	151.3	mJ
IAS	Single Pulse Avalanche Current (NOTE 2)	55	Α
P_{D}	Power Dissipation (T _C =25°C)	96	W
гр	Power Dissipation – Derate above 25°C	0.77	W/°
T_J	Storage Temperature Range	-50 to 150	°C
T _{STG}	Operating Junction Temperature Range	-50 to 150	°C
Marking Code		NG4P4	

Thermal Characteristics					
Symbol	Parameter	Тур.	Max.	Unit	
$R_{\theta JA}$	Thermal Resistance Junction to Ambient		62	°C/W	
$R_{\theta JC}$	Thermal Resistance Junction to Case		1.3	°C/W	





Electrical Characteristics (T_{.1}=25°C, unless otherwise noted)

Off Characteristics

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V_{GS} =0V , I_D =250uA	65			V
I _{DSS} Drain-Soul	Drain-Source Leakage Current	V_{DS} =60V , V_{GS} =0V , T_J =25°C			1	uA
	Dialii-Source Leakage Guireili	V_{DS} =48V , V_{GS} =0V , T_{J} =85 $^{\circ}$ C			10	uA
I_{GSS}	Gate-Source Leakage Current	V_{GS} =±20V , V_{DS} =0V			±100	nA

On Characteristics

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
R _{DS(ON)}	IStatic Drain-Source On-Resistance	V_{GS} =10V , I_D =20A		3.7	4.4	mΩ
		V _{GS} =4.5V , I _D =15A		5.8	7.5	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=250uA$	1.0	1.6	2.5	V
gfs	Forward Transconductance	V_{DS} =10V , I_{D} =3A		10		S

Dynamic and switching Characteristics

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
Q_g	Total Gate Charge	V _{DS} =48V , V _{GS} =10V , I _D =30A		36	54	
Q_gs	Gate-Source Charge	V_{DS} -46V, V_{GS} -10V, I_{D} -30A (NOTE 3 \ 4)		4.7	7.1	nC
Q_{gd}	Gate-Drain Charge	(NOTE 3 * 4)		13.5	20	ļ
$T_{d(on)}$	Turn-On Delay Time	V_{DD} =48V , V_{GS} =10V , R_{G} =6 Ω , I_{D} =1A (NOTE 3 \cdot 4)		10.2	15	
T _r	Rise Time			16	24	nS
$T_{d(off)}$	Turn-Off Delay Time			42	63	113
T_f	Fall Time			38	57	
C _{iss}	Input Capacitance	V _{DS} =48V , V _{GS} =0V , F=1MHz		1675	2510	
C _{oss}	Output Capacitance			322	485	pF
C _{rss}	Reverse Transfer Capacitance			14	25	
R_g	Gate resistance	V _{GS} =0V , V _{DS} =0V , F=1MHz		1.2		Ω

Drain-Source Diode Characteristics and Ratings

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
Is	Continuous Source Current	V _G =V _D =0V,Force Current			95	Α
I _{SM}	Pulsed Source Current	V _G -V _D -0V, Force Current			190	Α
V_{SD}	Diode Forward Voltage	V_{GS} =0V , I_{S} =1A , T_{J} =25 $^{\circ}$ C			1	V
t _{rr}	Reverse Recovery Time (NOTE 3)	V _R =50V , I _S =10A ,		54		nS
Q_{rr}	Reverse Recovery Charge (NOTE 3)	di/dt=100A/us , T _J =25°C		67		nC

NOTES:

- 1. Repetitive Rating: Pulsed width limited by maximum junction temperature.
- 2. V_{DD} =25V, V_{GS} =10V, L=0.1mH, I_{AS} =55A, R_{G} =25 Ω , Starting T_{J} =25 $^{\circ}$ C.
- 3. The data tested by pulsed , pulse width \leq 300us , duty cycle \leq 2%.
- 4. Essentially independent of operating temperature.





Characteristics Curves

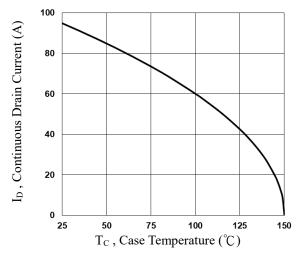


Fig.1 Continuous Drain Current vs. Tc

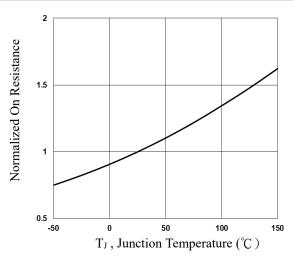


Fig.2 Normalized RDSON vs. TJ

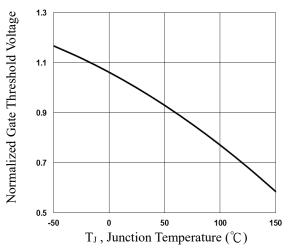


Fig.3 Normalized Vth vs. T_J

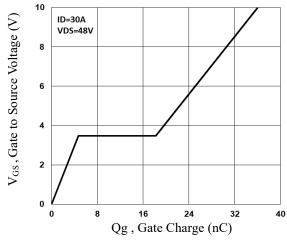


Fig.4 Gate Charge Characteristics

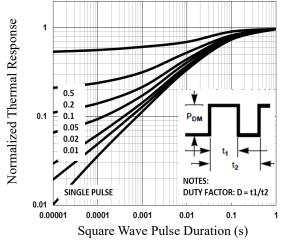


Fig.5 Normalized Transient Impedance

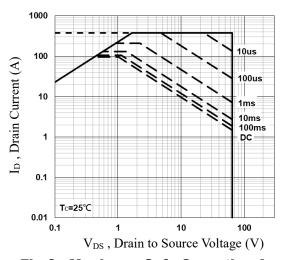
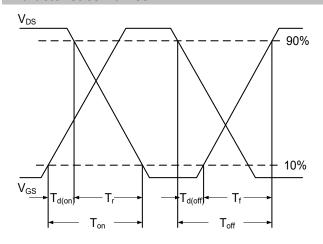


Fig.6 Maximum Safe Operation Area





Characteristics Curves



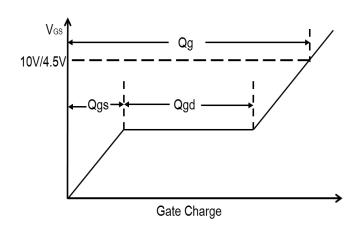
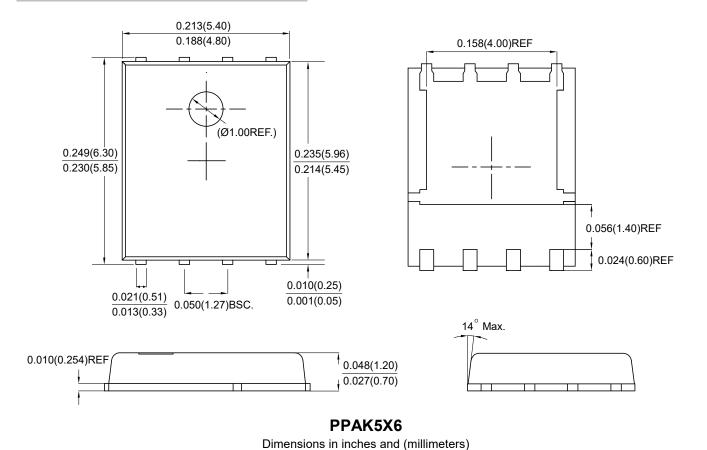


Fig.7 Switching Time Waveform

Fig.8 Gate Charge Waveform

Package Outline Dimensions







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