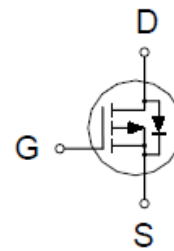
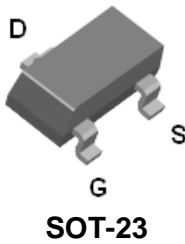


P6402FMG

P-Channel Logic Level Enhancement Mode MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
-20V	64mΩ @ $V_{GS} = -4.5V$	-4A



ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ °C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	±12	
Continuous Drain Current	$T_A = 25\text{ °C}$	I_D	-4	A
	$T_A = 70\text{ °C}$		-3	
Pulsed Drain Current ¹		I_{DM}	-20	
Power Dissipation	$T_A = 25\text{ °C}$	P_D	1.25	W
	$T_A = 70\text{ °C}$		0.8	
Operating Junction & Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient	$R_{\theta JA}$	75	100	°C / W
Junction-to-Case	$R_{\theta JC}$		60	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

P6402FMG

P-Channel Logic Level Enhancement Mode MOSFET

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250μA	-20			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	-0.45	-0.8	-1.2	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±12V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -16V, V _{GS} = 0V			-1	μA
		V _{DS} = -16V, V _{GS} = 0V, T _J = 125 °C			-10	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = -5V, V _{GS} = -4.5V	-20			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = -1.8V, I _D = -2A		90	120	mΩ
		V _{GS} = -2.5V, I _D = -3A		62	79	
		V _{GS} = -4.5V, I _D = -4A		55	64	
Forward Transconductance ¹	g _{fs}	V _{DS} = -5V, I _D = -4A		12		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = -15V, f = 1MHz		950		pF
Output Capacitance	C _{oss}			115		
Reverse Transfer Capacitance	C _{rss}			75		
Total Gate Charge ²	Q _g	V _{DS} = 0.5V _{(BR)DSS} , V _{GS} = -4.5V, I _D = -4A		9.4		nC
Gate-Source Charge ²	Q _{gs}			2		
Gate-Drain Charge ²	Q _{gd}			3		
Turn-On Delay Time ²	t _{d(on)}	V _{DD} = -10V I _D ≅ -1A, V _{GS} = -4.5V, R _G = 6Ω		6.3		nS
Rise Time ²	t _r			3.2		
Turn-Off Delay Time ²	t _{d(off)}			38		
Fall Time ²	t _f			12		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICE (T_C = 25 °C)						
Continuous Current	I _S				-1	A
Forward Voltage ¹	V _{SD}	I _F = I _S , V _{GS} = 0V			-1.2	V

¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

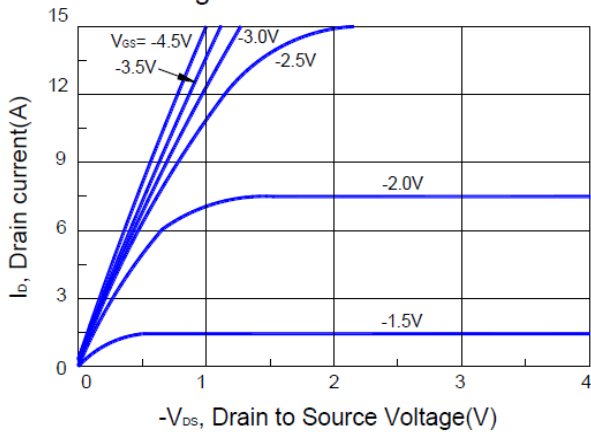
²Independent of operating temperature.

P6402FMG

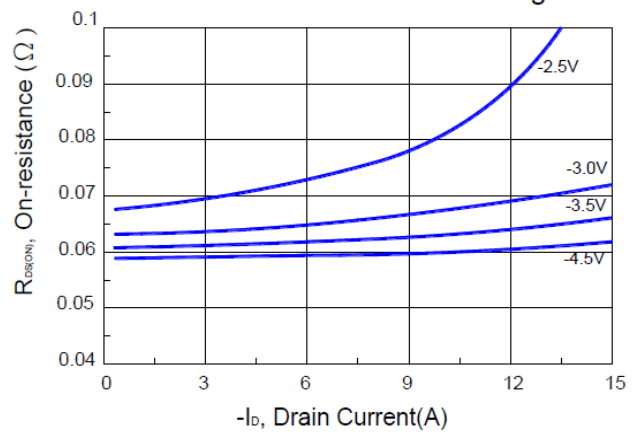
P-Channel Logic Level Enhancement Mode MOSFET

Typical Electrical Characteristics

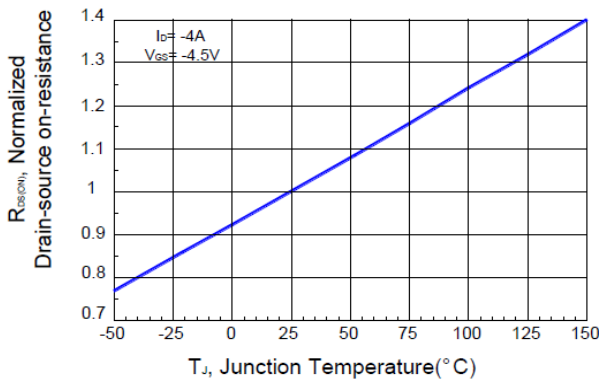
On-Region Characteristics.



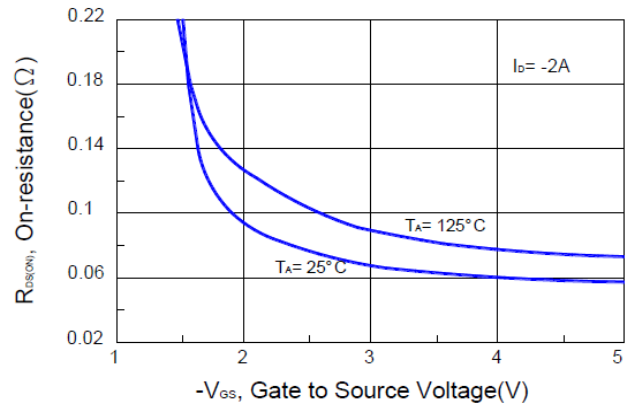
On-Resistance Variation with Drain Current and Gate Voltage.



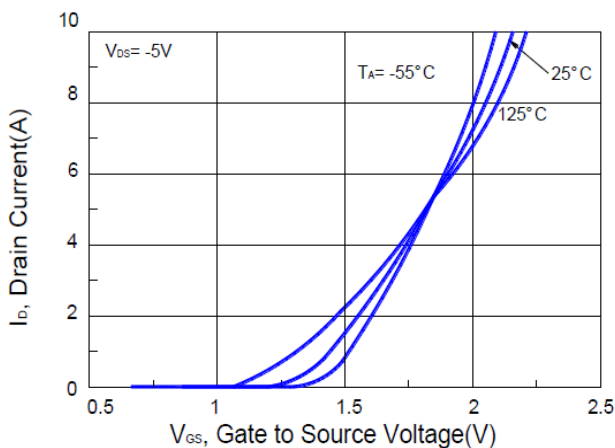
On-Resistance Variation with Temperature.



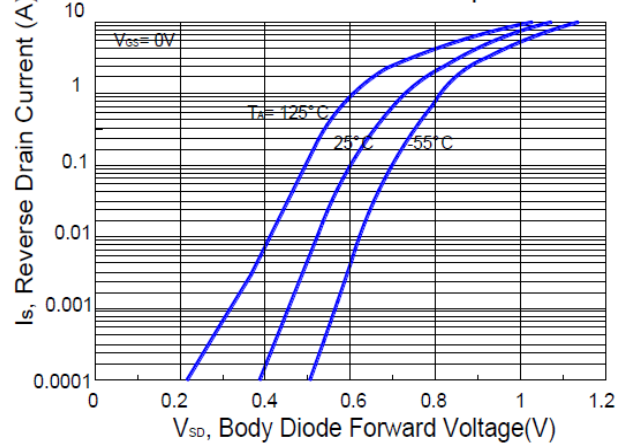
On-Resistance Variation with Gate-to-Source Voltage.



Transfer Characteristics.



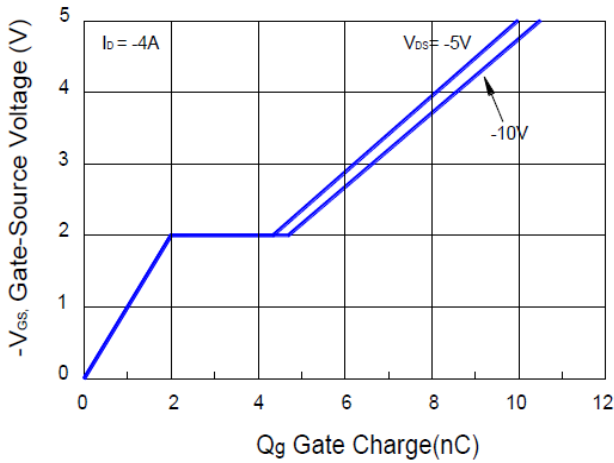
Body Diode Forward Voltage Variation with Source Current and Temperature.



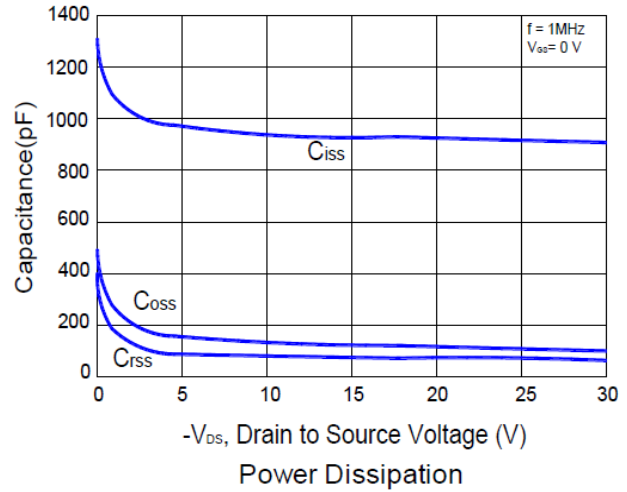
P6402FMG

P-Channel Logic Level Enhancement Mode MOSFET

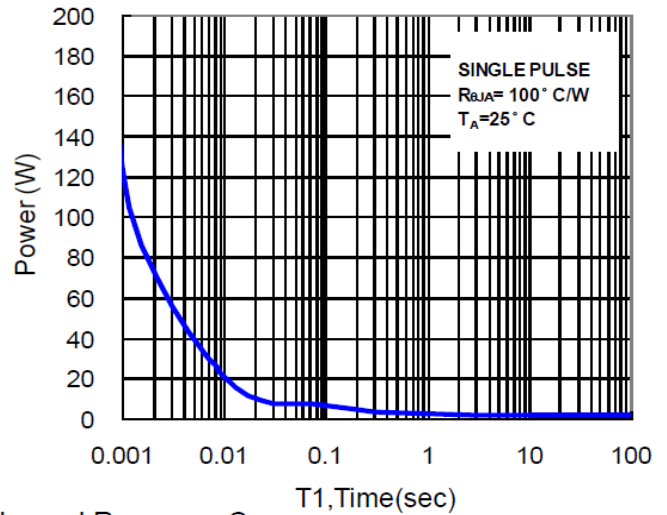
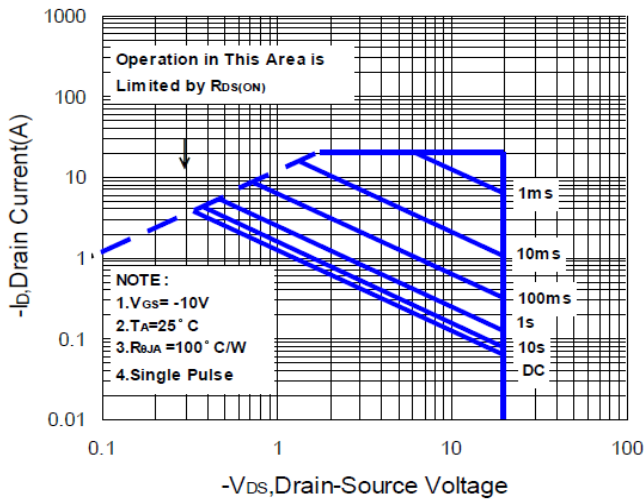
Gate-Charge Characteristics



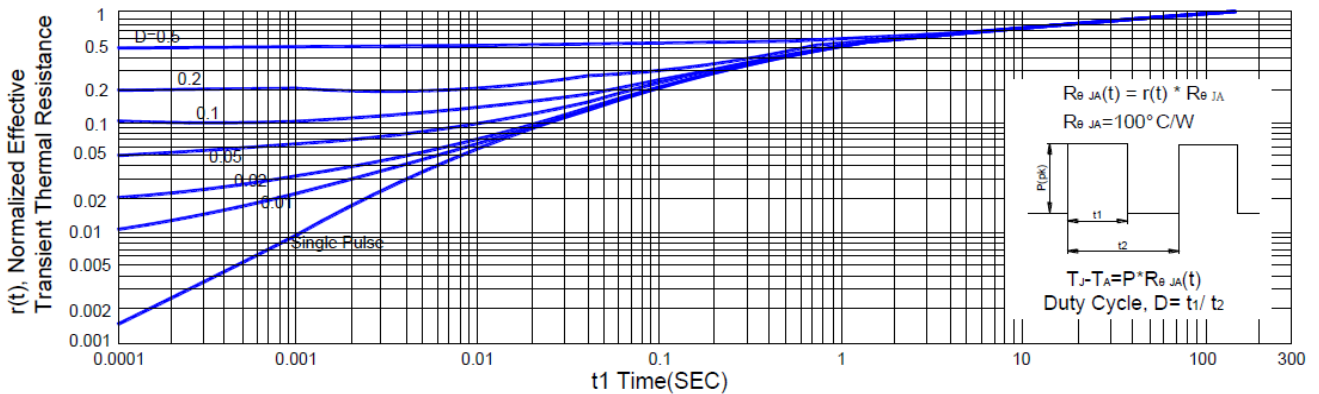
Capacitance Characteristics



Safe Operating Area



Transient Thermal Response Curve.



P6402FMG

P-Channel Logic Level Enhancement Mode MOSFET

Package Dimension

SOT-23 MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A		1.05		H	0.1		0.2
B	2.4		3	I	0.3		0.6
C	1.4		1.73				
D	2.7		3.1				
E	1		1.31				
F	0		0.15				
G	0.3		0.5				

