Embedded MCP specification

P6408T2B5X2

Datasheet Preliminary Ver 1.0

Apollo Memory System Company

<Product Specification>

-Compatible Approved Vendor List-

Chipset AVL	Chipset Model	eMCP PN
Mediatek	MT6582	08EMCP08-EL2BV100

Note 1: compatible AVL updated by 2014,Q4

-Device Summary-:

Table 1 – Device Summary

Product Part number	NAND	DRAM	CH & CS For DRAM	Operating voltage
P6408T2B5X2	8GB	8Gb	1CH, 2CS	VCC=3.3V VCCQ=1.8V/3.3V VDD1 = 1.8V VDD2, VDDQ = 1.2V

-System Performance-

Table 2 – *e*•MMC™ Device Performance

	Typical value	
	Read Sequential (MB/s)	Write Sequential (MB/s)
P6408T2B5X2	70	4

Note 1: Values given for an 8-bit bus width, running HS200 mode from proprietary tool, VCC=3.3V, VCCQ=1.8V.
Note 2: Performance numbers might be subject to changes without notice.

< Embedded MMC™ - NAND>

- Packaged NAND flash memory with *e*•MMC™ 5.0 interface
- Compliant with *e*•MMC™ Specification Ver.4.4, 4.41,4.5&5.0
- Supports three different data bus widths : 1 bit(default), 4 bits, 8 bits
  - Data transfer rate: up to 52Mbyte/s (using 8 parallel data lines at 52 MHz)
  - Single data rate : up to 200Mbyte/s @ HS200(Host clock @ 200MHz)
  - Dual data rate : up to 104Mbyte/s @ 52MHz
- Enhanced Write Protection with Permanent and Partial protection options
- Supports Multiple User Data Partition with Enhanced User Data Area options
- Supports Background Operations & High Priority Interrupt (HPI)
- Error free memory access
  - Internal error correction code (ECC) to protect data communication
  - Internal enhanced data management algorithm
  - Solid protection of sudden power failure safe-update operations for data content
- Security
  - Support secure bad block erase commands
  - Enhanced write Protection with permanent and partial protection options
- Supports Field Firmware Update(FFU)
- Enhanced Device Life time
- Optimal Size
- Supports Production State Awareness
- Supports Power Off Notification for Sleep

<Low power DDR2>

- Density: 4Gbits
- Organization
  - × 32 bits: 16M words × 32 bits × 8 banks
  - Row Address: R0 ~ R13
  - Column Address: C0 ~ C9
- Power supply
  - VDD1 = 1.70V to 1.95V ,VDD2, VDDQ = 1.14V to 1.30V
- Data rate: 1066Mbps max. (RL = 8)
- Interface: HSUL_12
- Burst lengths (BL): 4, 8, 16
- Burst type (BT)
  - Sequential (4, 8, 16)
  - Interleave (4, 8)
- Read latency (RL): 5, 6, 7, 8
- Refresh cycles: 8192 cycles/28ms
  - – Average refresh period: 3.4µs
  - - Storage temperature range: –40°C to +110°C
  - – Operating junction temperature range TJ = -15°C to +80°C

1. e•MMC™ Device and System

1.1. e•MMC™ System Overview

The *e*•MMC™ specification covers the behavior of the interface and the Device controller. As part of this specification the existence of a host controller and a memory storage array are implied but the operation of these pieces is not fully specified.

The Apollo NAND Device contains a single chip MMC controller and NAND flash memory module. The micro-controller interfaces with a host system allowing data to be written to and read from the NAND flash memory module. The controller allows the host to be independent from details of erasing and programming the flash memory.

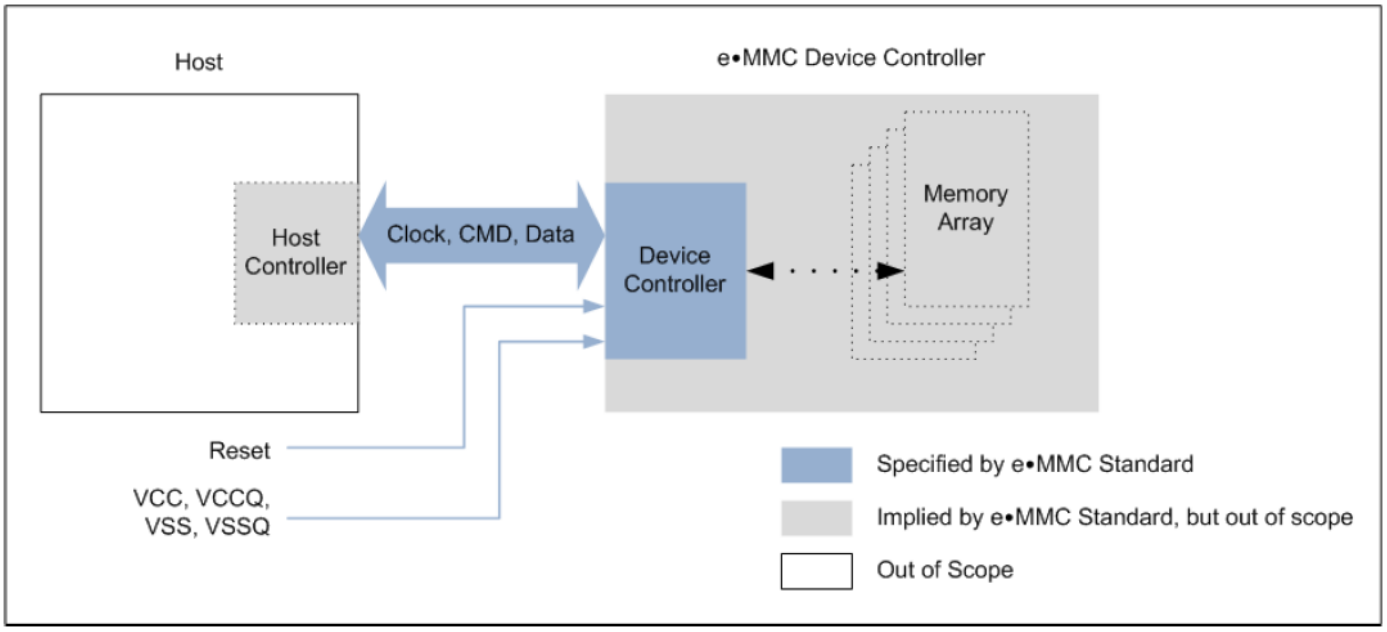


Figure 1 – *e*•MMC™ System Overview

1.2. *e•MMC™ Device Overview*

The *e*•MMC™ device transfers data via a configurable number of data bus signals. The communication signals are:

1.2.1 Clock (CLK)

Each cycle of this signal directs a one bit transfer on the command and either a one bit (1x) or a two bits transfer (2x) on all the data lines. The frequency may vary between zero and the maximum clock frequency.

1.2.2 Command (CMD)

This signal is a bidirectional command channel used for Device initialization and transfer of commands. The CMD signal has two operation modes: open-drain for initialization mode, and push-pull for fast command transfer. Commands are sent from the *e*•MMC™ host controller to the *e*•MMC™ Device and responses are sent from the Device to the host.

1.2.3 Input/Outputs (DAT0-DAT7)

These are bidirectional data channels. The DAT signals operate in push-pull mode. Only the Device or the host is driving these signals at a time. By default, after power up or reset, only DAT0 is used for data transfer. A wider data bus can be configured for data transfer, using either DAT0-DAT3 or DAT0-DAT7, by the *e*•MMC™ host controller. The *e*•MMC™ Device includes internal pull-ups for data lines DAT1-DAT7. Immediately after entering the 4-bit mode, the Device disconnects the internal pull ups of lines DAT1, DAT2, and DAT3. Correspondingly, immediately after entering to the 8-bit mode the Device disconnects the internal pull-ups of lines DAT1–DAT7.The signals on the *e*•MMC™ interface are described in Table 3.

Table 3 – *e*•MMC™ Interface

Name	Type[1]	Description
CLK	I	Clock
DAT0	I/O/PP	Data
DAT1	I/O/PP	Data
DAT2	I/O/PP	Data
DAT3	I/O/PP	Data
DAT4	I/O/PP	Data
DAT5	I/O/PP	Data
DAT6	I/O/PP	Data
DAT7	I/O/PP	Data
CMD	I/O/PP/OD	Command/Response
RST_n	I	Hardware reset
VCC	S	Supply voltage for Core
VCCQ	S	Supply voltage for I/O
VSS	S	Supply voltage ground for Core
VSSQ	S	Supply voltage ground for I/O
Note1：**I**: input; **O**: output; **PP**: push-pull; **OD**: open-drain; **NC**: Not connected (or logical high); **S**: power supply.		

Each Device has a set of information registers (see also 0, Device Registers.)

Table 4 – *e*•MMC™ Registers

Name	Width (bytes)	Description	Implementation
CID	16	Device Identification number, an individual number for identification.	Mandatory
RCA	2	Relative Device Address, is the Device system address, dynamically assigned by the host during initialization.	Mandatory
DSR	2	Driver Stage Register, to configure the Device's output drivers.	Optional
CSD	16	Device Specific Data, information about the Device operation conditions.	Mandatory
OCR	4	Operation Conditions Register. Used by a special broadcast command to identify the voltage type of the Device.	Mandatory
EXT_CSD	512	Extended Device Specific Data. Contains information about the Device capabilities and selected modes. Introduced in standard v4.0	Mandatory

The host may reset the device by:

- Switching the power supply off and back on. The device shall have its own power-on detection circuitry which puts the device into a defined state after the power-on Device.
- A reset signal
- By sending a special command

1.3. Bus Speed Modes

e•MMC™ defines several bus speed modes. **Table 5** summarizes the various modes.

Table 5— Bus Speed Modes

Mode Name	Data Rate	IO Voltage	Bus Width	Frequency	Max Data Transfer (implies x8 bus width)
Backwards Compatibility with legacy MMC card	Single	3.3/1.8V	1, 4, 8	0-26MHz	26MB/s
High Speed SDR	Single	3.3/1.8V	4, 8	0-52MHz	52MB/s
High Speed DDR	Dual	3.3/1.8V	4, 8	0-52MHz	104MB/s
HS200	Single	1.8V	4, 8	0-200MHz	200MB/s

1.3.1 HS200 Bus Speed Mode

The HS200 mode offers the following features:

- SDR Data sampling method
- CLK frequency up to 200MHz Data rate – up to 200MB/s
- 8-bits bus width supported
- Single ended signaling with 4 selectable Drive Strength
- Signaling levels of 1.8V
- Tuning concept for Read Operations

1.3.2 HS200 System Block Diagram

Figure 2 shows a typical HS200 Host and Device system. The host has a clock generator, which supplies CLK to the Device. For write operations, clock and data direction are the same, write data can be transferred synchronous with CLK, regardless of transmission line delay. For read operations, clock and data direction are opposite; the read data received by Host is delayed by round-trip delay, output delay and latency of Host and Device. For reads, the Host needs to have an adjustable sampling point to reliably receive the incoming data.

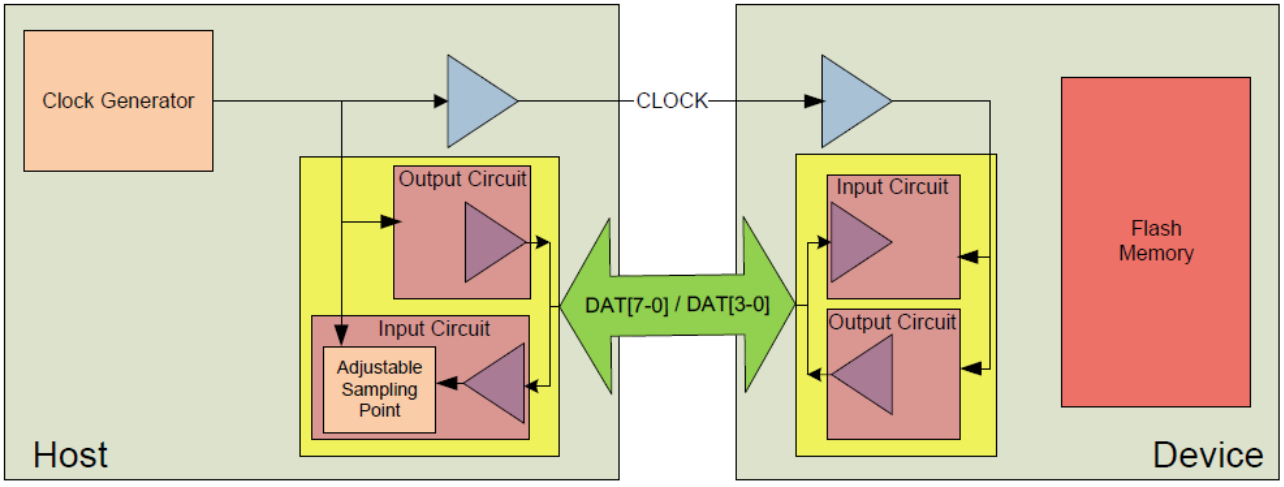


Figure 2 — Host and Device Block Diagram

2. e•MMC™ Functional Description

2.1 e•MMC™ Overview

All communication between host and device are controlled by the host (master). The host sends a command, which results in a device response. For more details, refer to section 6.1 of the JEDEC Standard Specification No.JESD84-B50.

Five operation modes are defined for the *e*•MMC™ system (hosts and devices):

- Boot mode
- Device identification mode
- Interrupt mode
- Data transfer mode
- Inactive mode

2.2 Boot Operation Mode

In boot operation mode, the master (*e*•MMC™ host) can read boot data from the slave (*e*•MMC™ device) by keeping CMD line low or sending CMD0 with argument + 0xFFFFFFFA, before issuing CMD1. The data can be read from either boot area or user area depending on register setting. For more details, refer to section 6.3 of the JEDEC Standard Specification No.JESD84-B50.

2.3 Device Identification Mode

While in device identification mode the host resets the device , validates operation voltage range and access mode, identifies the device and assigns a Relative device Address (RCA) to the device on the bus. All data communication in the Device Identification Mode uses the command line (CMD) only. For more details, refer to section 6.4 of the JEDEC Standard Specification No.JESD84-B50.

2.4 Interrupt Mode

The interrupt mode on the *e*•MMC™ system enables the master (*e*•MMC™ host) to grant the transmission allowance to the slaves (Device) simultaneously. This mode reduces the polling load for the host and hence, the power consumption of the system, while maintaining adequate responsiveness of the host to a Device request for service. Supporting *e*•MMC™ interrupt mode is an option, both for the host and the Device. For more details, refer to section 6.5 of the JEDEC Standard Specification No.JESD84-B50.

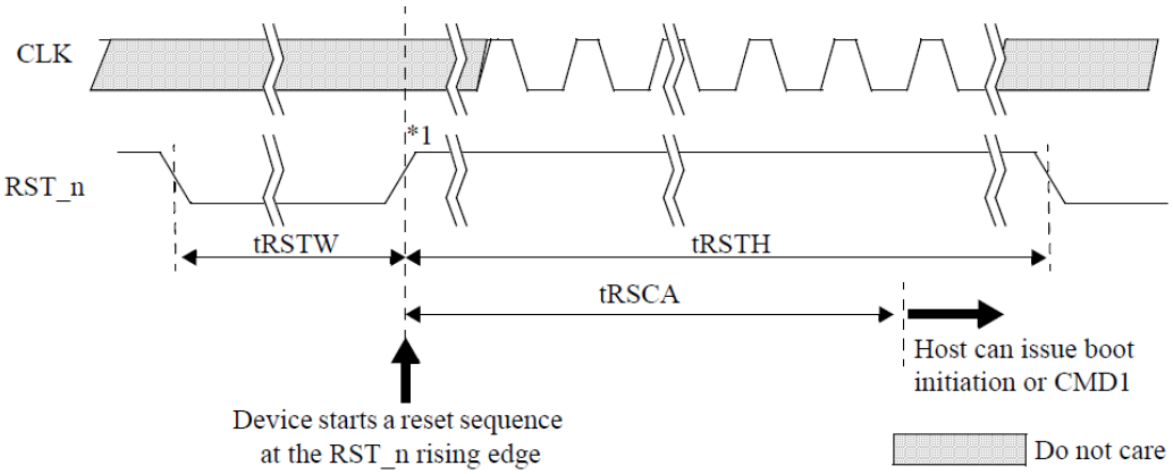
2.5 Data Transfer Mode

When the Device is in *Stand-by* State, communication over the CMD and DAT lines will be performed in push-pull mode. For more details, refer to section 6.6 of the JEDEC Standard Specification No.JESD84-B50.

*2.6*Inactive Mode

The device will enter inactive mode if either the device operating voltage range or access mode is not valid. The device can also enter inactive mode with GO_INACTIVE_STATE command (CMD15). The device will reset to *Pre-idle* state with power cycle. For more details, refer to section 6.1 of the JEDEC Standard Specification No.JESD84-B50.

2.7 H/W Reset Operation



Note1: Device will detect the rising edge of RST_n signal to trigger internal reset sequence

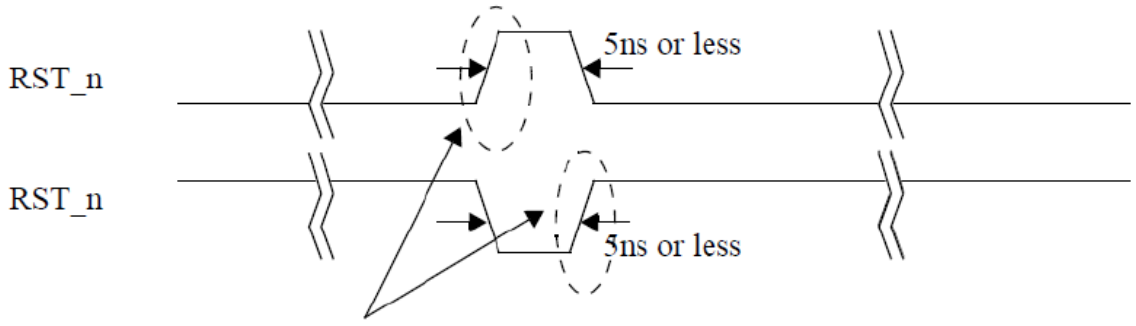
Figure 3 – H/W Reset Waveform

Table 6 – H/W Reset Timing Parameters

Symbol	Comment	Min	Max	Unit
tRSTW	RST_n pulse width	1		[us]
tRSCA	RST_n to Command time	200[1]		[us]
tRSTH	RST_n high period (interval time)	1		[us]
Note1：74 cycles of clock signal required before issuing CMD1 or CMD0 with argument 0xFFFFFFFA				

2.8 Noise Filtering Timing for H/W Reset

Device must filter out 5ns or less pulse width for noise immunity



Device must not detect these rising edge

Figure 4 – Noise Filtering Timing for H/W Reset

Device must not detect 5ns or less of positive or negative RST_n pulse. Device must detect more than or equal to 1us of positive or negative RST_n pulse width.

3. The e•MMC™ bus

The *e*•MMC™ bus has ten communication lines and three supply lines:

- **CMD**：Command is a bidirectional signal. The host and Device drivers are operating in two modes, open drain and push/pull.
- **DAT0-7**：Data lines are bidirectional signals. Host and Device drivers are operating in push-pull mode
- **CLK**：Clock is a host to Device signal. CLK operates in push-pull mode

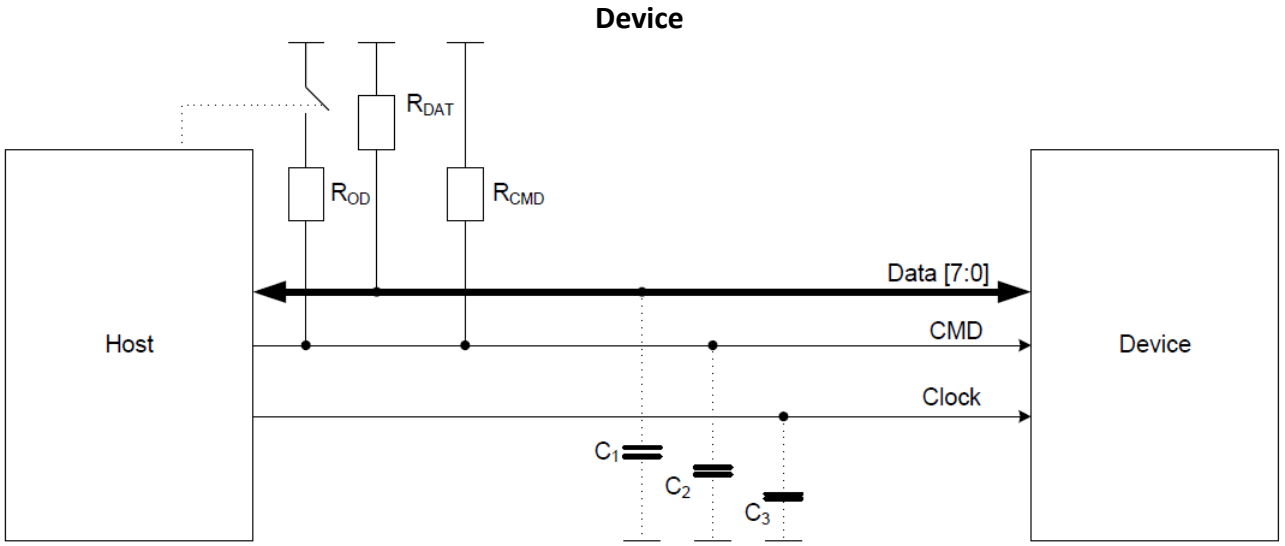


Figure 5 – Bus Circuitry Diagram

The R_{OD} is switched on and off by the host synchronously to the open-drain and push-pull mode transitions. The host does not have to have open drain drivers, but must recognize this mode to switch on the R_{OD}. R_{DAT} and R_{CMD} are pull-up resistors protecting the CMD and the DAT lines against bus floating device when all device drivers are in a high-impedance mode.

A constant current source can replace the R_{OD} by achieving a better performance (constant slopes for the signal rising and falling edges). If the host does not allow the switchable R_{OD} implementation, a fixed R_{CMD} can be used).

3.1. Power-up

3.1.1 e•MMC™ power-up

An *e*•MMC™ bus power-up is handled locally in each device and in the bus master. Figure 6 shows the power-up sequence and is followed by specific instructions regarding the power-up sequence. Refer to section 10.1 of the JEDEC Standard Specification No.JESD84-B50 for specific instructions regarding the power-up sequence.

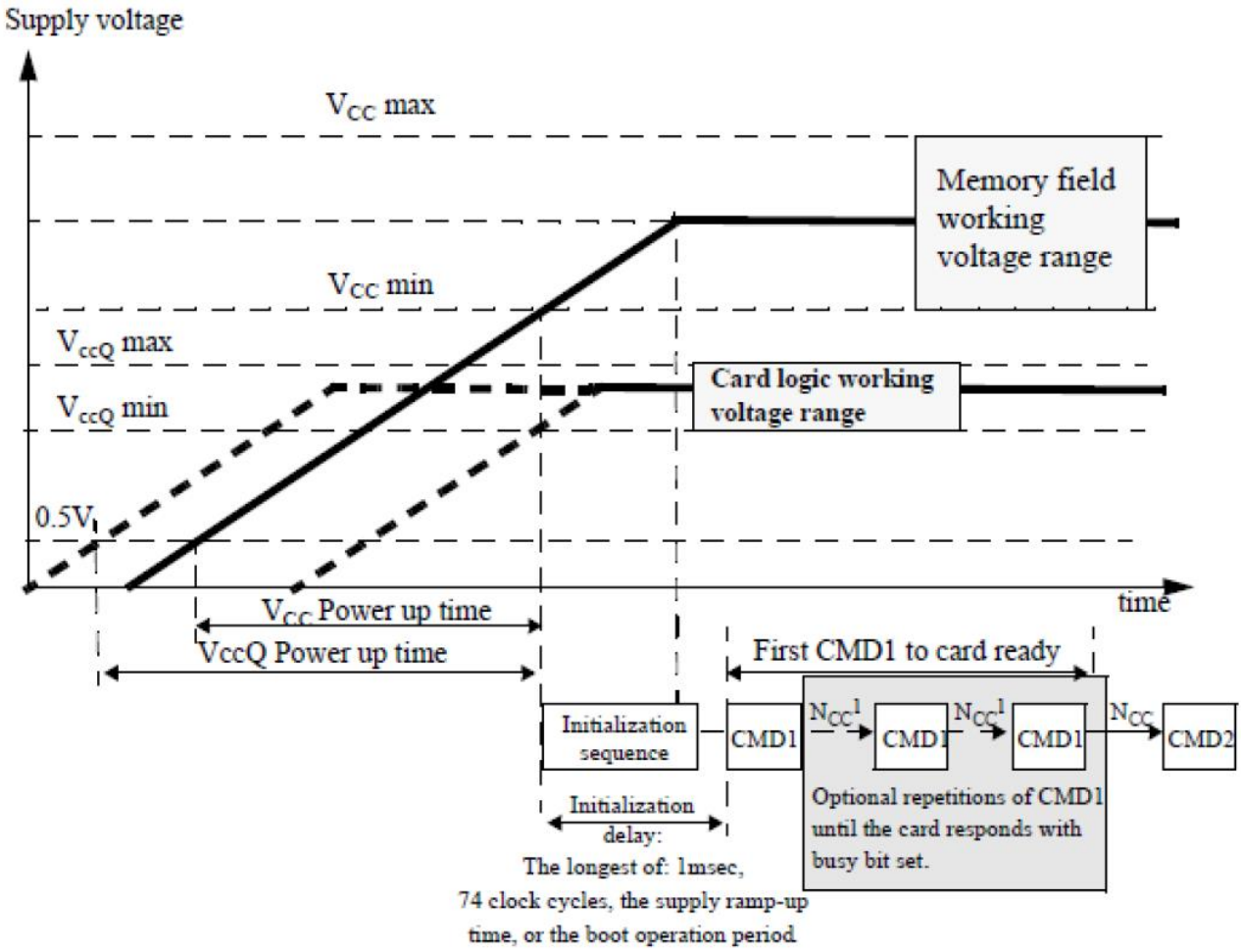


Figure 6 – *e*•MMC™ Power-up Diagram

3.1.2 *e•MMC™ Power Cycling*

The master can execute any sequence of V_{CC} and V_{CCQ} power-up/power-down. However, the master must not issue any commands until V_{CC} and V_{CCQ} are stable within each operating voltage range. After the slave enters sleep mode, the master can power-down V_{CC} to reduce power consumption. It is necessary for the slave to be ramped up to V_{CC} before the host issues CMD5 (SLEEP_AWAKE) to wake the slave unit. For more information about power cycling see Section 10.1.3 of the JEDEC Standard Specification No.JESD84-B50.

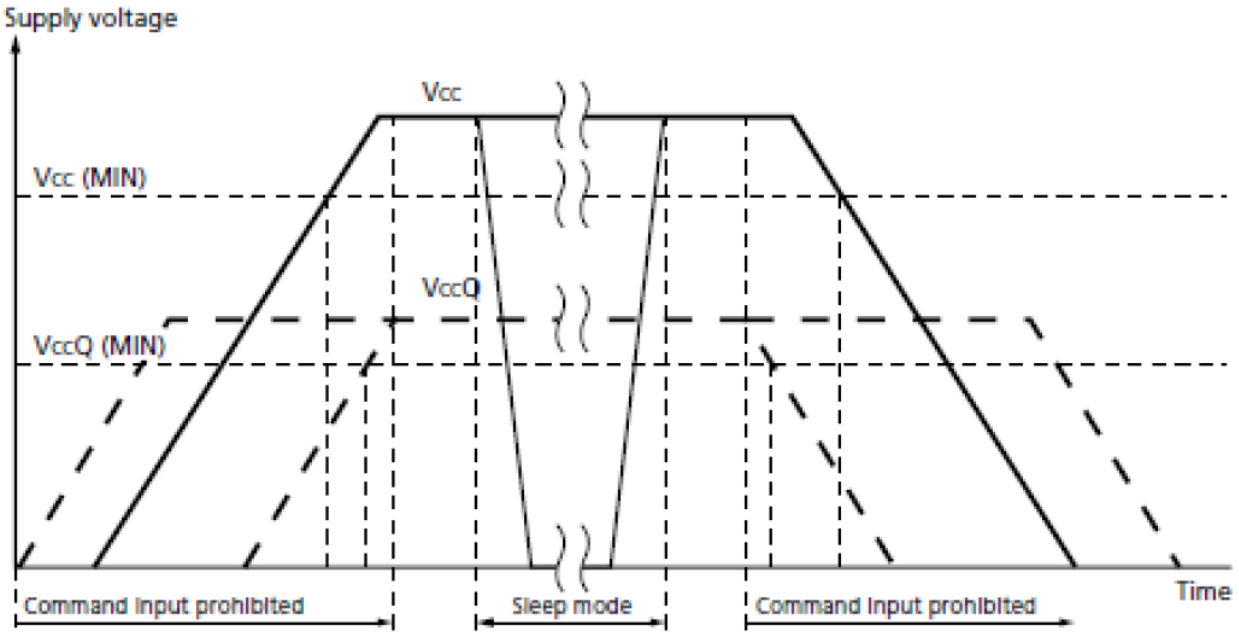


Figure 7 – The *e•*MMC™ Power Cycle

3.1.3 *Bus Operating Conditions*

Parameter	Symbol	Min	Max.	Unit	Remark
Peak voltage on all lines		-0.5	VCCQ + 0.5	V	
All Inputs					
Input Leakage Current (before initialization sequence and/or the internal pull up resistors connected)		-100	100	µA	
Input Leakage Current (after initialization sequence and the internal pull up resistors disconnected)		-2	2	µA	
All Outputs					
Output Leakage Current (before initialization sequence)		-100	100	µA	
Output Leakage Current (after initialization sequence)		-2	2	µA	
Note1：Initialization sequence is defined in section 10.1					

Table 7 – General Operating Conditions

3.1.4 *Power supply: e•MMC™*

In the *e*•MMC™, V_{CC} is used for the NAND flash device and its interface voltage; V_{CCQ} is for the controller and the MMC interface voltage shown in Figure 8. The core regulator is optional and only required when internal core logic voltage is regulated from V_{CCQ}. A C_{Reg} capacitor must be connected to the V_{Ddi} terminal to stabilize regulator output on the system.

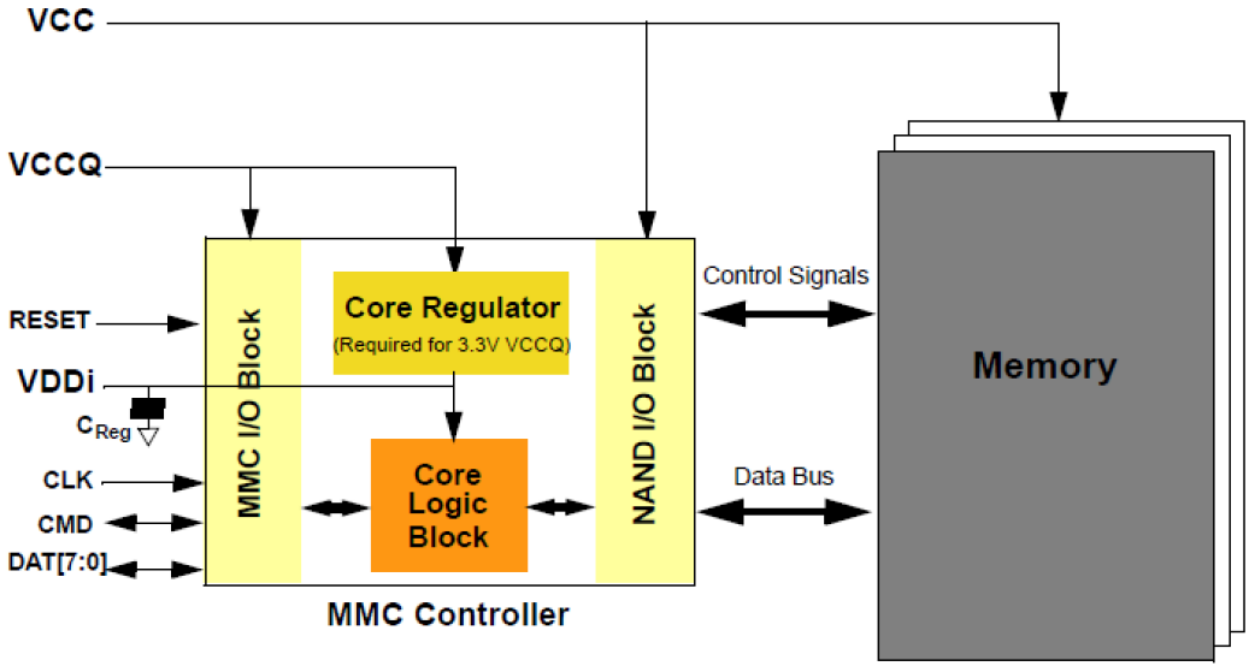


Figure 8 – *e*•MMC™ Internal Power Diagram

3.1.5 *e*•MMC™ Power Supply Voltage

The *e*•MMC™ supports one or more combinations of VCC and VCCQ as shown in Table 8. The VCCQ must be defined at equal to or less than VCC. The available voltage configuration is shown in Table 9.

Table 8 – *e*•MMC™ Power Supply Voltage

Parameter	Symbol	MIN	MAX	Unit	Remarks
Supply voltage (NAND)	VCC	2.7	3.6	V	
Supply voltage (I/O)	VCCQ	2.7	3.6	V	
		1.65	1.95	V	
Supply power-up for 3.3V	t_{PRUH}		35	ms	
Supply power-up for 1.8V	t_{PRUL}		25	ms	

The *e*•MMC™ must support at least one of the valid voltage configurations, and can optionally support all valid voltage configurations (see Table 9).

Table 9 – *e*•MMC™ Voltage Combinations

		VccQ	
		1.65V–1.95V	**2.7V–3.6V**[1]
Vcc	**2.7V-3.6V**	Valid	Valid
Note1：VccQ (I/O) 3.3 volt range is not supported in HS200 devices			

3.1.6 Bus Signal Line Load

The total capacitance C_L of each line of the *e*•MMC™ bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself, and the capacitance C_{DEVICE} of the Device connected to this line,

$$C_L = C_{HOST} + C_{BUS} + C_{DEVICE}$$

and requiring the sum of the host and bus capacitances not to exceed 20 pF (see Table 10).

Table 10 – Capacitance

Parameter	Symbol	Min	Max	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7	50	Kohm	to prevent bus floating
Pull-up resistance for DAT0–7	R_{DAT}	10	50	Kohm	to prevent bus floating
Pull-up resistance for RST_n	R_{RST_n}	4.7	50	Kohm	It is not necessary to put pull-up resistance on RST_n (H/W rest) line if host does not use H/W reset. (Extended CSD register [162] = 0 b)
Bus signal line capacitance	CL		30	pF	Single Device
Single Device capacitance	C_{BGA}		12	pF	
Maximum signal line inductance			16	nH	
Impedance on CLK / CMD / DAT0~7		45	55	ohm	Impedance match
Serial's resistance on CLK line	SR_{CLK}	0	47	ohm	
Serial's resistance on CMD / DAT0~7 line	SR_{CMD} $SR_{DAT0\sim7}$	0	47	ohm	
VccQ decoupling capacitor		2.2+0.1	4.7+0.22	µF	It should be located as close as possible to the balls defined in order to minimize connection parasitics
	CH1	1	2.2		CH1 should be placed adjacent to VccQ-VssQ balls (#K6 and #K4 accordingly, next to DAT [7..0] balls), It should be located as close as possible to the balls defined in order to minimize connection parasitics.
VCC capacitor value		1+0.1	4.7+0.22	µF	It should be located as close as possible to the balls defined in order to minimize connection parasitics
V_{Ddi} capacitor value	C_{REG}	1	4.7+0.1	µF	To stabilize regulator output to controller core logics. It should be located as close as possible to the balls defined in order to minimize connection parasitics

3.1.7 Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.

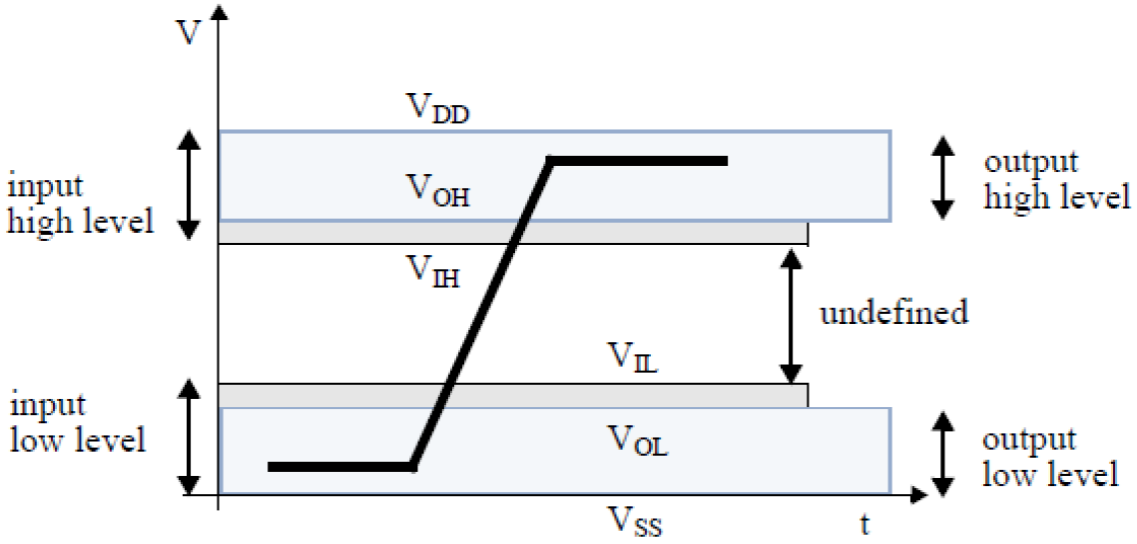


Figure 9 – Bus Signal Levels

3.1.8 Open-drain Mode Bus Signal Level

Table 11 – Open-drain Bus Signal Level

Parameter	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	VOH	VDD – 0.2		V	IOH = -100 µA
Output LOW voltage	VOL		0.3	V	IOL = 2 mA

The input levels are identical with the push-pull mode bus signal levels.

3.1.9 Push-pull mode bus signal level— *e*•MMC™

The device input and output voltages shall be within the following specified ranges for any V_{DD} of the allowed voltage range

For 2.7V-3.6V V_{CCQ} range (compatible with JESD8C.01)

Table 12 – Push-pull Signal Level—High-voltage *e*•MMC™

Parameter	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	VOH	0.75 * VCCQ		V	IOH = -100 µA @ VCCQ min
Output LOW voltage	VOL		0.125 * VCCQ	V	IOL = 100 µA @ VCCQ min
Input HIGH voltage	VIH	0.625 * VCCQ	VCCQ + 0.3	V	
Input LOW voltage	VIL	VSS – 0.3	0.25 * VCCQ	V	

For 1.65V – 1.95V VCCQ range (: Compatible with EIA/JEDEC Standard “EIA/JESD8-7 Normal Range” as defined in the following table.

Table 13 – Push-pull Signal Level—1.65-1.95 VCCQ Voltage Range

Parameter	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	VOH	V V_{CCQ} – 0.45V		V	IOH = -2mA
Output LOW voltage	VOL		0.45V	V	IOL = 2mA
Input HIGH voltage	VIH	0.65 * V_{CCQ} [1]	V_{CCQ} + 0.3	V	
Input LOW voltage	VIL	V_{SS} – 0.3	0.35 * V_{DD} [2]	V	

Note1：0.7 * V_{DD} for MMC™4.3 and older revisions.
Note2：0.3 * V_{DD} for MMC™4.3 and older revisions.

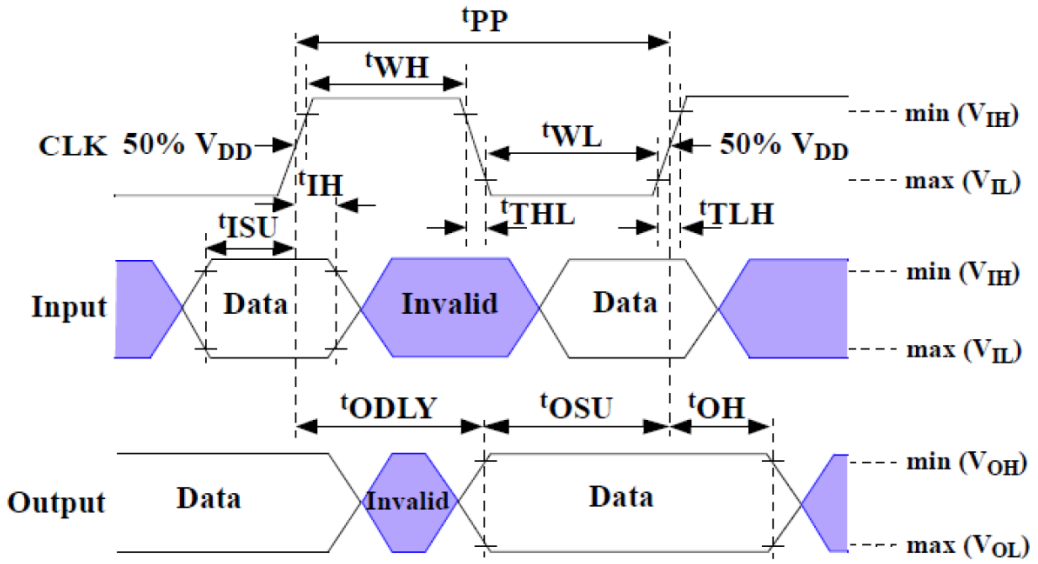
3.1.10 Bus Operating Conditions for HS200

The bus operating conditions for HS200 devices is the same as specified in sections 10.4.1 of JESD84-B50through 10.4.2 of JESD84-B50. The only exception is that V_{CCQ}=3.3v is not supported.

3.1.11 Device Output Driver Requirements for HS200

Refer to section 10.4.4 of the JEDEC Standard Specification No.JESD84-B50.

3.2. Bus Timing



Data must always be sampled on the rising edge of the clock.

Figure 10 – Timing Diagram: Data Input/Output

3.3. Device Interface Timings

Table 14 – High-speed Device Interface Timing

Parameter	Symbol	Min	Max.	Unit	Remark
Clock CLK[1]					
Clock frequency Data Transfer Mode (PP)[2]	fPP	0	52[3]	MHz	CL ≤ 30 pF Tolerance:+100KHz
Clock frequency Identification Mode (OD)	fOD	0	400	kHz	Tolerance: +20KHz
Clock high time	tWH	6.5		ns	CL ≤ 30 pF
Clock low time	tWL	6.5		ns	CL ≤ 30 pF
Clock rise time[4]	tTLH		3	ns	CL ≤ 30 pF
Clock fall time	tTHL		3	ns	CL ≤ 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	tISU	3		ns	CL ≤ 30 pF
Input hold time	tIH	3		ns	CL ≤ 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output delay time during data transfer	tODLY		13.7	ns	CL ≤ 30 pF
Output hold time	tOH	2.5		ns	CL ≤ 30 pF
Signal rise time[5]	tRISE		3	ns	CL ≤ 30 pF
Signal fall time	tFALL		3	ns	CL ≤ 30 pF

Note1：CLK timing is measured at 50% of VDD.

Note2：A *e*·MMC™ shall support the full frequency range from 0-26Mhz or 0-52MHz

Note3：Device can operate as high-speed Device interface timing at 26 MHz clock frequency.

Note4：CLK rise and fall times are measured by min (VIH) and max (VIL).

Note5：Inputs CMD DAT rise and fall times are measured by min (VIH) and max (VIL) and outputs CMD DAT rise and fall times are measured by min (VOH) and max (VOL). “

Table 15 – Backward-compatible Device Interface Timing

Parameter	Symbol	Min	Max.	Unit	Remark[1]
Clock CLK[2]					
Clock frequency Data Transfer Mode (PP)[3]	fPP	0	26	MHz	CL ≤ 30 pF
Clock frequency Identification Mode (OD)	fOD	0	400	kHz	
Clock high time	tWH	10			CL ≤ 30 pF
Clock low time	tWL	10		ns	CL ≤ 30 pF
Clock rise time[4]	tTLH		10	ns	CL ≤ 30 pF
Clock fall time	tTHL		10	ns	CL ≤ 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	tISU	3		ns	CL ≤ 30 pF
Input hold time	tIH	3		ns	CL ≤ 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output set-up time[5]	tOSU	11.7		ns	CL ≤ 30 pF
Output hold time[5]	tOH	8.3		ns	CL ≤ 30 pF

Note1：The Device must always start with the backward-compatible interface timing. The timing mode can be switched to high-speed interface timing by the host sending the SWITCH command (CMD6) with the argument for high-speed interface select.

Note2：CLK timing is measured at 50% of VDD.

Note3：For compatibility with Devices that support the v4.2 standard or earlier, host should not use > 26 MHz before switching to high-speed interface timing.

Note4：CLK rise and fall times are measured by min (VIH) and max (VIL).

Note5：tOSU and tOH are defined as values from clock rising edge. However, there may be Devices or devices which utilize clock falling edge to output data in backward compatibility mode. Therefore, it is recommended for hosts either to settWL value as long as possible within the range which will not go over tCK-tOH(min) in the system or to use slow clock frequency, so that host could have data set up margin for those devices. In this case, each devicewhich utilizes clock falling edge might show the correlation either between tWL and tOSU or between tCK and tOSU for the device in its own datasheet as a note or its application notes.

3.4. Bus Timing for DAT Signals During Dual Data Rate Operation

These timings applies to the DAT[7:0] signals only when the device is configured for dual data mode operation. In this dual data mode, the DAT signals operates synchronously of both the rising and the falling edges of CLK. The CMD signal still operates synchronously of the rising edge of CLK and therefore complies with the bus timing specified in section 10.5, therefore there is no timing change for the CMD signal.

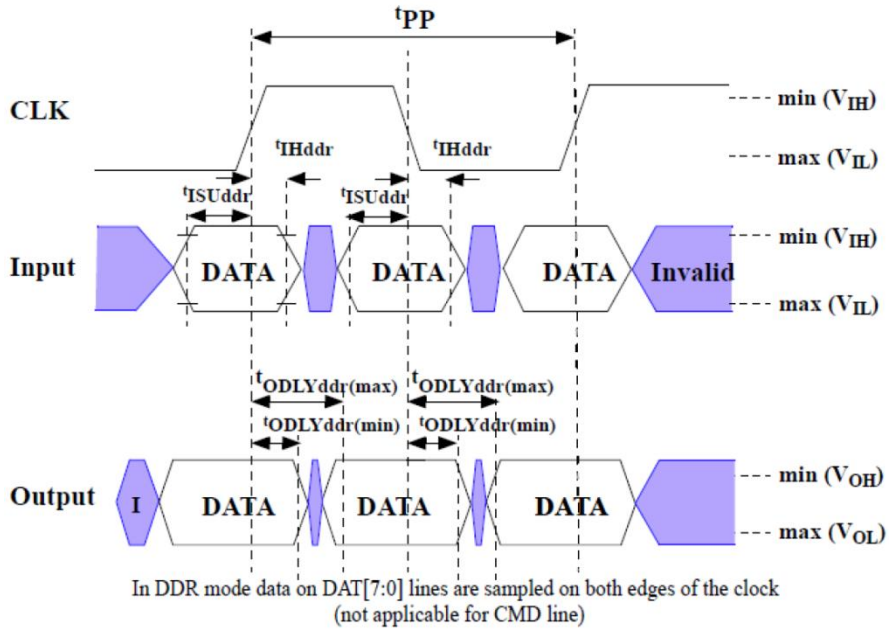


Figure 11 – Timing Diagram: Data Input/Output in Dual Data Rate Mode

6.1.1 Dual Data Rate Interface Timings

Table 16 – High-speed Dual Data Rate Interface Timing

Parameter	Symbol	Min	Max.	Unit	Remark
Input CLK[1]					
Clock duty cycle		45	55	%	Includes jitter, phase noise
Input DAT (referenced to CLK-DDR mode)					
Input set-up time	tISUddr	2.5		ns	CL ≤ 20 pF
Input hold time	tIHddr	2.5		ns	CL ≤ 20 pF
Output DAT (referenced to CLK-DDR mode)					
Output delay time during data transfer	tODLYddr	1.5	7	ns	CL ≤ 20 pF
Signal rise time (all signals)[2]	tRISE		2	ns	CL ≤ 20 pF
Signal fall time (all signals)	tFALL		2	ns	CL ≤ 20 pF

Note1：CLK timing is measured at 50% of VDD.

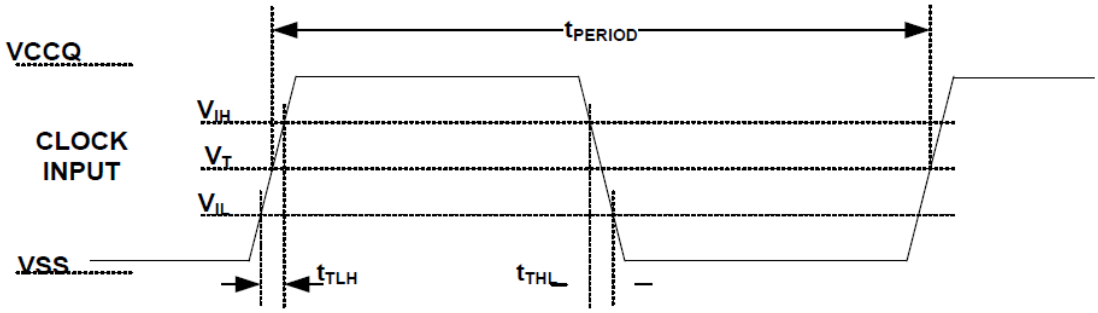
Note2：Inputs CMD, DAT rise and fall times are measured by min (V_{IH}) and max (V_{IL}), and outputs CMD, DAT rise and fall times are measured by min (V_{OH}) and max (V_{OL})

3.5. Bus Timing Specification in HS200 Mode

3.5.1 HS200 Clock Timing

Host CLK Timing in HS200 mode shall conform to the timing specified in Figure 12 and **Table 17**. CLK input shall satisfy the clock timing over all possible operation and environment conditions. CLK input parameters should be measured while CMD and DAT lines are stable high or low, as close as possible to the Device.

The maximum frequency of HS200 is 200MHz. Hosts can use any frequency up to the maximum that HS200 mode allows.



Note1：V_{IH} denote V_{IH}(min.) and V_{IL} denotes V_{IL}(max.).

Note2：V_T=0.975V – Clock Threshold, indicates clock reference point for timing measurements.

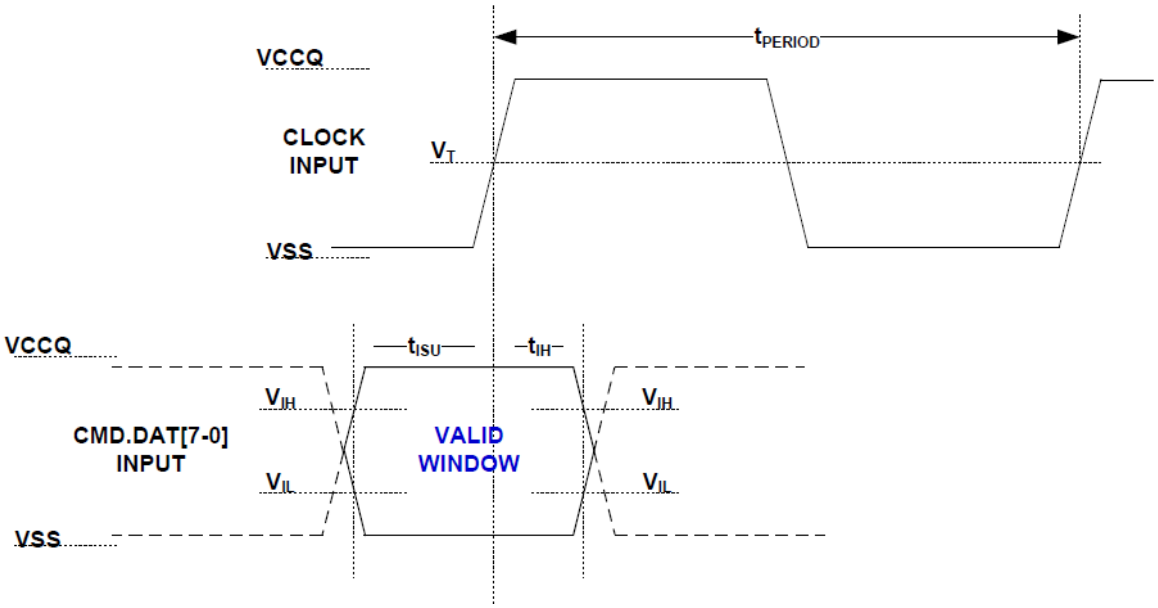
Figure 12 – HS200 Clock Signal Timing

Table 17 – HS200 Clock Signal Timing

Symbol	Min.	Max.	Unit	Remark
t_{PERIOD}	5	-	ns	200MHz (Max.), between rising edges
t_{TLH}, t_{THL}	-	0.2* t_{PERIOD}	ns	t_{TLH}, t_{THL} < 1ns (max.) at 200MHz, C_{BGA}=12pF, The absolute maximum value of t_{TLH}, t_{THL} is 10ns regardless of clock frequency.
Duty Cycle	30	70	%	

3.5.2 HS200 Device Input Timing

Figure 13 and Table 18 define Device input timing.



Note1: t_{ISU} and t_{IH} are measured at V_{IL}(max.) and V_{IH}(min.).
Note2: V_{IH} denote V_{IH}(min.) and V_{IL} denotes V_{IL}(max.).

Figure 13 – HS200 Device Input Timing

Table 18 – HS200 Device Input Timing

Symbol	Min.	Max.	Unit	Remark
t_{ISU}	1.4	-	ns	$5pF \leq C_{BGA} \leq 12pF$
t_{IH}	0.8		ns	$5pF \leq C_{BGA} \leq 12pF$

4 LPDDR2 Interface

4.1. Pin Function and Descriptions

Table 19 – Pin Function and Descriptions

Name	Type	Description
CK_t, CK_c	Input	**Clock:** CK_t and CK_c are differential clock inputs. All Double Data Rate (DDR) CA inputs are sampled on both positive and negative edge of CK_t. Single Data Rate (SDR) inputs, CS_n and CKE, are sampled at the positive Clock edge. Clock is defined as the differential pair, CK_t and CK_c. The positive Clock edge is defined by the crosspoint of a rising CK_t and a falling CK_c. The negative Clock edge is defined by the crosspoint of a falling CK_t and a rising CK_c.
CKE	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates internal clock signals and therefore device input buffers and output drivers. Power savings modes are entered and exited through CKE transitions. CKE is considered part of the command code. See Command Truth Table for command code descriptions. CKE is sampled at the positive Clock edge.
CS	Input	**Chip Select:** CS_n is considered part of the command code. See Command Truth Table for command code descriptions. CS_n is sampled at the positive Clock edge.
CA0 – CA9	Input	**DDR Command/Address Inputs:** Uni-directional command/address bus inputs. CA is considered part of the command code. See Command Truth Table for command code descriptions.
DQ0 – DQ31	I/O	Data Inputs/Output: Bi-directional data bus
DQS0_t – DQS3_t, DQS0_c – DQS3_c	I/O	**Data Strobe (Bi-directional, Differential):** The data strobe is bi-directional (used for read and write data) and differential (DQS_t and DQS_c). It is output with read data and input with write data. DQS_t is edge-aligned to read data and centered with write data. DQS0_t and DQS0_c correspond to the data on DQ0 – DQ7, DQS1_t and DQS1_c to the data on DQ8 – DQ15, DQS2_t and DQS2_c to the data on DQ16 – DQ23, DQS3_t and DQS3_c to the data on DQ24 – DQ31.
DM0 – DM3	Input	**Input Data Mask:** DM is the input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS_t. Although DM is for input only, the DM loading shall match the DQ and DQS (or DQS_c). DM0 is the input data mask signal for the data on DQ0-7, DM1 is the input data mask signal for the data on DQ8-15, DM2 is the input data mask signal for the data on DQ16-23, DM3 is the input data mask signal for the data on DQ24-31.
VDD1	Supply	**Core Power Supply 1**
VDD2	Supply	**Core Power Supply 2**
VDDCA	Supply	**Input Receiver Power Supply:** Power supply for CA0-9, CKE, CS_n, CK_t, and CK_c input buffers.
VDDQ	Supply	**I/O Power Supply:** Power supply for Data input/output buffers.
VREF(CA)	Supply	**Reference Voltage for CA Command and Control Input Receiver:** Reference voltage for all CA0-9, CKE, CS_n, CK_t, and CK_c input buffers.
VREF(DQ)	Supply	**Reference Voltage for DQ Input Receiver:** Reference voltage for all Data input buffers.
VSS	Supply	**Ground**
VSSCA	Supply	**Ground for Input Receivers**
VSSQ	Supply	**I/O Ground**
ZQ	I/O	**Reference Pin for Output Drive Strength Calibration**

4.2. Simplified State Diagram

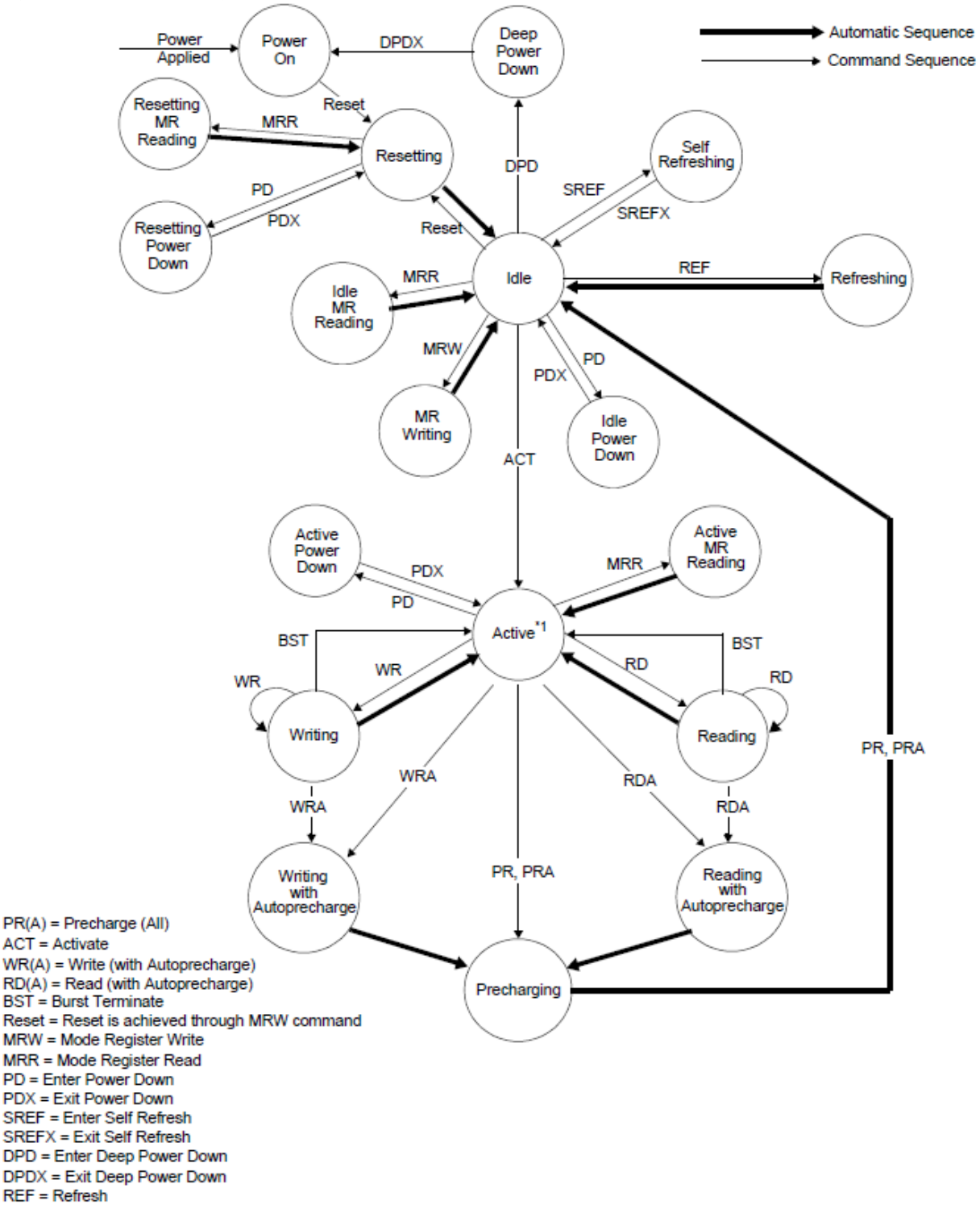


Figure 14 — Simplified Bus Interface State Diagram

Note 1: For DDR2 Mobile RAM in the Idle state, all banks are precharged.

4.3. Electrical Conditions

All voltages are referenced to VSS (GND)

- Execute power-up and Initialization sequence before proper device operation is achieved.
- Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the DDR2 Mobile RAM Device must be powered down and then restarted through the specialized initialization sequence before normal operation can continue.
-

4.3.1 Absolute Maximum Ratings

Table 20 Absolute Maximum Ratings

Parameter	Symbol	min.	max.	Unit	Note
VDD1 supply voltage relative to VSS	VDD1	-0.4	2.3	V	2
VDD2 supply voltage relative to VSS	VDD2	-0.4	1.6	V	2
VDDQ supply voltage relative to VSSQ	VDDQ	-0.4	1.6	V	2, 3
Voltage on any ball relative to VSS	VIN, VOUT	-0.4	1.6	V	
Storage Temperature	TSTG	-40	110	°C	

Notes: 1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. See Power-Ramp section "Power-up, initialization and Power-Off" on section7.6 for relationship between power supplies.
3. VREF ≤ 0.6 x VDDQ; however, VREF may be ≥ VDDQ provided that VREF ≤ 300mV.
4. Storage Temperature is the case surface temperature on the center/top side of the DDR2 Mobile RAM Device. For the measurement conditions, please refer to JESD51-2 standard.

Caution

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

4.3.2 Recommended DC Operating Conditions

Table 21 Recommended DC Operating Conditions(TJ = -15°C to +80°C)

Parameter	Symbol	min.	max.	Unit	Note
Core Power1	VDD1	1.7	1.8	1.95	V
Core Power2, Input Buffer Power	VDD2	1.14	1.2	1.3	V
I/O Buffer Power	VDDQ	1.14	1.2	1.3	V

4.3.3 AC and DC Input Measurement Levels

4.3.3.1 AC and DC Input Levels for Single-Ended CA/CS Signals

Table 22 Single-Ended AC and DC Input Levels for CA/CS Inputs

Parameter	Symbol	Speed	min.	max.	Unit	Note
AC input logic high	VIHCA(AC)	533 to 1066	VREF + 0.220	Note 2	V	1, 2
		400	VREF + 0.300			
AC input logic low	VILCA(AC)	533 to 1066	Note 2	VREF – 0.220	V	1, 2
		400		VREF – 0.300		
DC input logic high	VIHCA(DC)	533 to 1066	VREF + 0.130	VDD2	V	1
		400	VREF + 0.200			
DC input logic low	VILCA(DC)	533 to 1066	VSS	VREF – 0.130	V	1
		400		VREF – 0.200		
Reference Voltage for CA/CS inputs	VREFCA(DC)		0.49 × VDD2	0.51 × VDD2	V	3, 4

Notes: 1. For CA/CS input only pins. VREF = VREFCA(DC).
2. See “Overshoot and Undershoot Specifications” , please refer to JESD209-2F standard.
2. The ac peak noise on VREFCA may not allow VREFCA to deviate from VREFCA(DC) by more than ± 1% VDD2 (for reference: 26dditio. ± 12 mV).
3. For reference: 26dditio. VDD2/2 ± 12 mV.

4.3.3.2 AC and DC Input Levels for CKE

Table 23 Single-Ended AC and DC Input Levels for CKE

Parameter	Symbol	min.	max.	Unit	Note
CKE Input High Level	VIHCKE	0.8 × VDD2	Note 1	V	1
CKE Input Low Level	VILCKE	Note 1	0.2 × VDD2	V	1

Note: 1. See “Overshoot and Undershoot Specifications” , please refer to JESD209-2F standard.

4.3.3.3 AC and DC Input Levels for Single-Ended Data Signals

Table 24 Single-Ended AC and DC Input Levels for DQ and DM

Parameter	Symbol	Speed	min.	max.	Unit	Note
AC input logic high	VIHDQ(AC)	533 to 1066	VREF + 0.220	Note 2	V	1, 2
		400	VREF + 0.300			
AC input logic low	VILDQ(AC)	533 to 1066	Note 2	VREF – 0.220	V	1, 2
		400		VREF – 0.300		
DC input logic high	VIHDQ(DC)	533 to 1066	VREF + 0.130	VDDQ	V	1
		400	VREF + 0.200			
DC input logic low	VILDQ(DC)	533 to 1066	VSSQ	VREF – 0.130	V	1
		400		VREF – 0.200		
Reference Voltage for DQ, DM inputs	VREFDQ(DC)		0.49 × VDDQ	0.51 × VDDQ	V	3, 4

Notes: 1. For DQ input only pins. VREF = VREFDQ(DC).
2. See “Overshoot and Undershoot Specifications” , please refer to JESD209-2F standard.
3. The ac peak noise on VREFDQ may not allow VREFDQ to deviate from VREFDQ(DC) by more than ± 1% VDDQ (for reference: 26dditio. ± 12 mV).
4. For reference: 26dditio. VDDQ ± 12 mV.

4.3.3.4 Differential Swing Requirements for Clock (CK – /CK) and Strobe (DQS – /DQS)

Table 25 Differential AC and DC Input Levels

Parameter	Symbol	min.	max.	Unit	Note
Differential input high	VIHdiff(DC)	2 × (VIH(DC) – VREF)	Note 3	V	1
Differential input low	VILdiff(DC)	Note 3	2 × (VIL(DC) – VREF)	V	1
Differential input high AC	VIHdiff(AC)	2 × (VIH(AC) – VREF)	Note 3	V	2
Differential input low AC	VILdiff(AC)	Note 3	2 × (VIL(AC) – VREF)	V	2

Notes: 1. Used to define a differential signal slew-rate.
2. For CK – /CK use VIH/VIL(AC) of CA and VREFCA; for DQS – /DQS, use VIH/VIL(AC) of DQs and VREFDQ; if a reduced AC-high or AC-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however the single-ended signals CK, /CK, DQS, and /DQS need to be within the respective limits (VIH(DC) max, VIL(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot Specifications" , please refer to JESD209-2F standard
4. For CK and /CK, VREF = VREFCA(DC). For DQS and /DQS, VREF = VREFDQ(DC).

Table 26 Allowed Time Before Ringback (tDVAC) for CK – /CK and DQS – /DQS

Slew Rate [V/ns]	**tDVAC** [ps] @ **|VIH/Ldiff(AC)|** = 440mV	**tDVAC** [ps] @ **|VIH/Ldiff(AC)|** = 600mV
	min.	min.
> 4.0	175	75
4	170	57
3	167	50
2	163	38
1.8	162	34
1.6	161	29
1.4	159	22
1.2	155	13
1	150	0
< 1.0	150	0

4.3.3.5 Single-ended Requirements for Differential Signals

Table 27 Single-ended Levels for CK, DQS, /CK, /DQS

Parameter	Symbol	Speed	min.	max.	Unit	Note
Single-ended high-level for strobes	VSEH(AC)	533 to 1066	(VDDQ / 2) + 0.220	Note 3	V	1, 2
		400	(VDDQ / 2) + 0.300			
Single-ended high-level for CK, /CK		533 to 1066	(VDD2 / 2) + 0.220	Note 3	V	1, 2
		400	(VDD2 / 2) + 0.300			
Single-ended low-level for strobes	VSEL(AC)	533 to 1066	Note 3	(VDDQ / 2) – 0.220	V	1, 2
		400		(VDDQ / 2) – 0.300		
Single-ended low-level for CK, /CK		533 to 1066	Note 3	(VDD2 / 2) – 0.220	V	1, 2
		400		(VDD2 / 2) – 0.300		

Notes: 1. For CK, /CK use VSEH/VSEL(AC) of CA; for strobes (DQS0, /DQS0, DQS1, /DQS1, DQS2, /DQS2, DQS3, /DQS3) use VIH/VIL(AC) of DQs.
2. VIH(AC)/VIL(AC) for DQs is based on VREFDQ; VSEH(AC)/VSEL(AC) for CA is based on VREFCA; if a reduced Achigh or AC-low level is used for a signal group, then the reduced level applies also here
3. These values are not defined, however the single-ended signals CK, /CK, DQS0, /DQS0, DQS1, /DQS1, DQS2, /DQS2, DQS3, /DQS3 need to be within the respective limits (VIH(DC) max, VIL(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot Specifications" , please refer to JESD209-2F standard.

4.3.4 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, /CK and DQS, /DQS) must meet the requirements in Table 28. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.

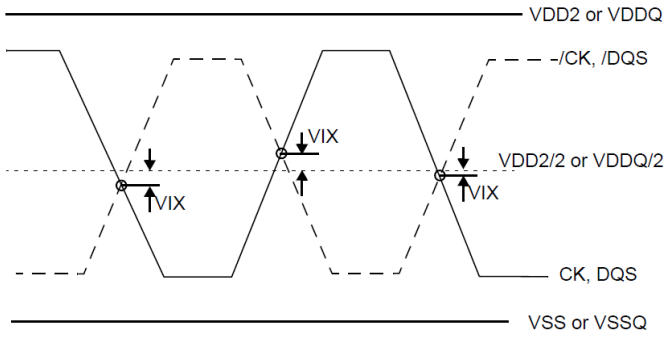


Figure 22 — VIX Definition

Table 28 Cross Point Voltage for Differential Input Signals (CK, DQS)

Parameter	Symbol	min.	max.	Unit	Note
Differential Input Cross Point Voltage relative to VDD2/2 for CK, /CK	VIXCA	-120	120	mV	1, 2
Differential Input Cross Point Voltage relative to VDDQ/2 for DQS, /DQS	VIXDQ	-120	120	mV	1, 2

Notes: 1. The typical value of VIX(AC) is expected to be about 0.5 × VDD of the transmitting device, and VIX(AC) is expected to track variations in VDD. VIX(AC) indicates the voltage at which differential input signals must cross.
2. For CK and /CK, VREF = VREFCA(DC). For DQS and /DQS, VREF = VREFDQ(DC).

AC and DC Output Measurement Levels

4.3.4.1 Single Ended AC and DC Output Levels

Table 29 shows the output levels used for measurements of single ended signals.

Table 29 Single-ended AC and DC Output Levels

Parameter	Symbol		Value	Unit	Note
DC output high measurement level (for IV curve linearity)	VOH(DC)		0.9 × VDDQ	V	1
DC output low measurement level (for IV curve linearity)	VOL(DC)		0.1 × VDDQ	V	2
AC output high measurement level (for output slew rate)	VOH(AC)		VREFDQ + 0.12	V	
AC output low measurement level (for output slew rate)	VOL(AC)		VREFDQ – 0.12	V	
Output Leakage current (DQ, DM, DQS, /DQS) (DQ, DQS, /DQS are disabled; 0V . VOUT . VDDQ)	IOZ	min.	-5	µA	
		max.	5	µA	
Delta RON between pull-up and pull-down for DQ/DM	MMPUPD	min.	-15	%	
		max.	15	%	

Notes: 1. IOH = -0.1mA. 2.IOL = 0.1mA.

4.3.4.2 Differential AC and DC Output Levels

Table 30 shows the output levels used for measurements of differential signals.

Table 30 Differential AC and DC Output Levels

Parameter	Symbol	Value	Unit	Note
AC differential output high measurement level (for output SR)	VOHdiff(AC)	+0.2 × VDDQ	V	
AC differential output low measurement level (for output SR)	VOLdiff(AC)	-0.2 × VDDQ	V	

4.3.4.3 Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC) for single ended signals as shown in Table 31 and Figure 16.

Table 31 Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Single-ended output slew rate for rising edge	VOL(AC)	VOH(AC)	[VOH(AC) – VOL(AC)] / DeltaTRse
Single-ended output slew rate for falling edge	VOH(AC)	VOL(AC)	[VOH(AC) – VOL(AC)] / DeltaTFse

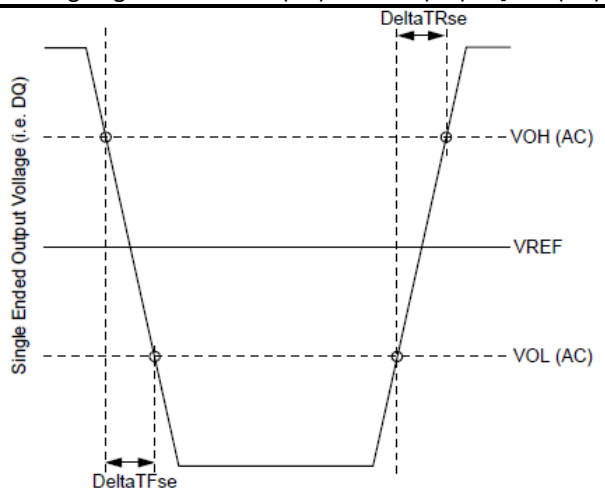


Figure 16 — Single Ended Output Slew Rate Definition

Table 32 Output Slew Rate (single-ended)

Parameter	Symbol	min.	max.	Unit
Single-ended Output Slew Rate (RON = 40Ω ± 30%)	SRQse	1.5	3.5	V/ns
Single-ended Output Slew Rate (RON = 60Ω ± 30%)	SRQse	1.0	2.5	V/ns
Output slew-rate matching Ratio (Pull-up to Pull-down)		0.7	1.4	

Remark: SR: Slew Rate, Q: Query Output (like in DQ, which stands for Data-in, Query-Output), se: Single-ended Signals

Notes: 1. Measured with output reference load.

2. The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pulldown drivers due to process variation.
3. The output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC).
4. Slew rates are measured under normal SSO conditions, with 1/2 of DQ signals per data byte driving logic high and 1/2 of DQ signals per data byte driving logic low.

4.3.5 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in Table 33 and Figure 17.

Table 33 Differential Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential output slew rate for rising edge	VOLdiff(AC)	VOHdiff(AC)	[VOHdiff(AC) – VOLdiff(AC)] / DeltaTRdiff
Differential output slew rate for falling edge	VOHdiff(AC)	VOLdiff(AC)	[VOHdiff(AC) – VOLdiff(AC)] / DeltaTFdiff

Note: 1. Output slew rate is verified by design and characterization, and may not be subject to production test.

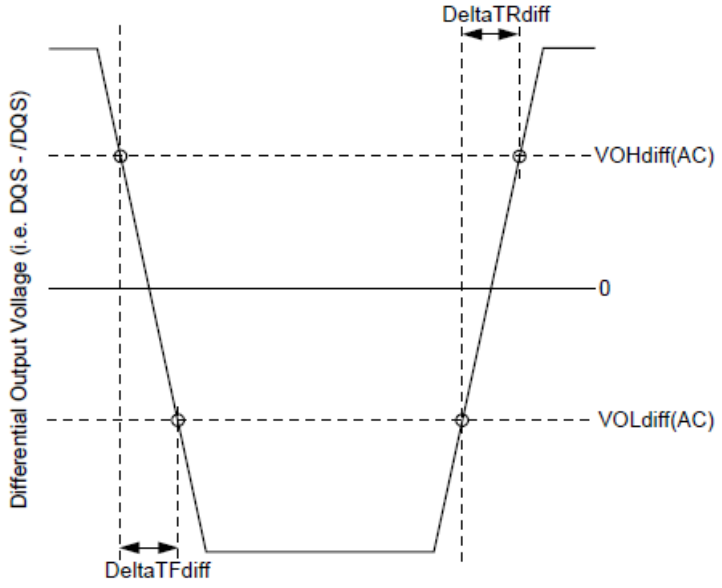


Figure 17 — Differential Output Slew Rate Definition

Table 34 Differential Output Slew Rate

Parameter	Symbol	min.	max.	Unit
Differential Output Slew Rate (RON = 40Ω ± 30%)	SRQdiff	3.0	7.0	V/ns
Differential Output Slew Rate (RON = 60Ω ± 30%)	SRQdiff	2.0	5.0	V/ns

Remark: SR: Slew Rate, Q: Query Output (like in DQ, which stands for Data-in, Query-Output), diff: Differential Signals

Notes: 1. Measured with output reference load.
2. The output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC).
3. Slew rates are measured under normal SSO conditions, with 1/2 of DQ signals per data byte driving logic high and 1/2 of DQ signals per data byte driving logic low.

4.3.6 Overshoot and Undershoot Specifications

Table 35 AC Overshoot/Undershoot Specification

Parameter		1066	933	800	667	533	400	Unit
Maximum peak amplitude allowed for overshoot area.	Max.			0.35				V
Maximum peak amplitude allowed for undershoot area.	Max.			0.35				V
Maximum overshoot area above VDD*1 .	max.	0.15	0.17	0.20	0.24	0.30	0.40	V-ns
Maximum undershoot area below VSS*2	max.	0.15	0.17	0.20	0.24	0.30	0.40	V-ns

Notes: 1. For CA0 – CA9, CK, /CK, /CS, and CKE, VDD stands for VDD2. For DQ, DM, DQS, and /DQS, VDD stands for VDDQ.
2. For CA0 – CA9, CK, /CK, /CS, and CKE, VSS stands for VSS. For DQ, DM, DQS, and /DQS, VSS stands for VSSQ.
3. Values are referenced from actual VDDQ, VDD2, VSSQ, and VSS levels.

4.3.6.1 RONPU and RONPD Characteristics with ZQ Calibration

Output driver impedance RON is defined by the value of the external reference resistor RZQ. Nominal RZQ is 240Ω.

4.3.6.2 RONPU and RONPD Characteristics without ZQ Calibration

Output driver impedance RON is defined by design and characterization as default setting.

4.4. Electrical Specifications

4.4.1. DC Characteristics 1 (For 4Gb)

(TJ = -15°C to +80°C, VDD1 = 1.70V to 1.95V, VDD2, VDDQ = 1.14V to 1.30V)

Table 36 IDD Specification Parameters and Operating Conditions

Symbol	Power Supply	1066	800	Unit	Parameter/Condition
		max.	max.		
IDD0_1	VDD1	8	8	mA	**Operating one bank active-pecharge current:** tCK = tCK(avg)min; tRC = tRCmin; CKE is HIGH; /CS is HIGH between valid commands; CA bus inputs are SWITCHING; Data bus inputs are STABLE
IDD0_2	VDD2	50	45	mA	
IDD0_IN	VDDQ	0.6	0.6	mA	
IDD2P_1	VDD1	1	1	mA	**Idle power-down standby current:** tCK = tCK(avg)min; CKE is LOW; /CS is HIGH; All banks idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE
IDD2P_2	VDD2	2.25	2.25	mA	
IDD2P_IN	VDDQ	0.2	0.2	mA	
IDD2PS_1	VDD1	1	1	mA	**Idle power-down standby current with clock stop:** CK = LOW, /CK = HIGH; CKE is LOW; /CS is HIGH; All banks idle; CA bus inputs are STABLE; Data bus inputs are STABLE
IDD2PS_2	VDD2	2.25	2.25	mA	
IDD2PS_IN	VDDQ	0.2	0.2	mA	
IDD2N_1	VDD1	0.6	0.6	mA	**Idle non power-down standby current:** tCK = tCK(avg)min; CKE is HIGH; /CS is HIGH; All banks idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE
IDD2N_2	VDD2	13	11	mA	
IDD2N_IN	VDDQ	0.6	0.6	mA	
IDD2NS_1	VDD1	0.6	0.6	mA	**Idle non power-down standby current with clock stop:** CK = LOW, /CK = HIGH; CKE is HIGH; /CS is HIGH; All banks idle; CA bus inputs are STABLE; Data bus inputs are STABLE
IDD2NS_2	VDD2	6	6	mA	
IDD2NS_IN	VDDQ	0.6	0.6	mA	
IDD3P_1	VDD1	0.8	0.8	mA	**Active power-down standby current:** tCK = tCK(avg)min; CKE is LOW; /CS is HIGH; One bank active; CA bus inputs are SWITCHING; Data bus inputs are STABLE
IDD3P_2	VDD2	5	5	mA	
IDD3P_IN	VDDQ	0.1	0.1	mA	
IDD3PS_1	VDD1	0.8	0.8	mA	**Active power-down standby current with clock stop:** CK = LOW, /CK = HIGH; CKE is LOW; /CS is HIGH; One bank active; CA bus inputs are STABLE; Data bus inputs are STABLE
IDD3PS_2	VDD2	5	5	mA	
IDD3PS_IN	VDDQ	0.1	0.1	mA	
IDD3N_1	VDD1	1.2	1.2	mA	**Active non power-down standby current:** tCK = tCK(avg)min; CKE is HIGH; /CS is HIGH; One bank active; CA bus inputs are SWITCHING; Data bus inputs are STABLE
IDD3N_2	VDD2	19	17	mA	
IDD3N_IN	VDDQ	0.6	0.6	mA	

IDD3NS_1	VDD1	1.2	1.2	mA	**Active non power-down standby current with clock stop:** CK = LOW, /CK = HIGH; CKE is HIGH; /CS is HIGH; One bank active; CA bus inputs are STABLE; Data bus inputs are STABLE
IDD3NS_2	VDD2	12	12	mA	
IDD3NS_IN	VDDQ	0.6	0.6	mA	

Table 37 IDD Specification Parameters and Operating Conditions (cont'd)

Symbol	Power Supply	1066 max.	800 max.	Unit	Parameter/Condition
IDD4R_1	VDD1	2	2	mA	**Operating burst read current:** tCK = tCK(avg)min; /CS is HIGH between valid commands; One bank active; BL = 4; RL = Rlmin; CA bus inputs are SWITCHING; 50% data change each burst transfer; Values in parenthesis are for x16 bits;
IDD4R_2	VDD2	160	130	mA	
IDD4W_1	VDD1	2	2	mA	**Operating burst write current:** tCK = tCK(avg)min; /CS is HIGH between valid commands; One bank active; BL = 4; WL = Wlmin; CA bus inputs are SWITCHING; 50% data change each burst transfer; Values in parenthesis are for x16 bits;
IDD4W_2	VDD2	150	120	mA	
IDD4W_IN	VDDQ	1	1	mA	
IDD5_1	VDD1	20	20	mA	**All Bank Auto Refresh Burst current:** tCK = tCK(avg)min; CKE is HIGH between valid commands; tRC = tRFCabmin; Burst refresh; CA bus inputs are SWITCHING; Data bus inputs are STABLE;
IDD5_2	VDD2	120	120	mA	
IDD5_IN	VDDQ	0.6	0.6	mA	
IDD5AB_1	VDD1	2	2	mA	**All Bank Auto Refresh Average current:** tCK = tCK(avg)min; CKE is HIGH between valid commands; tRC = tREFI; CA bus inputs are SWITCHING; Data bus inputs are STABLE;
IDD5AB_2	VDD2	16	15	mA	
IDD5AB_IN	VDDQ	0.6	0.6	mA	
IDD5PB_1	VDD1	2	2	mA	**Per Bank Auto Refresh Average current:** tCK = tCK(avg)min; CKE is HIGH between valid commands; tRC = tREFI/8; CA bus inputs are SWITCHING; Data bus inputs are STABLE;
IDD5PB_2	VDD2	16	15	mA	
IDD5PB_IN	VDDQ	0.6	0.6	mA	

Notes: 1. IDD values published are the maximum of the distribution of the arithmetic mean.

0. IDD current specifications are tested after the device is properly initialized.

Table 38 IDD6 Full and Partial Array Self-Refresh Current

Parameter		Symbol	Value	Unit	Condition
Self-Refresh Current +45°C ≦ TJ ≦ +80°C	Full Array	IDD6_1	1800	µA	CK = LOW, /CK = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE;
		IDD6_2	6400	µA	
		IDD6_IN	24	µA	

Note: 1. IDD values published are the maximum of the distribution of the arithmetic mean.

4.4.3. Pin Capacitance (For 4Gb)

(TA = +25°C, VDD1 = 1.70V to 1.95V, VDD2, VDDQ = 1.14V to 1.30V)

Table 39 Input/Output Capacitance

Parameter	Symbol	min.	max.	Unit	Note
Input capacitance, CK and /CK	CCK	1.0	2.0	pF	1, 2
Input capacitance delta, CK and /CK	CDCK	0	0.2	pF	1, 2, 3
Input capacitance, all other input-only pins	CI	1.0	2.0	pF	1, 2, 4
Input capacitance delta, all other input-only pins	CDI	-0.4	0.4	pF	1, 2, 5
Input/output capacitance, DQ, DM, DQS, /DQS	CIO	1.25	2.5	pF	1, 2, 6, 7
Input/output capacitance delta, DQS, /DQS	CDDQS	0	0.25	pF	1, 2, 7, 8
Input/output capacitance delta, DQ, DM	CDIO	-0.5	0.5	pF	1, 2, 7, 9
Input/output capacitance ZQ Pin	CZQ	0	2.5	pF	1, 2

Notes: 1. This parameter applies to die device only (does not include package capacitance).
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS, VSSQ applied and all other pins floating.
3. Absolute value of CCK – C/CK.
4. CI applies to /CS, CKE, CA0 – CA9.
5. CDI = CI – 0.5 × (CCK + C/CK)
6. DM loading matches DQ and DQS.
7. MR3 I/O configuration DS OP3-OP0 = 0001B (34.3 Ω typical)
8. Absolute value of CDQS and C/DQS.
9. CDIO = CIO – 0.5 × (CDQS + C/DQS) in byte-lane.

4.4.4. AC Characteristics

(TJ = -15°C to +80°C, VDD1 = 1.70V to 1.95V, VDD2, VDDQ = 1.14V to 1.30V)

Table 40 AC Characteristics Table[*6]

Parameter	Symbol	min. max.	min. tCK[*9]	1066	933	800	667	533	400	Unit
Max. Frequency[*4]			—	533	466	400	333	266	200	MHz
Clock Timing										
Average Clock Period	tCK(avg)	min.	—	1.875	2.15	2.5	3	3.75	5	ns
		max.	—	100						ns
Average high pulse width	tCH(avg)	min.	—	0.45						tCK (avg)
		max.	—	0.55						
Average low pulse width	tCL(avg)	min.	—	0.45						tCK (avg)
		max.	—	0.55						
Absolute Clock Period	tCK(abs)	min.	—	tCK(avg)(min.) + tJIT(per)(min.)						ps
Absolute clock HIGH pulse width (with allowed jitter)	tCH(abs), allowed	min.	—	0.43						tCK (avg)
		max.	—	0.57						
Absolute clock LOW pulse width (with allowed jitter)	tCL(abs), allowed	min.	—	0.43						tCK (avg)
		max.	—	0.57						
Clock Period Jitter (with allowed jitter)	tJIT(per), allowed	min.	—	-90	-95	-100	-110	-120	-140	ps
		max.	—	90	95	100	110	120	140	
Maximum Clock Jitter between two consecutive clock cycles (with allowed jitter)	tJIT(cc), allowed	max.	—	180	190	200	220	240	280	ps
Duty cycle Jitter (with allowed jitter)	tJIT(duty), allowed	min.	—	min((tCH(abs),min – tCH(avg),min), (tCL(abs),min – tCL(avg),min)) × tCK(avg)						ps
		max.	—	max((tCH(abs),max – tCH(avg),max), (tCL(abs),max – tCL(avg),max)) × tCK(avg)						
Cumulative error across 2 cycles	tERR(2per), allowed	min.	—	-132	-140	-147	-162	-177	-206	ps
		max.	—	132	140	147	162	177	206	
Cumulative error across 3 cycles	tERR(3per), allowed	min.	—	-157	-166	-175	-192	-210	-245	ps
		max.	—	157	166	175	192	210	245	
Cumulative error across 4 cycles	tERR(4per), allowed	min.	—	-175	-185	-194	-214	-233	-272	ps
		max.	—	175	185	194	214	233	272	
Cumulative error across 5 cycles	tERR(5per), allowed	min.	—	-188	-199	-209	-230	-251	-293	ps
		max.	—	188	199	209	230	251	293	
Cumulative error across 6 cycles	tERR(6per),	min.	—	-200	-211	-222	-244	-266	-311	ps

	allowed	max.	—	200	211	222	244	266	311	
Cumulative error across 7 cycles	tERR(7per), allowed	min.	—	-209	-221	-232	-256	-279	-325	ps
		max.	—	209	221	232	256	279	325	
Cumulative error across 8 cycles	tERR(8per), allowed	min.	—	-217	-229	-241	-266	-290	-338	ps
		max.	—	217	229	241	266	290	338	
Cumulative error across 9 cycles	tERR(9per), allowed	min.	—	-224	-237	-249	-274	-299	-349	ps
		max.	—	224	237	249	274	299	349	
Cumulative error across 10 cycles	tERR(10per), allowed	min.	—	-231	-244	-257	-282	-308	-359	ps
		max.	—	231	244	257	282	308	359	
Cumulative error across 11 cycles	tERR(11per), allowed	min.	—	-237	-250	-263	-289	-316	-368	ps
		max.	—	237	250	263	289	316	368	
Cumulative error across 12 cycles	tERR(12per), allowed	min.	—	-242	-256	-269	-296	-323	-377	ps
		max.	—	242	256	269	296	323	377	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper), allowed	min.	—	tERR(nper),allowed,min. = (1 + 0.68ln(n)) × tJIT(per),allowed,min.						
		max.	—	tERR(nper),allowed,max. = (1 + 0.68ln(n)) × tJIT(per),allowed,max.						
Read Parameters										
DQS output access time from CK, /CK	tDQSCK	min.	—	2500						ps
		max.	—	5500						
DQSCK Delta Short[*15]	tDQSCKDS	max.	—	330	380	450	540	670	900	ps
DQSCK Delta Medium[*16]	tDQSCKDM	max.	—	680	780	900	1050	1350	1800	ps
DQSCK Delta Long[*17]	tDQSCKDL	max.	—	920	1050	1200	1400	1800	2400	ps
DQS – DQ skew	tDQSQ	max.	—	200	220	240	280	340	400	ps
Data hold skew factor	tQHS	max.	—	230	260	280	340	400	480	ps
DQS Output High Pulse Width	tQSH	min.	—	tCH(abs) – 0.05						tCK (avg)
DQS Output Low Pulse Width	tQSL	min.	—	tCL(abs) – 0.05						tCK (avg)
Data Half Period	tQHP	min.	—	min(tQSH, tQSL)						tCK (avg)
DQ / DQS output hold time from DQS	tQH	min.	—	tQHP – tQHS						ps
Read preamble*12,[*13]	tRPRE	min.	—	0.9						tCK (avg)
Read postamble*12,[*14]	tRPST	min.	—	tCL(abs) – 0.05						tCK (avg)
DQS low-Z from clock[*12]	tLZ(DQS)	min.	—	tDQSCK(min.) – 300						ps

DQ low-Z from clock[*12]	tLZ(DQ)	min.	—	tDQSCK(min.) –(1.4 × tQHS(max.))						ps
DQS high-Z from clock[*12]	tHZ(DQS)	max.	—	tDQSCK(max.) – 100						ps
DQ high-Z from clock[*12]	tHZ(DQ)	max.	—	tDQSCK(max.) +(1.4 × tDQSQ(max.))						ps
Write Parameters[*11]										
DQ and DM input hold time (VREF based)	tDH	min.	—	210	235	270	350	430	480	ps
DQ and DM input setup time (VREF based)	tDS	min.	—	210	235	270	350	430	480	ps
DQ and DM input pulse width	tDIPW	min.	—	0.35						tCK (avg)
Write command to 1st DQS latching transition	tDQSS	min.	—	0.75						tCK (avg)
		max.	—	1.25						
DQS input high-level width	tDQSH	min.	—	0.4						tCK (avg)
DQS input low-level width	tDQSL	min.	—	0.4						tCK (avg)
DQS falling edge to CK setup time	tDSS	min.	—	0.2						tCK (avg)
DQS falling edge hold time from CK	tDSH	min.	—	0.2						tCK (avg)
Write postamble	tWPST	min.	—	0.4						tCK (avg)
Write preamble	tWPRE	min.	—	0.35						tCK (avg)
CKE Input Parameters										
CKE min. pulse width (high and low pulse width)	tCKE	min.	3	3						tCK (avg)
CKE input setup time	tISCKE*2	min.	—	0.25						tCK (avg)
CKE input hold time	tIHCKE*3	min.	—	0.25						tCK (avg)
Command Address Input Parameters[*11]										
Address and control input setup time (VREF based)	tIS*1	min.	—	220	250	290	370	460	600	ps
Address and control input hold time (VREF based)	tIH*1	min.	—	220	250	290	370	460	600	ps
Address and control input pulse width	tIPW	min.	—	0.40						tCK (avg)
Boot Parameters (10 MHz – 55 MHz)[*5,*7,*8]										
Clock Cycle Time	tCKb	max.	—	100						ns
		min.	—	18						
CKE Input Setup Time	tISCKEb	min.	—	2.5						ns
CKE Input Hold Time	tIHCKEb	min.	—	2.5						ns

Address & Control Input Setup Time	tISb	min.	—	1150						ps
Address & Control Input Hold Time	tIHb	min.	—	1150						ps
DQS Output Data Access Time fromCK, /CK	tDQSCKb	min.	—	2.0						ns
		max.	—	10.0						
Data Strobe Edge to Ouput Data Edge tDQSQb – 1.2	tDQSQb	max.	—	1.2						ns
Data Hold Skew Factor	tQHSb	max.	—	1.2						ns
Mode Register Parameters										
Mode Register Write command period	tMRW	min.	5	5						tCK (avg)
Mode Register Read command period	tMRR	min.	2	2						tCK (avg)
DDR2 Mobile RAM Core Parameters[*9]										
Read Latency	RL	min.	3	8	7	6	5	4	3	tCK (avg)
Write Latency	WL	min.	1	4	4	3	2	2	1	tCK (avg)
ACTIVE to ACTIVE command period	tRC	min.	—	tRAS + tRPab (with all-bank Precharge) tRAS + tRPpb(with per-bank Precharge)						ns
CKE min. pulse width during Self-Refresh (low pulse width during Self-Refresh)	tCKESR	min.	3	15						ns
Self-refresh exit to next valid command delay	tXSR	min.	2	tRFCab + 10						ns
Exit power down to next valid command delay	tXP	min.	2	7.5						ns
CAS to CAS delay	tCCD	min.	2	2						tCK (avg)
Internal Read to Precharge command delay	tRTP	min.	2	7.5						ns
RAS to CAS Delay	tRCD	min.	3	18						ns
Row Precharge Time (single bank)	tRPpb	min.	3	18						ns
Row Precharge Time (all banks)	tRPab	min.	3	21						ns
Row Active Time	tRAS	min.	3	42						ns
		max.	—	70						µs
Write Recovery Time	tWR	min.	3	15						ns
Internal Write to Read Command Delay	tWTR	min.	2	7.5						ns
Active bank A to Active bank B	tRRD	min.	2	10						ns
Four Bank Activate Window	tFAW	min.	8	50						ns
Minimum Deep Power Down Time	tDPD	min.	—	500						µs
DDR2 Mobile RAM Refresh Requirement Parameters										

Refresh Window	tREFW	max.	—	32	ms
Required number of REFRESH commands	R	min.	—	8192	
Average time between REFRESH commands (for reference only)	tREFI	max.	—	3.9	µs
tREFIpb		max.	—	0.4875	µs
Refresh Cycle time	tRFCab	min.	—	130	ns
Per Bank Refresh Cycle time	tRFCpb	min.	—	60	ns
Burst Refresh Window = 4 × 8 × tRFCab	tREFBW	min.	—	4.16	µs
ZQ Calibration Parameters*9					
Initialization Calibration Time	tZQINIT	min.	—	1	µs
Long Calibration Time	tZQCL	min.	6	360	ns
Short Calibration Time	tZQCS	min.	6	90	ns
Calibration Reset Time	tZQRESET	min.	3	50	ns

Notes: 1. Input set-up/hold time for signal(CA0 – CA9, /CS).
2. CKE input setup time is measured from CKE reaching high/low voltage level to CK, /CK crossing.
3. CKE input hold time is measured from CK, /CK crossing to CKE reaching high/low voltage level.
4. Frequency values are for reference only. Clock cycle time (tCK) shall be used to determine device capabilities.
5. To guarantee device operation before the DDR2 Mobile RAM Device is configured a number of AC boot timing parameters are defined in the Table 40. Boot parameter symbols have the letter b appended, e.g. tCK during boot is tCKb.
6. Frequency values are for reference only. Clock cycle time (tCK or tCKb) shall be used to determine device capabilities.
7. The DDR2 Mobile RAM will set some Mode register default values upon receiving a RESET (MRW) command as specified in "Mode Register Definition" , please refer to JESD209-2F standard.
8. The output skew parameters are measured with Ron default settings into the reference load.
9. These parameters should be satisfied with both specification, analog (ns) value and min. tCK.
10. All AC timings assume an input slew rate of 1V/ns.
11. Read, Write, and Input Setup and Hold values are referenced to VREF.
12. For low-to-high and high-to-low transitions the timing reference will be at the point when the signal crosses VTT. tHZ and tLZ transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for tRPST, tHZ(DQS) and tHZ(DQ)), or begins driving (for tRPRE, tLZ(DQS), tLZ(DQ)). Figure 28 shows a method to calculate the point when device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

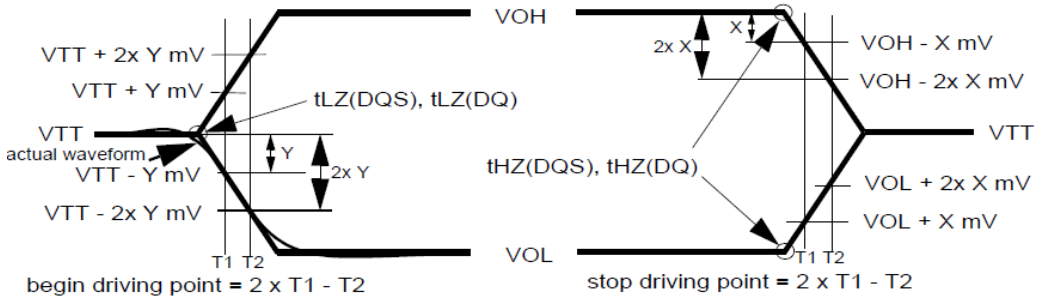


Figure 28 — tLZ and tHZ Method for Calculating Transition and Endpoints

The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single-ended. The timing parameters tRPRE and tRPST are determined from the differential signal DQS-/DQS.

13. Measured from the start driving of DQS – /DQS to the start driving the first rising strobe edge.
14. Measured from the from start driving the last falling strobe edge to the stop driving DQS – /DQS.
15. tDQSCKDS is the absolute value of the difference between any two tDQSCK measurements (within a byte lane) within a contiguous sequence of bursts within a 160ns rolling window. tDQSCKDS is not tested and is guaranteed by design. Temperature drift in the system is < 10°C/s. Values do not include clock jitter.
16. tDQSCKDM is the absolute value of the difference between any two tDQSCK measurements (within a byte lane) within a 1.6µs rolling window. tDQSCKDM is not tested and is guaranteed by design. Temperature drift in the system is < 10°C/s. Values do not include clock jitter.
17. tDQSCKDL is the absolute value of the difference between any two tDQSCK measurements (within a byte lane) within a 32ms rolling window. tDQSCKDL is not tested and is guaranteed by design. Temperature drift in the system is < 10°C/s. Values do not include clock jitter.

4.5. Power-up, initialization and Power-Off

DDR2 Mobile RAM Devices must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

4.5.3. Power Ramp and Device Initialization

The following sequence shall be used to power-up an DDR2 Mobile RAM Device. Unless specified otherwise, these steps are mandatory.

4.5.1.1 Power Ramp

While applying power (after Ta), CKE shall be held at a logic low level (≤ 0.2 × VDD2), all other inputs shall be between VILmin and VIHmax. The DDR2 Mobile RAM Device will only guarantee that outputs are in a high impedance state while CKE is held low.
On or before the completion of the power ramp (Tb) CKE must be held low.
DQ, DM, DQS and /DQS voltage levels must be between VSSQ and VDDQ during voltage ramp time to avoid latch-up. CK, /CK, /CS and CA inputs levels must be between VSS and VDD2 during voltage ramp up to avoid latch-up.

The following conditions apply:
Ta is the point where any power supply first reaches 300mV.
After Ta is reached, VDD1 must be greater than VDD2 – 200mV.
After Ta is reached, VDD1 and VDD2 must be greater than VDDQ – 200mV.
After Ta is reached, VREF must always be less than all other supply voltages.
The voltage difference between any of VSS and VSSQ pins may not exceed 100mV.
The above conditions apply between Ta and power-off (controlled or uncontrolled).
Tb is the point when all supply and reference voltages are within their respective min/max operating conditions.
For supply and reference voltage operating conditions.
Power ramp duration tINIT0 (Tb – Ta) must be no greater than 20ms.
Note: VDD2 is not present in some systems. Rules related to VDD2 in those cases do not apply.

Table 41 Timing Parameters for Initialization

Symbol	min.	max.	Unit	Comment
tINIT0	—	20	ms	Maximum Power Ramp Time
tINIT1	100	—	ns	Minimum CKE low time after completion of power ramp
tINIT2	5	—	tCK	Minimum stable clock before first CKE high
tINIT3	200	—	µs	Minimum Idle time after first CKE assertion
tINIT4	1	—	µs	Minimum Idle time after Reset command
tINIT5	—	10	µs	Maximum duration of Device Auto-Initialization
tZQINIT	1	—	µs	ZQ Initial Calibration
tCKb	18	100	ns	Clock cycle time during boot

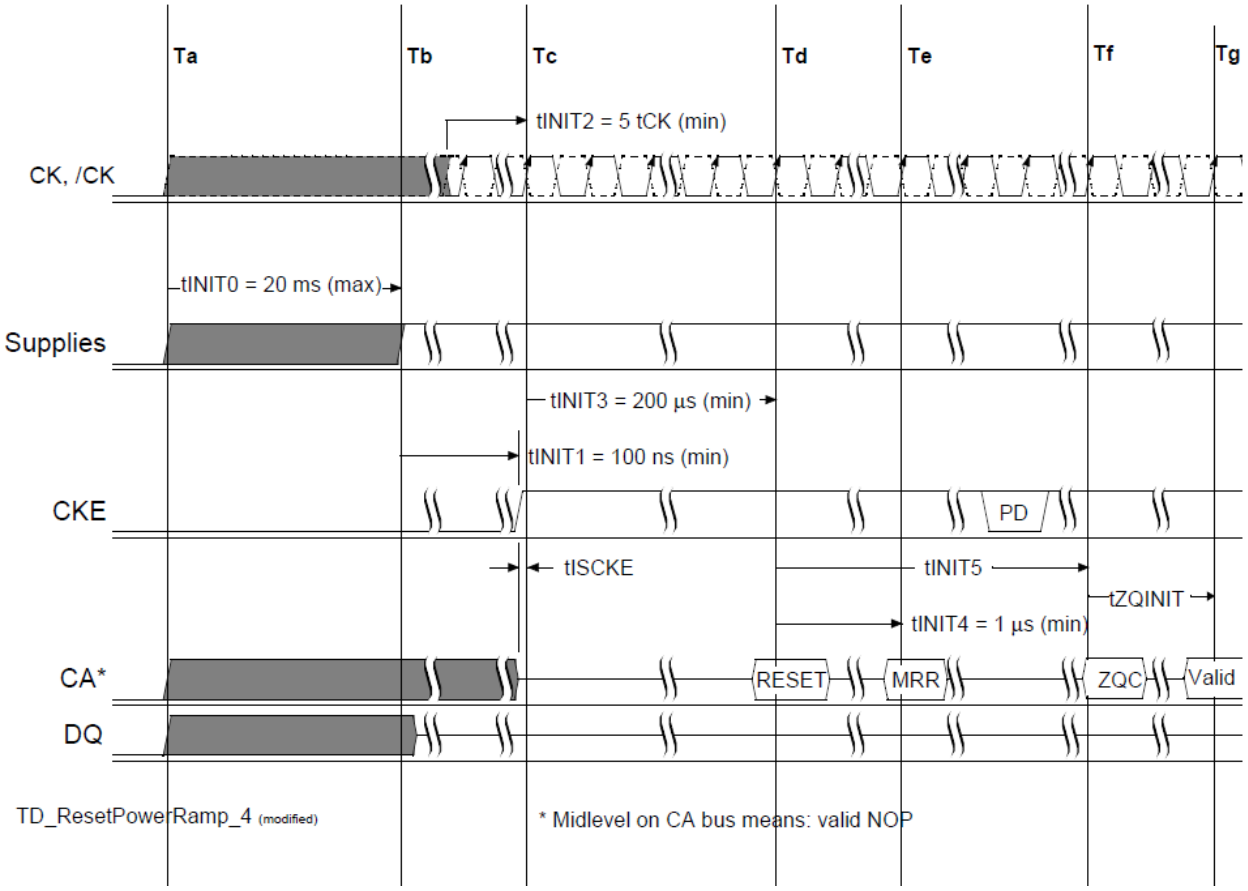


Figure 19 — Power Ramp and Initialization Sequence

4.5.4. Initialization After Reset (without Power Ramp):

If the RESET command is issued outside the power-up initialization sequence, the re-initialization procedure shall begin with step 3 (Td).

4.5.5. Power-Off Sequence

The following sequence shall be used to power-off the DDR2 Mobile RAM Device. Unless specified otherwise, these steps are mandatory.

While removing power, CKE shall be held at a logic low level (≤ 0.2 × VDD2), all other inputs shall be between VILmin and VIHmax. The DDR2 Mobile RAM Device will only guarantee that outputs are in a high impedance state while CKE is held low.

DQ, DM, DQS and /DQS voltage levels must be between VSSQ and VDDQ during power-off sequence to avoid latch-up.

CK, /CK, /CS and CA input levels must be between VSS and VDD2 during power-off sequence to avoid latch-up.

Tx is the point where any power supply decreases under its minimum value specified in the DC operating condition table.

Tz is the point where all power supplies are below 300mV. After Tz, the device is powered off.

The time between Tx and Tz (tPOFF) shall be less than 2s.

The following conditions apply:

Between Tx and Tz, VDD1 must be greater than VDD2 – 200mV.

Between Tx and Tz, VDD1 and VDD2 must be greater than VDDQ – 200mV.

Between Tx and Tz, VREF must always be less than all other supply voltages.

The voltage difference between any of VSS and VSSQ pins may not exceed 100mV.

For supply and reference voltage operating conditions.

Table 42 Timing Parameters for Power-Off

Symbol	min.	max.	Unit	Comment
tPOFF	—	2	s	Maximum Power-Off ramp time

4.6. Truth Tables

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the DDR2 Mobile RAM Device must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
Table 43 provides the command truth table.

Table 43 Command Truth Table

Command	SDR Command Pins			DDR CA pins (10)										
	CKE		/CS	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CK EDGE
	CK(n-1)	CK(n)												
MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	↑
				MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	↓
MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	↑
				MA6	MA7				X					↓
Refresh (per bank)	H	H	L	L	L	H	L				X			↑
									X					↓
Refresh (all bank)	H	H	L	L	L	H	H				X			↑
									X					↓
Enter Self-Refresh	H	L	L	L	L	H				X				↑
									X					↓
Activate (bank)	H	H	L	L	H	R8	R9	R10	R11	R12	BA0	BA1	BA2	↑
				R0	R1	R2	R3	R4	R5	R6	R7	R13	RFU	↓
Write (bank)	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
				AP[*3]	C3	C4	C5	C6	C7	C8	C9	RFU	RFU	↓
Read (bank)	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
				AP[*3]	C3	C4	C5	C6	C7	C8	C9	RFU	RFU	↓
Precharge (bank)	H	H	L	H	H	L	H	AB	X	X	BA0	BA1	BA2	↑
				X	X	X	X	X	X	X	X	X	X	↓
BST	H	H	L	H	H	L	L				X			↑
									X					↓
Enter Deep Power Down	H	L	L	H	H	L				X				↑
									X					↓

NOP	H	H	L	H	H	H	X		
							X		
Maintain PD, SREF, DPD(NOP)	L	L	L	H	H	H	X		
							X		
NOP	H	H	H				X		
							X		
Maintain PD, SREF, DPD(NOP)	L	L	H				X		
							X		
Enter Power Down	H	L	H				X		
							X		
Exit PD, SREF, DPD	L	H	H				X		
							X		

Notes: 1. All commands are defined by states of /CS, CA0, CA1, CA2, CA3, and CKE at the rising edge of the clock.
2. Bank addresses determine which bank is to be operated upon.
3. AP "high" during a READ or WRITE command indicates that an auto-precharge will occur to the bank associated with the READ or WRITE command.
4. "X" means "H or L (but a defined logic level)"
5. Self-refresh exit and Deep Power Down exit are asynchronous.
6. VREF must be between 0 and VDDQ during Self-Refresh and Deep Power Down operation.
7. Caxr refers to command/address bit "x" on the rising edge of clock.
8. Caxf refers to command/address bit "x" on the falling edge of clock.
9. /CS and CKE are sampled at the rising edge of clock.
10. The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.
11. RFU needs to input "H" or "L" (but a defined logic level).

4.7. Mode Register Definition

Each register is denoted as “R” if it can be read but not written and “W” if it can be written but not read. Mode Register Read command shall be used to read a register. Mode Register Write command shall be used to write a register.

Table 44 Mode Register Assignment

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link
0	00H	Device Info.	R	(RFU)			RZQI		(RFU)	DI	DAI	MR#0
1	01H	Device Feature 1	W	nWR (for AP)			WC	BT	BL			MR#1
2	02H	Device Feature 2	W	(RFU)					RL & WL			MR#2
3	03H	I/O Config-1	W	(RFU)					DS			MR#3
4	04H	Refresh Rate	R	TUF	(RFU)				Refresh Rate			MR#4
5	05H	Basic Config-1	R	Manufacturer ID								MR#5
6	06H	Basic Config-2	R	Revision ID1 (Die Revision)								MR#6
7	07H	Basic Config-3	R	Revision ID2 (RFU)								MR#7
8	08H	Basic Config-4	R	I/O width			Density			Type		MR#8
9	09H	Test Mode	W	Vendor-Specific Test Mode								
10	0AH	IO Calibration	W	Calibration Code								MR#10
11:15	0BH~0FH	(Reserved)		(RFU)								
16	10H	PASR_Bank	W	Bank Mask								MR#16
17	11H	PASR_Seg	W	Segment Mask								MR#17
18:19	12H~13H	(Reserved)		(RFU)								
32	20H	DQ Calibration Pattern A	R	See “DQ Calibration” of “DDR2 Mobile RAM General Functionality and Electrical Condition” datasheet.								MR#32
33:39	21H~27H	(Do Not Use)										
40	28H	DQ Calibration Pattern B	R	See “DQ Calibration” of “DDR2 Mobile RAM General Functionality and Electrical Condition” datasheet.								MR#40
41:47	29H~2FH	(Do Not Use)										
48:62	30H~3EH	(Reserved)		(RFU)								
63	3FH	Reset	W	X								MR#63
64:126	40H~7EH	(Reserved)		(RFU)								
127	7FH	(Do Not Use)										
128:190	80H~BEH	(Reserved)		(RFU)								
191	BFH	(Do Not Use)										
192:254	C0H~FEH	(Reserved)		(RFU)								
255	FFH	(Do Not Use)										

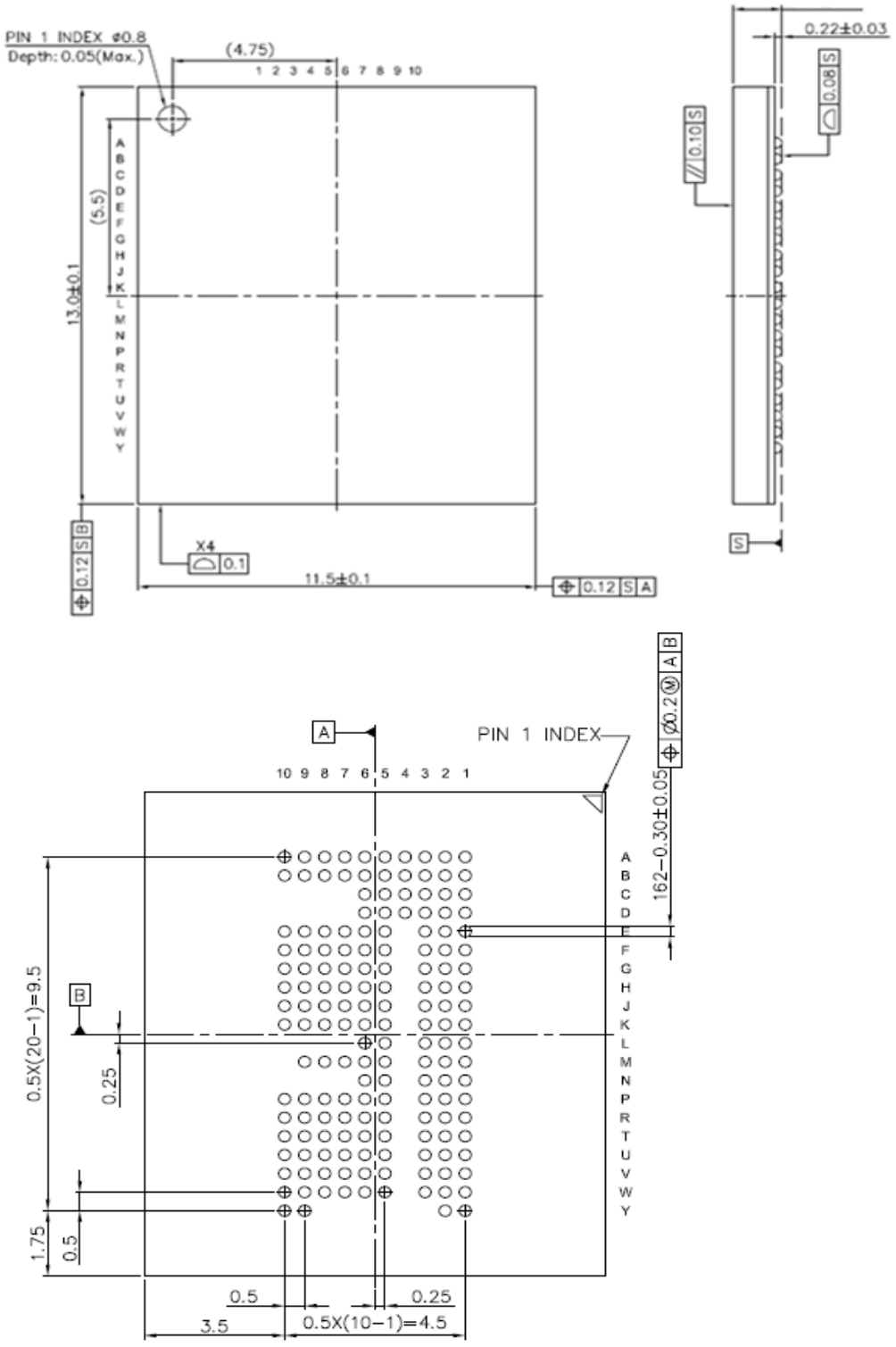
Notes: 1. RFU bits shall be set to ‘0’ during Mode Register writes.
2. RFU bits shall be read as ‘0’ during Mode Register reads.
3. All Mode Registers that are specified as RFU or write-only shall return undefined data when read and DQS, /DQS shall be toggled.
4. All Mode Registers that are specified as RFU shall not be written.
5. Writes to read-only registers shall have no impact on the functionality of the device.

MR#5_Basic Configuration 1 (MA<7:0> = 05H): Read-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Manufacturer ID OP<7:0> 00000011B (Elpida)							

5. Package Mechanical

5.1 162 ball FBGA 11.5 x 13.0 x (0.9mm ± 0.1mm, Max 1.0mm)



6. Ball Assignment

6.1 162 ball assignment

	1	2	3	4	5	6	7	8	9	10	
A	DNU	DNU	DAT0	DAT6	VDDi	DAT5	DAT3	VCC	DNU	DNU	A
B	DNU	VCC	DAT1	DAT7	CLK	DAT4	DAT2	VCCQ	VSS	DNU	B
C	RST_n	NC	VSSQ	NC	CMD	NC					C
D	NC	NC	NC	NC	NC	NC					D
E	VSS	NC	NC		VDD2	VDD1	DQ31	DQ29	DQ26	DNU	E
F	VDD1	LP2 VSS	ZQ1		LP2 VSS	LP2 VSSQ	VDDQ	DQ25	LP2 VSSQ	VDDQ	F
G	VSS	VDD2	ZQ0		VDDQ	DQ30	DQ27	DQS3	/DQS3	LP2 VSSQ	G
H	VSSCA	CA9	CA8		DQ28	DQ24	DM3	DQ15	VDDQ	LP2 VSSQ	H
J	VDDCA	CA6	CA7		LP2 VSSQ	DQ11	DQ13	DQ14	DQ12	VDDQ	J
K	VDD2	CA5	Vref(CA)		/DQS1	DQS1	DQ10	DQ9	DQ8	LP2 VSSQ	K
L	VDDCA	LP2 VSS	/CLK		DM1	VDDQ					L
M	LP2 VSSCA	NC	CLK		LP2 VSSQ	VDDQ	VDD2	LP2 VSS	VREF(DQ)		M
N	CKE0	CKE1	NC		DM0	VDDQ					N
P	CS0_n	CS1_n	NC		/DQS0	DQS0	DQ5	DQ6	DQ7	LP2 VSSQ	P
R	CA4	CA3	CA2		LP2 VSSQ	DQ4	DQ2	DQ1	DQ3	VDDQ	R
T	LP2 VSSCA	VDDCA	CA1		DQ19	DQ23	DM2	DQ0	VDDQ	LP2 VSSQ	T
U	LP2 VSS	VDD2	CA0		VDDQ	DQ17	DQ20	DQS2	/DQS2	LP2 VSSQ	U
V	VDD1	LP2 VSS	NC		LP2 VSS	LP2 VSSQ	VDDQ	DQ22	LP2 VSSQ	VDDQ	V
W	DNU	NC	NC		VDD2	VDD1	DQ16	DQ18	DQ21	DNU	W
Y	DNU	DNU							DNU	DNU	Y
	1	2	3	4	5	6	7	8	9	10	

Figure 20 – Top View–Ball Down

7. Revision History

Rev.	History	Date	Remark
1.0	Preliminary	Dec. / 2014	