Rev.3.0

Date: 2011/1/7

Product Functional Specification

65" Full HD Color TFT-LCD Module
Model Name: P645HW03 V0

() Preliminary Specification
(*) Final Specification

Note: This specification is subject to change without notice.

Contents

Record of Revision

Rev.	Data	Page	Items	New Description	Remark
0.0	2010/4/20		First Draft		
1.0	2010/0728	5	Total Power Consumption	440 => 403	
		7~20	3. Electrical Specification	New format with modified data highlighted in red	
		21	Response time	6.5 ms=>8 ms	
		25~26	Drawing	Front & Rear views in 1 frame=> Front & Rear views in separate frames	
2.0	2010/11/30	5	Display Colors	1073.4 M (10-bit) => 1073.7M (10-bit)	
		5	Total Power Consumption	403(typ.) => 396(typ.)	
		5	Add Note [2]		
		7	Power Supply Input Current	Max. TBD=>1.1	
		7	Power Consumption	Max. TBD=>13.2	
		7	Inrush Current	Max. TBD=> 4.5	
		15	Input Current	Min. 15.5=>15.2, Typ. 16.5=>16.2, Max. 17.5=>17.2	
		15	Input power	Min. 335=>365, Typ. 396=>389, Max. 431=>413	
		15	Operating frequency	Min. TBD=> 40, Max. TBD=>44	
		15	On/Off control voltage	ON: Max. 5.5=>5 OFF: Min 0=>-0.3	
		18	CN10 of Master board	S3B-ZR-SM3A-TF(JST) => CI4603M1HR0(Cvilux)	
		21	Color Coordinates	RED: TBD => Rx 0.64, Ry 0.33 Green: TBD=> Gx 0.29, Gy 0.6 Blue: TBD=> Bx 0.15, By 0.06	
3.0	2011/1/7	27	Reliability Test item 1	300hrs => 500hrs	
		27	Reliability Test item 2	300hrs => 500hrs	
		27	Reliability Test item 3	300hrs => 500hrs	
		27	Reliability Test item 4	300hrs => 500hrs	

1. General Description

This specification applies to the 65 inch Color TFT-LCD Module P645HW03 V0. This LCD module has a TFT active matrix type liquid crystal panel 1920x1080 pixels, and diagonal size of 64.5 inch. This module supports Full HD mode (non-interlace).

Each pixel is divided into Red, Green, and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined by 10-bit gray scale signal for each dot.

The P645HW03 V0 has been designed to apply the 10-bit 2-channel LVDS interface method. It is intended to support displays where high brightness, wide viewing angle, and high color depth are important.

The P645HW03 V0 is RoHS verified which can be distinguished on panel label.

◆ General Information

Items	Specification	Unit	Note
Active Screen Size	64.5	inches	Diagonal
Display Area	1428.48 (H) x 803.52 (V)	mm	
Outline Dimension	1482.4(V) x 862.0(H) x 58.9(D)	mm	With inverter
Driver Element	a-Si TFT active matrix		
Display Colors	1073.7M (10-bit)	colors	
Color Gamut	72	%	NTSC
Number of Pixels	1920 x 1080	pixel	
Pixel Arrangement	RGB vertical stripe		
Pixel Pitch	0.744	mm	
Display Mode	Transmissive, Normally Black		
Surface Treatment	Anti-glare, 3H		
Total Power Consumption	396(typ.)	W	include BLU & Signal
Life Time (minimum)	50,000	hours	[1]
RoHS	RoHS compliance		
Display Orientation	Portrait/Landscape enable		[2]

Note [1] The life is determined as the time at which luminance of the single lamp is 50% compared to that of initial value at the typical lamp current on condition of horizontally continuous operating at 25±2℃.

[2] The lamps are horizontal as the panel is arranged in portrait mode.

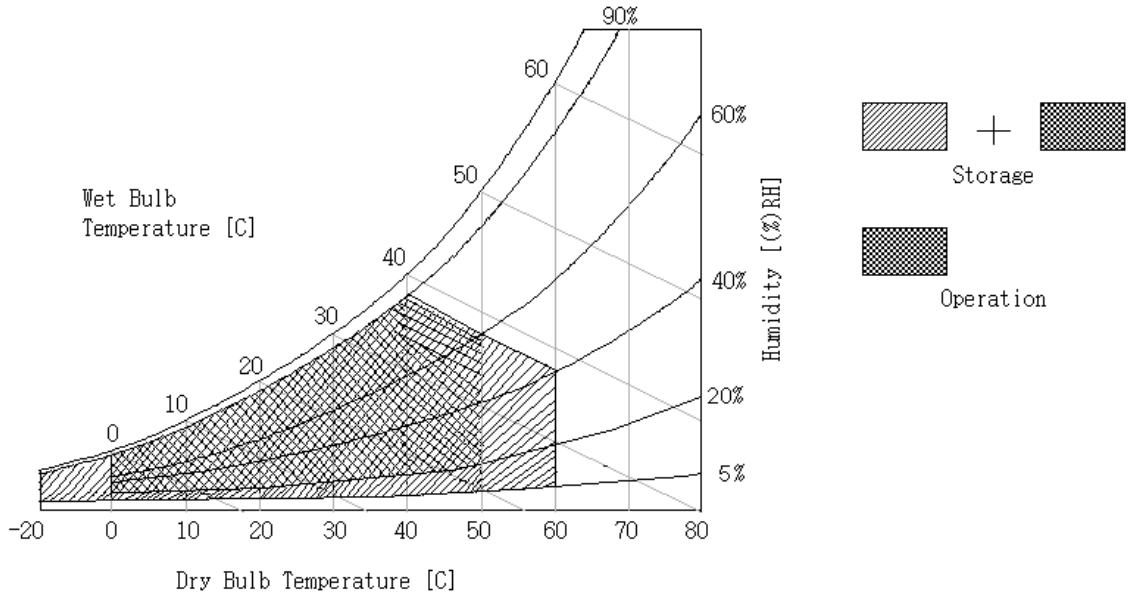
2. Absolute Maximum Ratings

The followings are maximum values which, if exceeded, may cause faulty operation or damage to the unit:

Item	Symbol	Min.	Max	Unit	Note
Logic/LCD Drive Voltage	V_{CC}	-0.3	+14.0	V	1
Input Voltage of Signal	V_{IN}	-0.3	+4.0	V	1
BLU Input Voltage	V_{DDB}	-0.3	+27.0	V	1
On/Off control voltage	V_{BLON}	-0.3	+5.5	V	1
Operating Temperature	T_{OP}	0	+50	℃	2
Operating Humidity	H_{OP}	10	90	%RH	2
Storage Temperature	T_{ST}	-20	+60	℃	2
Storage Humidity	H_{ST}	10	90	%RH	2
Open Lamp Voltage	V_{FB}	-0.3	+3.6	V	
Panel Surface Temperature	T_{SUR}	-	+65	℃	2

Note 1: If operating over spec. but under absolute maximum rating, duration must be < 50ms.

Note 2: Maximum Wet-Bulb should be 39℃ and no condensation. The relative humidity must not exceed 80% non-condensing at temperatures of 40℃ or less. At temperatures greater than 40℃, the wet bulb temperature must not exceed 39℃. When operate at low temperatures, the brightness of CCFL will drop and the life time of CCFL will be reduced.



3. Electrical Specification

The P645HW03 V0 requires two power inputs. One is employed to power the LCD electronics and to drive the TFT array and liquid crystal. The second input which powers the CCFL, is typically generated by an inverter.

3.1 Signal Electrical Characteristics

3.1.1: DC Characteristics

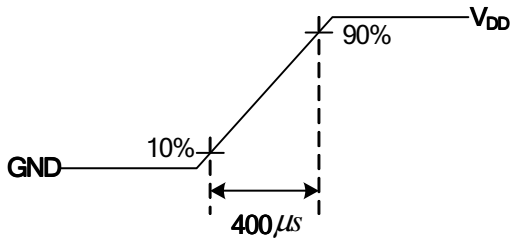
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max		
Power Supply Input Voltage		V_{DD}	10.8	12	13.2	V_{DC}	
Power Supply Input Current		I_{DD}	--	0.58	1.1	A	1
Power Consumption		P_C	--	6.96	13.2	Watt	1
Inrush Current		I_{RUSH}	--	--	4.5	A	2
LVDS Interface	Input Differential Voltage	$\|V_{ID}\|$	200	400	600	mV_{DC}	3
	Differential Input High Threshold Voltage	V_{TH}	+100	--	+300	mV_{DC}	3
	Differential Input Low Threshold Voltage	V_{TL}	-300	--	-100	mV_{DC}	3
	Input Common Mode Voltage	V_{ICM}	1.1	1.25	1.4	V_{DC}	3
CMOS Interface	Input High Threshold Voltage	V_{IH} (High)	2.7	--	3.3	V_{DC}	4
	Input Low Threshold Voltage	V_{IL} (Low)	0	--	0.6	V_{DC}	4

3.1.2: AC Characteristics

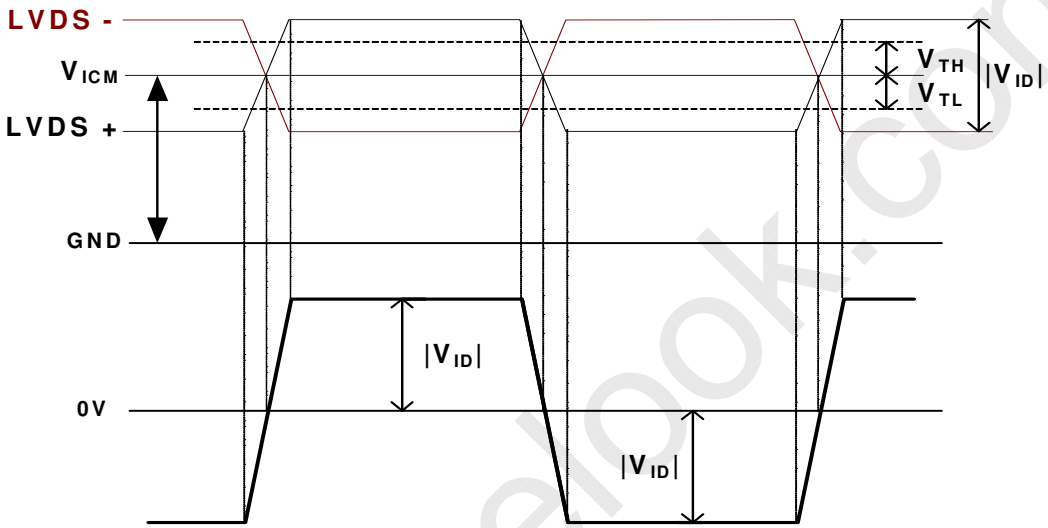
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max		
LVDS Interface	Receiver Clock : Spread Spectrum Modulation range	Fclk_ss	Fclk -3%	--	Fclk +3%	MHz	5
	Receiver Clock : Spread Spectrum Modulation frequency	Fss	30	--	200	KHz	5
	Receiver Data Input Margin	tRMG	-0.4	--	0.4	ns	6

Note :

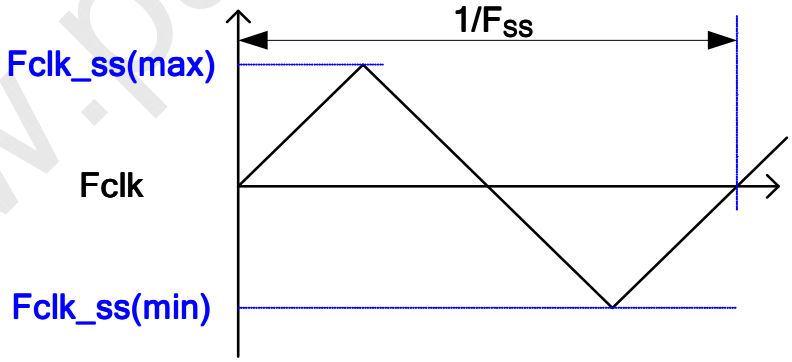
1. V_{DD} = 12.0V, Fv = 60Hz, Fclk= 82MHz , 25 ℃, Test Pattern : White Pattern
2. Measurement condition : Rising time = 400us



3. V_{ICM} = 1.25V

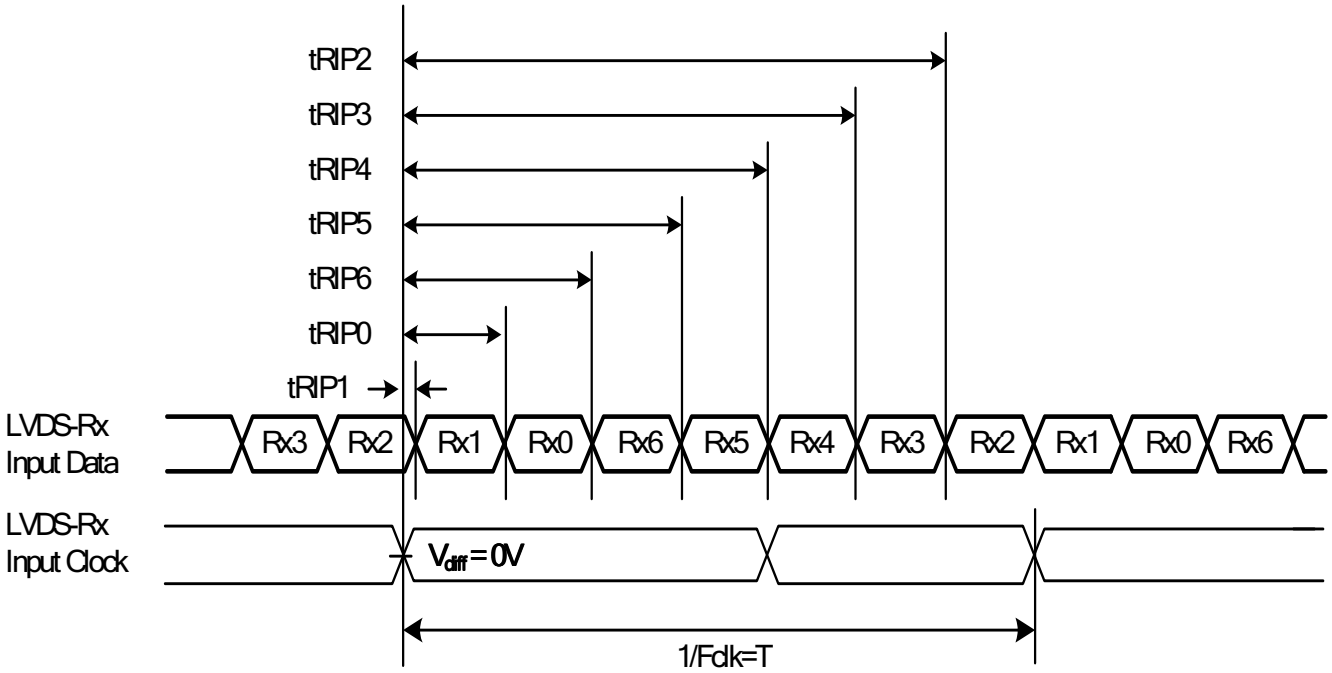


4. The measure points of V_{IH} and V_{IL} are in LCM side after connecting the System Board and LCM.
5. LVDS Receiver Clock SSCG (Spread spectrum clock generator) is defined as below figures



6. Receiver Data Input Margin

Parameter	Symbol	Rating			Unit	Note
		Min	Type	Max		
Input Clock Frequency	Fclk	Fclk (min)	--	Fclk (max)	MHz	**T=1/Fclk**
Input Data Position0	tRIP1	-|tRMG|	0	|tRMG|	ns	
Input Data Position1	tRIP0	T/7-|tRMG|	T/7	T/7+|tRMG|	ns	
Input Data Position2	tRIP6	2T/7-|tRMG|	2T/7	2T/7+|tRMG|	ns	
Input Data Position3	tRIP5	3T/7-|tRMG|	3T/7	3T/7+|tRMG|	ns	
Input Data Position4	tRIP4	4T/7-|tRMG|	4T/7	4T/7+|tRMG|	ns	
Input Data Position5	tRIP3	5T/7-|tRMG|	5T/7	5T/7+|tRMG|	ns	
Input Data Position6	tRIP2	6T/7-|tRMG|	6T/7	6T/7+|tRMG|	ns	



3.2 Signal Interface Connections

- LCD connector: FI-RE51S-HF (Manufactured by JAE)
- Mating connector: FI-RE51S-HL (Manufactured by JAE)

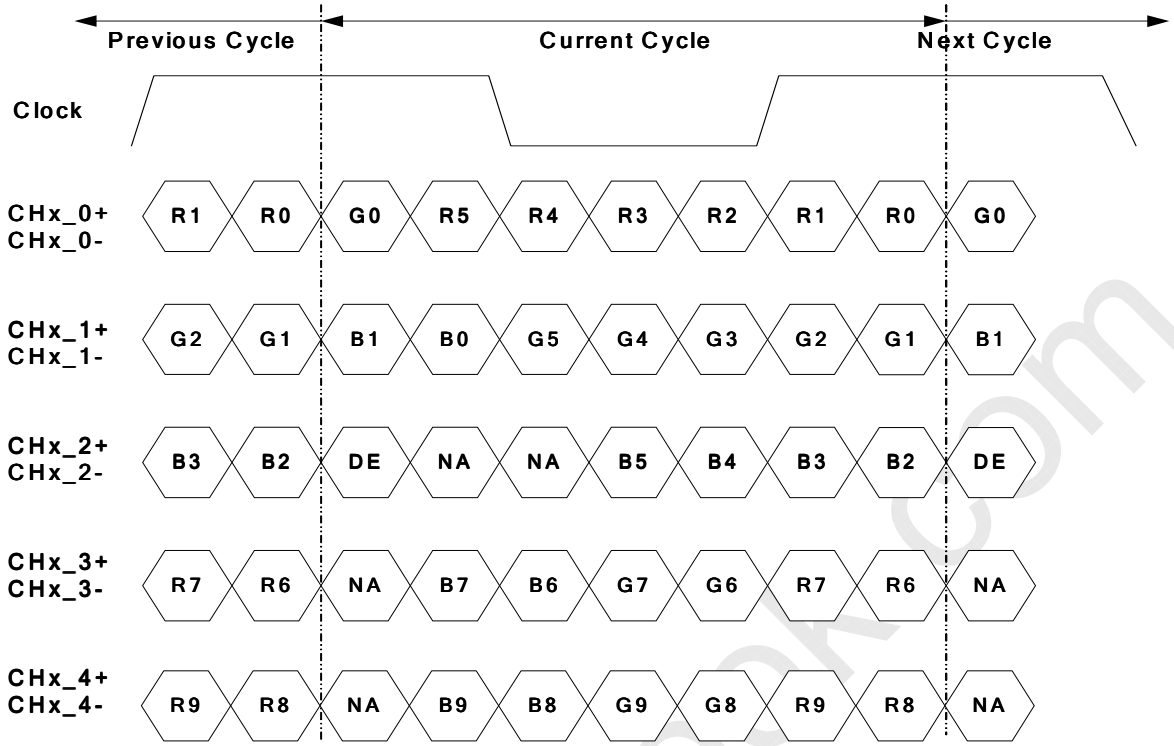
No.	Symbol	Description	No.	Symbol	Description
1	VCC	+12V Power Supply	27	RXEN1	LVDS Even pixel data input pair 1(-)
2	VCC	+12V Power Supply	28	RXEP1	LVDS Even pixel data input pair 1(+)
3	VCC	+12V Power Supply	29	RXEN2	LVDS Even pixel data input pair 2(-)
4	VCC	+12V Power Supply	30	RXEP2	LVDS Even pixel data input pair 2(+)
5	VCC	+12V Power Supply	31	GND	Ground
6	GND	Ground	32	RXENCLK	LVDS Even pixel clock input pair(-)
7	GND	Ground	33	RXEPCLK	LVDS Even pixel clock input pair(+)
8	GND	Ground	34	GND	Ground
9	GND	Ground	35	RXEN3	LVDS Even pixel data input pair 3(-)
10	RXON0	LVDS Odd pixel data input pair 0(-)	36	RXEP3	LVDS Even pixel data input pair 3(+)
11	RXOP0	LVDS Odd pixel data input pair 0(+)	37	RXEN4	LVDS Even pixel data input pair 4(-)
12	RXON1	LVDS Odd pixel data input pair 1(-)	38	RXEP4	LVDS Even pixel data input pair 4(+)
13	RXOP1	LVDS Odd pixel data input pair 1(+)	39	GND	Ground
14	RXON2	LVDS Odd pixel data input pair 2(-)	40	NC	No connected
15	RXOP2	LVDS Odd pixel data input pair 2(+)	41	NC	No connected
16	GND	Ground	42	NC	No connected
17	RXONCLK	LVDS Odd pixel clock input pair(-)	43	NC	No connected
18	RXOPCLK	LVDS Odd pixel clock input pair(+)	44	NC	No connected
19	GND	Ground	45	LVDSORD	Select LVDS data order: ● High or NC → NS ● Low → JEIDA
20	RXON3	LVDS Odd pixel data input pair 3(-)	46	Reserved	AUO Internal Use Only
21	RXOP3	LVDS Odd pixel data input pair 3(+)	47	Reserved	AUO Internal Use Only
22	RXON4	LVDS Odd pixel data input pair 4(-)	48	Reserved	AUO Internal Use Only
23	RXOP4	LVDS Odd pixel data input pair 4(+)	49	Reserved	AUO Internal Use Only
24	GND	Ground	50	Reserved	AUO Internal Use Only
25	RXEN0	LVDS Even pixel data input pair 0(-)	51	Reserved	AUO Internal Use Only
26	RXEP0	LVDS Even pixel data input pair 0(+)			

Note 1: All GND (ground) pins should be connected together and should also be connected to the LCD's metal frame.

Note 2: All V_{DD} (power input) pins should be connected together.

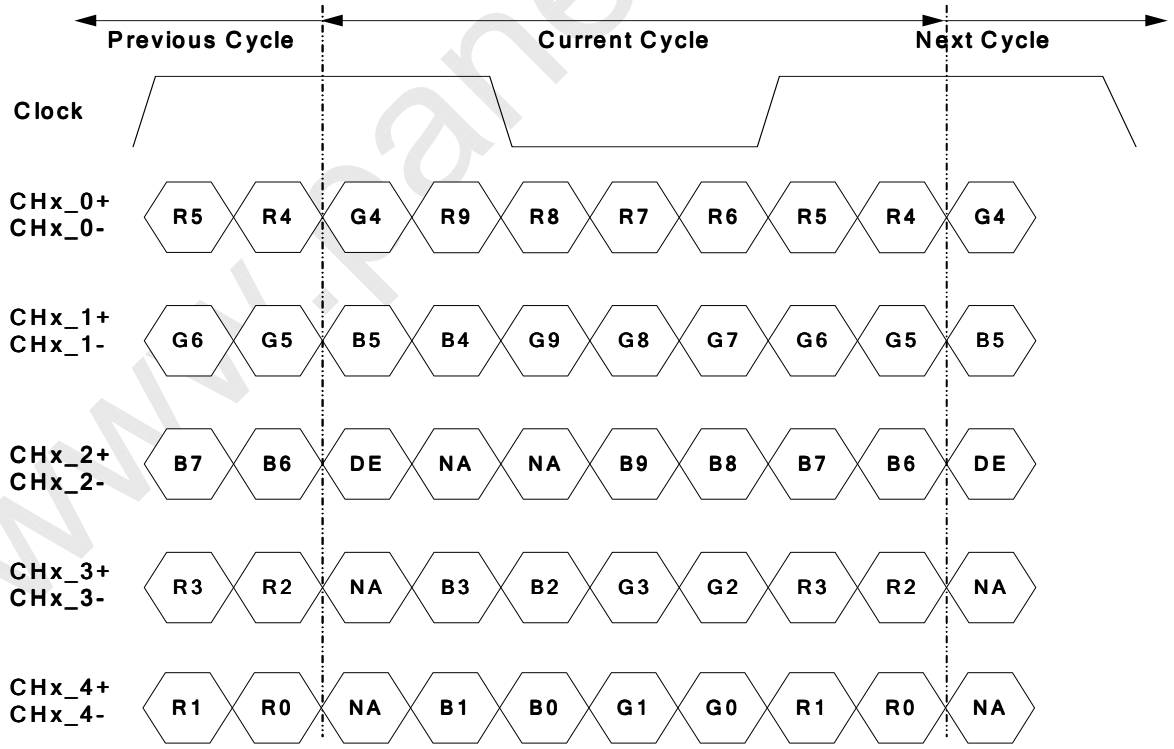
Note 3: All NC (no connection) pins should be open without voltage input.

◆ LVDS Option = Open/High(3.3V) → NS



Note: x = 1, 2, 3, 4…

◆ LVDS Option = Low(GND) → JEIDA



Note: x = 1, 2, 3, 4…

3.3 Signal Timing Specification

This is the signal timing required at the input of the user connector. All of the interface signal timing should be satisfied with the following specifications for its proper operation.

Timing Table (DE only Mode)

Signal	Item	Symbol	Min.	Typ.	Max	Unit
Vertical Section	Period	Tv	1090	1125	1480	Th
	Active	Tdisp (v)		1080		Th
	Blanking	Tblk (v)	10	45	400	Th
Horizontal Section	Period	Th	1030	1100	1325	Tclk
	Active	Tdisp (h)		960		Tclk
	Blanking	Tblk (h)	70	140	365	Tclk
Clock	Frequency	Fclk=1/Tclk	50	74.25	82	MHz
Vertical Frequency	Frequency	Fv	47	60	63	Hz
Horizontal Frequency	Frequency	Fh	60	67.5	73	KHz

Notes:

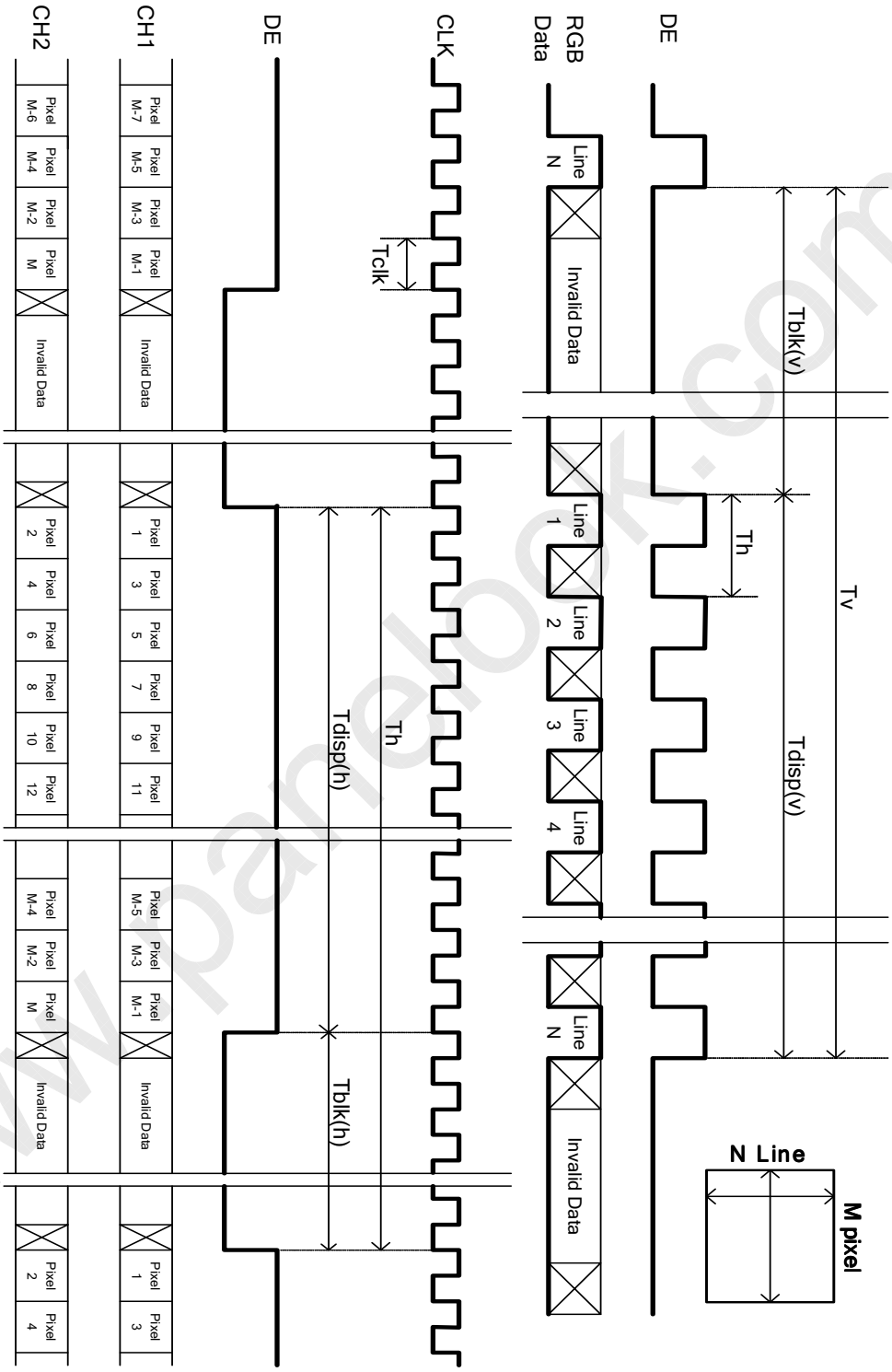
(1) Display position is specific by the rise of DE signal only.
Horizontal display position is specified by the rising edge of 1st DCLK after the rise of 1st DE, is displayed on the left edge of the screen.

(2) Vertical display position is specified by the rise of DE after a “Low” level period equivalent to eight times of horizontal period. The 1st data corresponding to one horizontal line after the rise of 1st DE is displayed at the top line of screen.

(3) If a period of DE “High” is less than 1920 DCLK or less than 1080 lines, the rest of the screen displays black.

(4) The display position does not fit to the screen if a period of DE “High” and the effective data period do not synchronize with each other.

3.4 Signal Timing Waveform



3.5 Color Input Data Reference

The brightness of each primary color (red, green, and blue) is based on the 10-bit gray scale data input for the color; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

Color		Input Color Data																													
		RED										GREEN										BLUE									
		MSB									LSB	MSB									LSB	MSB									LSB
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	RED(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(001)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	RED(1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GREEN	GREEN(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

	GREEN(1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	GREEN(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
BLUE	BLUE(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	BLUE(1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	BLUE(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

3.6 Backlight Power Specification

◆ Electrical Specification

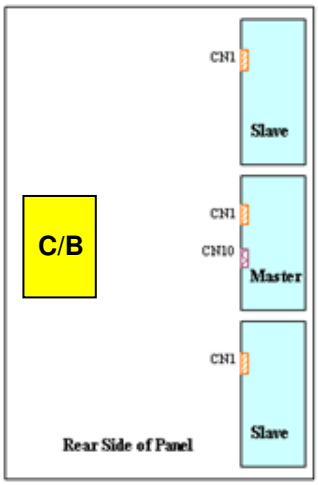
(Ta=25±5°C, Turn-on after 60mins)

Item	Symbol		Condition	Spec			Unit	Note
				Min	Typ	Max		
Input Voltage	V_{DDB}		-	21.6	24.0	26.4	VDC	-
Input Current	I_{DDB}		VDDB=24V	15.2	16.2	17.2	ADC	1
Input Power	P_{DDB}		VDDB=24V	365	389	413	W	1
Inrush Current	I_{RUSH}		VDDB=24V	-	-	26.3	ADC	2
Operating Frequency	FBL		VDDB=24V	40	42	44	KHz	-
On/Off control voltage	V_{BLON}	ON	VDDB=24V	2	-	5	VDC	-
		OFF		-0.3	-	0.8		-
On/Off control current	I_{BLON}		VDDB=24V	0	-	1.5	mA	-
Internal PWM Dimming Control Voltage	V_IPWM	MAX	VDDB=24V	3.0	-	3.3	VDC	-
		MIN		-	0	-	VDC	-
Internal PWM Dimming Control Current	I_IPWM		VDDB=24V	0	-	2	mADC	-
Internal PWM Dimming Ratio	R_IPWM		VDDB=24V	30	-	100	%	-
External PWM Control Voltage	V_EPWM	MAX	VDDB=24V	2	-	3.3	VDC	-
		MIN	VDDB=24V	0	-	0.8		-
External PWM Control Current	I_EPWM		VDDB=24V	0	-	2	mADC	-
External PWM Duty ratio	D_EPWM		VDDB=24V	30	-	100	%	-
External PWM Frequency	F_EPWM		VDDB=24V	140	180	240	Hz	-

Note 1 : Dimming ratio= 100% (MAX)（Ta=25±5℃, Turn on for 45minutes）
Note 2 : Measurement condition Rising time = 20ms (VDDB : 10%~90%);

Backlight Connector Pin Configuration

1. Input specification



CN1 of Master board: S14B-PH-SM3-TB (JST) or equivalent

Pin No	Symbol	Description
1	VDDB	Operating Voltage Supply, +24V DC regulated
2	VDDB	Operating Voltage Supply, +24V DC regulated
3	VDDB	Operating Voltage Supply, +24V DC regulated
4	VDDB	Operating Voltage Supply, +24V DC regulated
5	VDDB	Operating Voltage Supply, +24V DC regulated
6	BLGND	Ground and Current Return
7	BLGND	Ground and Current Return
8	BLGND	Ground and Current Return
9	BLGND	Ground and Current Return
10	BLGND	Ground and Current Return
11	NC	No connect
12	VBLON	Backlight On/Off: Open/High(+3.3V) for BL on, Low(GND) for BL off
13	PDIM(1)	External PWM Dimming Control input; Open/High (3.3V/100% Duty) for 100% Lum Internal PWM Dimming Control Input: Open/High (3.3V) for 100% Lum; GND for 30% Lum
14	PDIM Selection(2,3)	Dimming mode Selection. Low(GND)/Open: External PWM dimming; High(3.3V): Internal PWM dimming.

Note 1: PDIM is PWM duty control input for +3.3V TTL level signal or DC voltage by Pin 14 input. This input signal is (a) continuous pulse signal with +3.3V, 100% duty (i.e. +3.3V, DC level), backlight should perform 100% luminance. Duty ratio of this input signal should be proportional relationship in certain range of control without any

kind of inherent side effect like waterfall effect on screen. Guaranteed duty range and dimming ratio should be specified with supplementary measurement result.

Note 2: Pin 14 is the selection pin for dimming control method; if this pin is connected to High , PDIM (Pin 13) input should have DC level signal. Therefore the inverter should have SAW Tooth Wave Generator to generate internal PWM signal. If Pin 14 is connected to GND/open, PDIM (Pin 13) input should have external PWM signal.

Note 3: Pin 14 selection vs Pin 13 control function table:

	Pin 13 (Default: Open/High 100%)
Pin 14 = GND / open	**External PWM (AC signal control duty)**
Pin 14 = High	**Internal PWM (DC power control duty)**

CN1 of slave board: S12B-PH-SM3-TB (JST) or equivalent

Pin No	Symbol	Description
1	VDDB	Operating Voltage Supply, +24V DC regulated
2	VDDB	Operating Voltage Supply, +24V DC regulated
3	VDDB	Operating Voltage Supply, +24V DC regulated
4	VDDB	Operating Voltage Supply, +24V DC regulated
5	VDDB	Operating Voltage Supply, +24V DC regulated
6	VDDB	Operating Voltage Supply, +24V DC regulated
7	BLGND	Ground and Current Return
8	BLGND	Ground and Current Return
9	BLGND	Ground and Current Return
10	BLGND	Ground and Current Return
11	BLGND	Ground and Current Return
12	BLGND	Ground and Current Return

CN10 of Master board: CI4603M1HR0 (Cvilux)

Pin NO.	Signal name	Description
1	FB1	Feedback pin 1 (Sensor open lamp signal)
2	FB2	Feedback pin 2 (Sensor open lamp signal)
3	GND	GROND

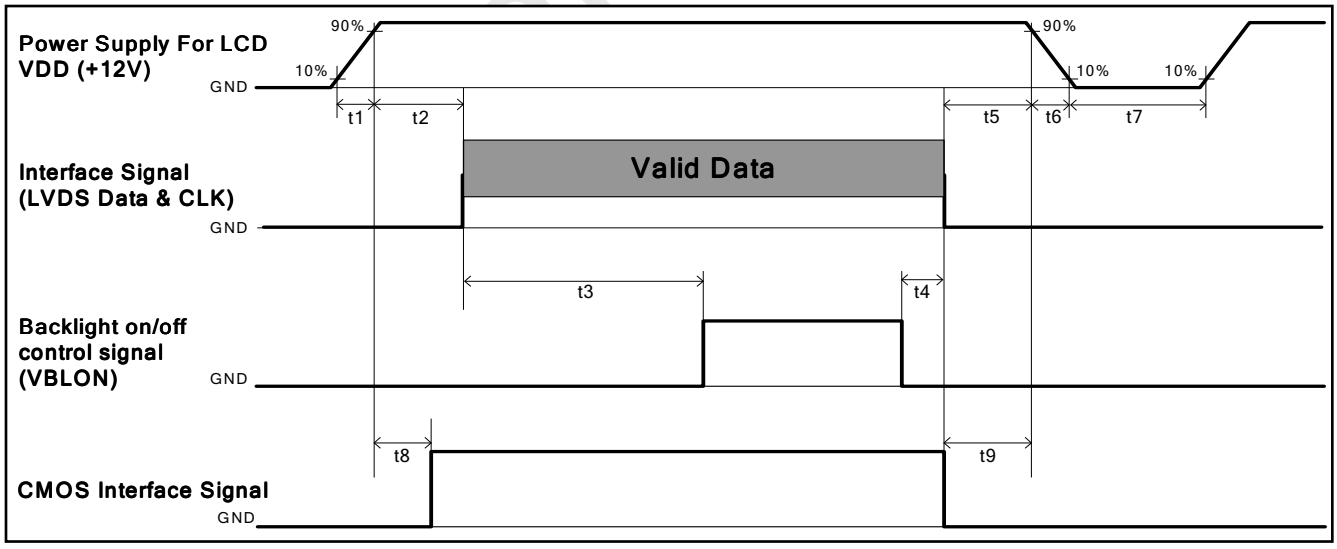
Note :

Open Lamp Detection Configuration:

Lamp status	(FB1, FB2)	Remark
Normal	(L,L)	No Open Lamp
1 lamp open	(L,H)	Inverter still work and send alarm signal continually.
2~3 lamps open	(H,L)	Inverter still work and send alarm signal continually.
≧4 lamps open	(H,H)	Inverter shut down

3.7 Power Sequence

◆ **Power Sequence of LCD**



Parameter	Values			Unit
	Min.	Type.	Max.	
t1	0.4	---	30	ms
t2	0.1	---	50	ms

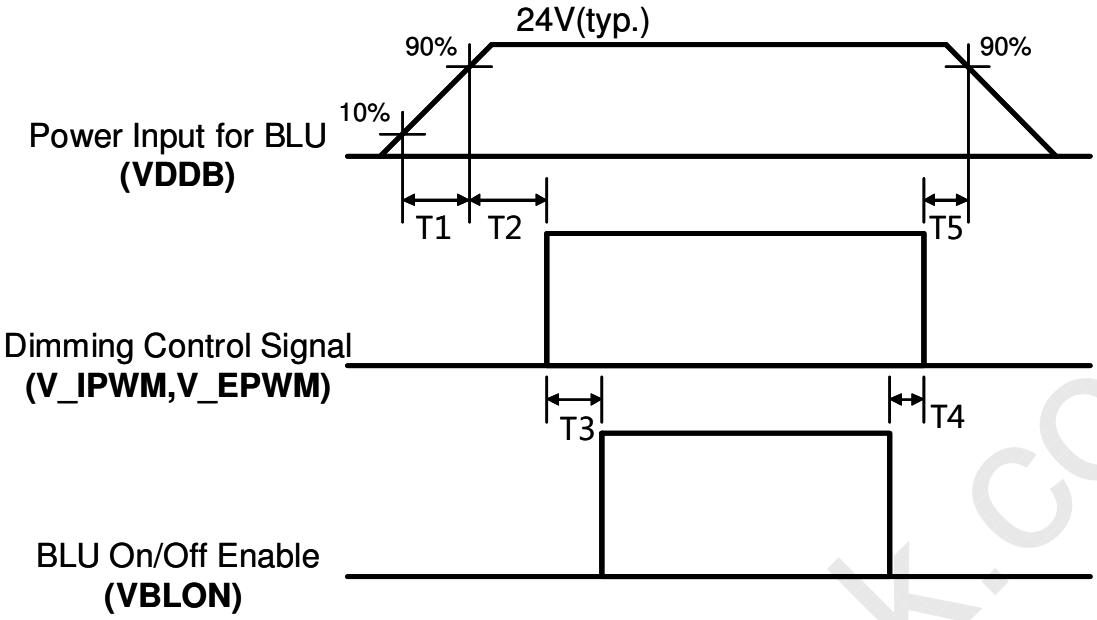
t3	450	---	---	ms
t4	0 *1	---	---	ms
t5	0	---	---	ms
t6	---	---	--- *2	ms
t7	500	---	---	ms
t8	10	---	50	ms
t9	0	---	---	ms

Note:
(1) t4=0 : concern for residual pattern before BLU turn off.
(2) t6 : voltage of VDD must decay smoothly after power-off. (Customer system decide this value)

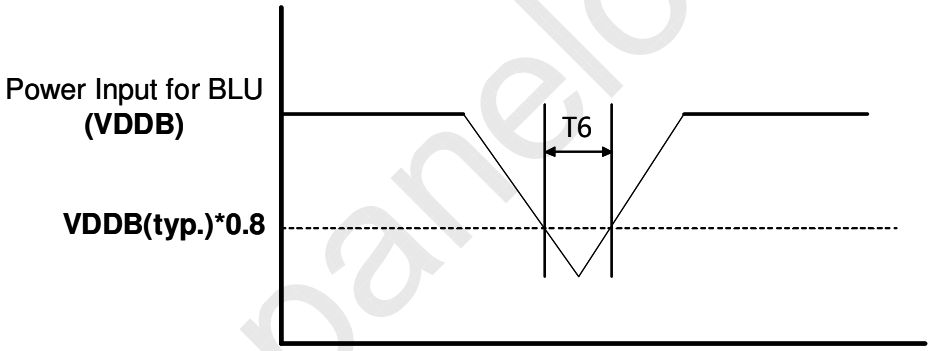
Apply the lamp voltage within the LCD operating range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal.

Caution: The above on/off sequence should be applied to avoid abnormal function in the display. In case of handling, make sure to turn off the power when you plug the cable into the input connector or pull the cable out of the connector.

◆ Power Sequence of Inverter



Dip condition for Inverter

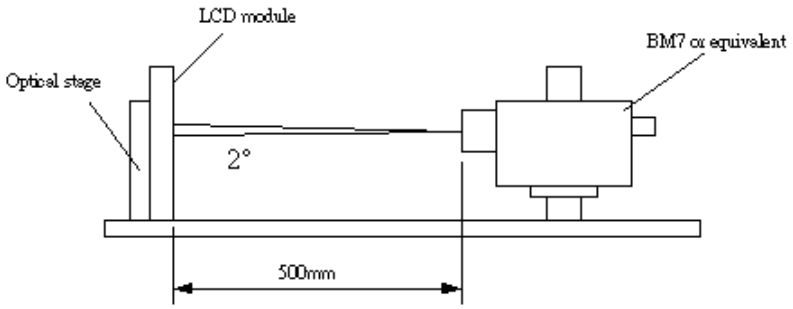


Parameter	Values			Unit
	Min.	Typ.	Max.	
T1	20	--	--	ms
T2	500	--	--	ms
T3	250	--	--	ms
T4	0	--	--	ms
T5	1	--	--	ms
T6	--	--	10	ms

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 60 minutes in a dark environment at 25℃. The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of φ and θ equal to 0°.

Test condition:



(Ta=25±5°C, Turn-on after 60mins)

Parameter	Symbol	Values			Unit	Notes
		Min.	Typ.	Max		
Contrast Ratio	CR	3000	4000	--		1
Surface Luminance (White)	L_{WH}	550	700	--	cd/m^2	2
Luminance Variation	$\delta_{WHITE(9P)}$	--	--	1.3		3
Response Time (Average)	T_R	--	8	--	ms	5 (Gray to Gray)
Rising Time	T_r	--	15	25	ms	4
Falling Time	T_f	--	8	10	ms	4
Color Coordinates						
Red	R_x	Typ.-0.03	0.64	Typ.+0.03		
	R_y		0.33			
Green	G_x		0.29			
	G_y		0.6			
Blue	B_x		0.15			
	B_y		0.06			
White	W_x		0.28			
	W_y		0.29			
Viewing Angle						(Contrast Ratio>10)
x axis, right(φ=0°)	θ_r	--	89	--	degree	6
x axis, left(φ=180°)	θ_l	--	89	--	degree	6
y axis, up(φ=90°)	θ_u	--	89	--	degree	6
y axis, down (φ=270°)	θ_d	--	89	--	degree	6

Note:

1. Contrast Ratio (CR) is defined mathematically as:

$$\text{Contrast Ratio(CR)} = \frac{\text{Surface Luminance with all" white" pixels}}{\text{Surface Luminance with all "black" pixels}}$$

2. Surface luminance is luminance value at point 1 across the LCD surface 50cm from the surface with all pixels displaying white. From more information see Fig. 4-2. When V_{DDB} = 24V, I_{DDB} = 12.5 A. $L_{WH}=L_{on1}$, Where Lon1 is the luminance with all pixels displaying white at center 1 location.

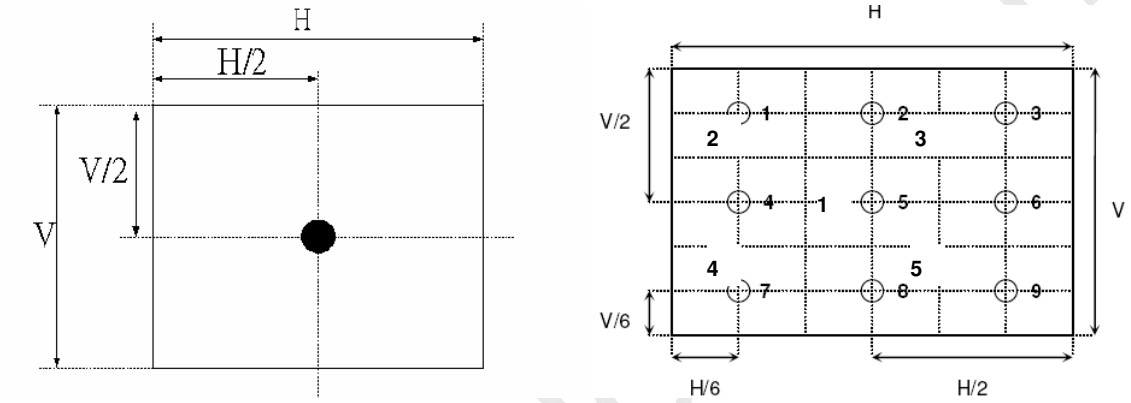


Fig.4-2 Optical measurement point

3. The variation in surface luminance, δ_{WHITE} is defined under 100% brightness as:

$$\delta_{WHITE(5P)}=\text{Maximum}(L_{on1}, L_{on2},\ldots,L_{on5})/\text{Minimum}(L_{on1}, L_{on2},\ldots L_{on5})$$

4. Response time is the time required for the display to transition from white(L255) to black(L0) (Decay Time, Tr_D=Tf) and from black(L0) to white(L255) (Rise Time, Tr_R=Tr). For additional information see Fig. 4-3.

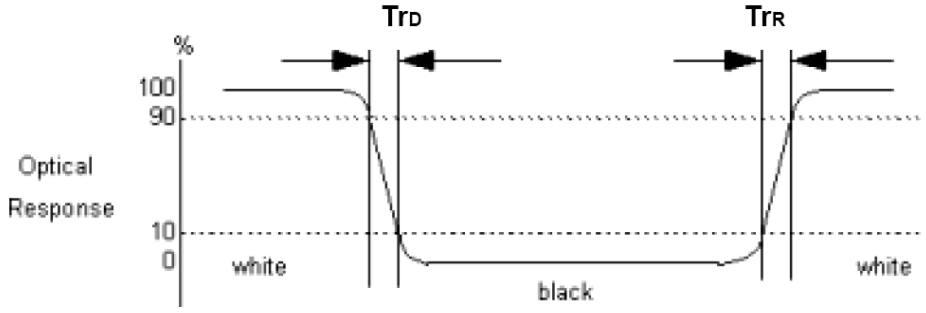


Fig.4-3 Response time

5. The response time is defined as the following figure and shall be measured by switching the input signal among 0%, 25%, 50%, 75%, 100% luminance. For additional information see Fig. 4-4.

	0%	25%	50%	75%	100%
0%		t: 0%-25%	t: 0%-50%	t: 0%-75%	t: 0%-100%
25%	t: 25%-0%		t: 25%-50%	t: 25%-75%	t: 25%-100%
50%	t: 50%-0%	t: 50%-25%		t: 50%-75%	t: 50%-100%
75%	t: 75%-0%	t: 75%-25%	t: 75%-50%		t: 75%-100%
100%	t: 100%-0%	t: 100%-25%	t: 100%-50%	t: 100%-75%	

Fig.4-4 Response time

6. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see Fig. 4-5. (Optical measurement by SR3)

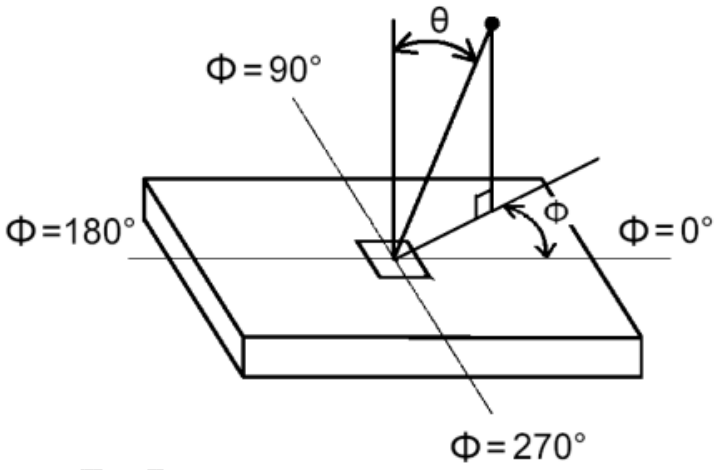


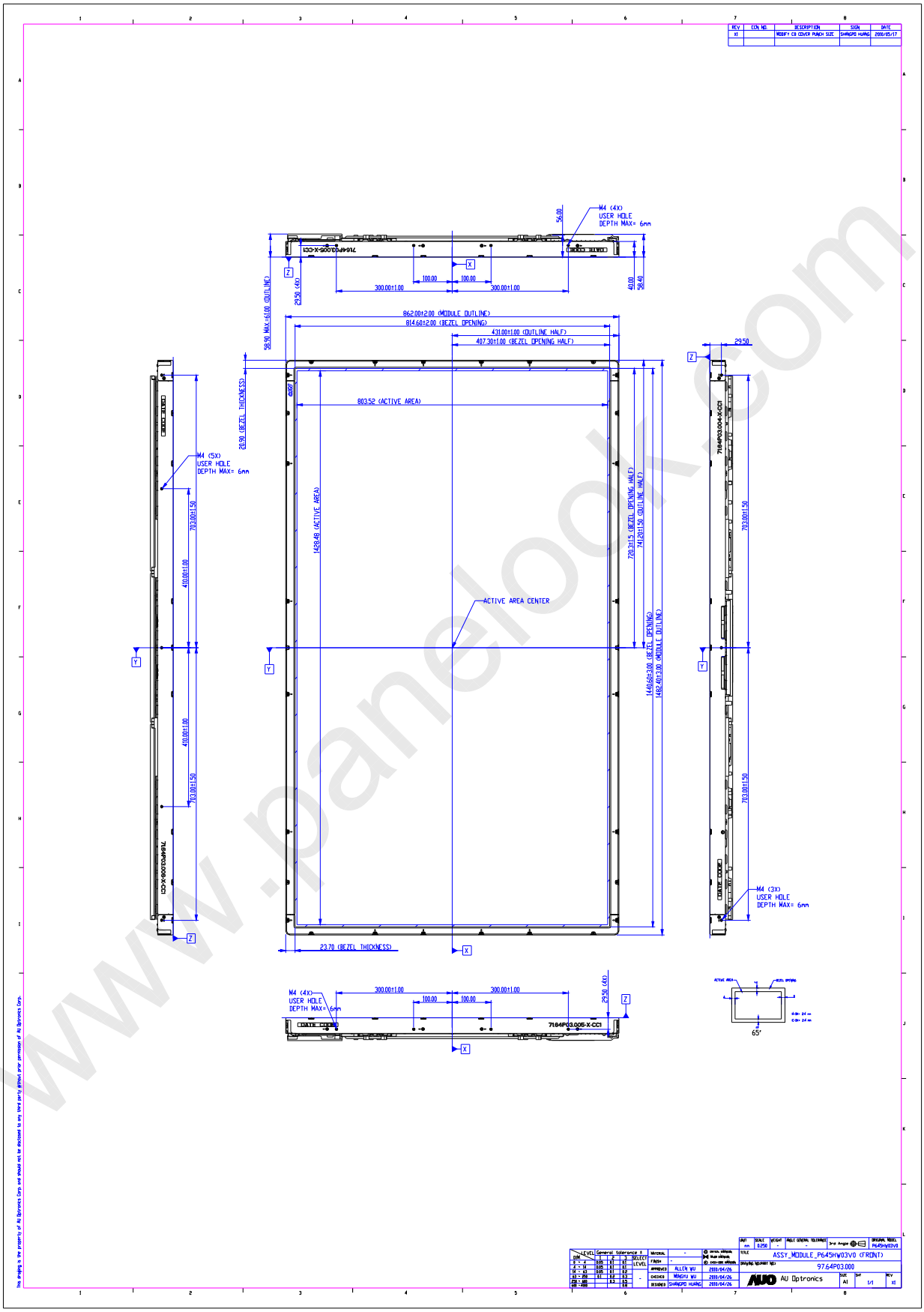
Fig.4-5 Viewing Angle Definition

5. Mechanical Characteristics

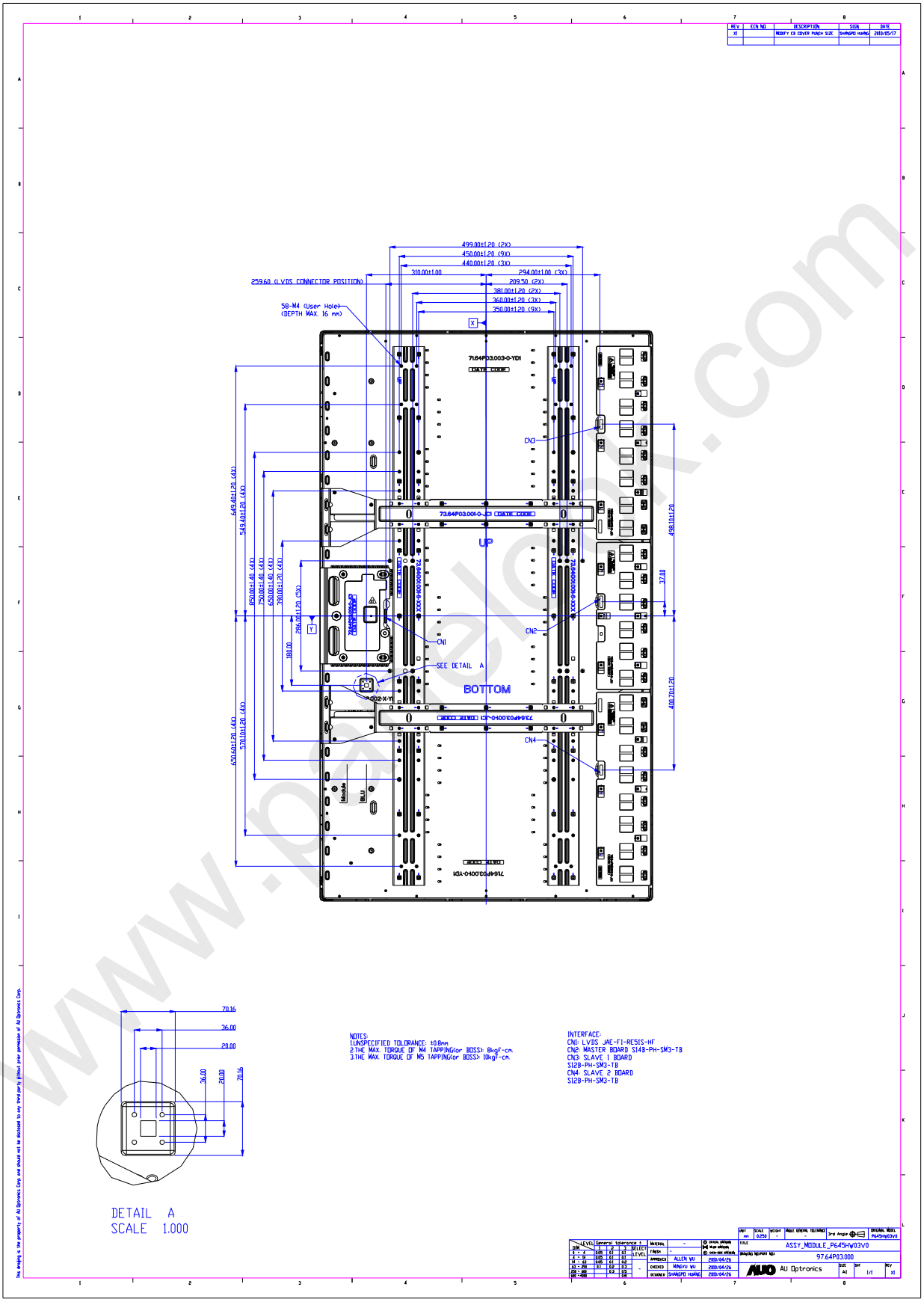
The contents provide general mechanical characteristics for the model P645HW03 V0. Detailed mechanical drawings are shown in the following pages.

Outline Dimension	Horizontal (typ.)	1482.4 mm
	Vertical (typ.)	862.0 mm
	Depth (typ.)	58.9mm (with inverter)
Bezel Opening Area	Horizontal (typ.)	1440.6mm
	Vertical (typ.)	814.6 mm
Active Display Area	Horizontal	1428.48 mm
	Vertical	803.52 mm
Weight	30 KG (Max)	

2D Drawing (Front)



2D Drawing (Rear)



Packing

6. Reliability Test

No	Test Item	Condition
1	High temperature storage test	Ta=60℃, 500hrs judge
2	Low temperature storage test	Ta=-20℃, 500hrs judge
3	High temperature operation test	Ta=50℃, 500hrs judge
4	Low temperature operation test	Ta=-5℃, 500hrs judge
5	Vibration test (with carton)	Wave form: Random Vibration level: 1.5G RMS, Bandwidth: 10~200Hz Duration: X, Y, Z (30min each direction)
6	Drop test (with carton)	Bottom flats:25.4 cm (ASTMD4169-I)

7. International Standard

7.1 Safety

(1) UL60065,2003, Underwriters Laboratories, Inc. (AUO file number : E204356)
Audio, video and similar electronic apparatus, safety requirement

(2) UL60950-1,2003, Underwriters Laboratories, (AUO file number : E204356)
Standard for safety of information technology equipment including electrical business equipment

(3) EN60065

(4) EN60950

(5) IEC 60065, European Committee for Electro technical Standardization (CENELEC)
Audio, video and similar electronic apparatus, safety requirement

(6) IEC 60950-1:
European Committee for Electrotechnical Standardization (CENELEC)
European Standard for safety of information technology equipment including electrical business equipment

7.2 EMC

(1) ANSI C63.4 “Methods of Measurement of Radio-Noise Emissions from Low-Voltage Electrical and Electrical Equipment in the Range of 9kHz to 40GHz. “American National standards Institute(ANSI), 1992

(2) C.I.S.P.R “Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment.” International Special committee on Radio Interference.

(3) EN 55022 “Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment.” European Committee for Electrotechnical Standardization. (CENELEC), 1998

8. Packing

A. **Panel Label**

1. Shipping Label Outline(P/N：82.64P01.001): 100mm * 23mm

Green mark description

(1) For Pb Free Product, AUO will add Pb for identification.

(2) For RoHs compatible products, AUO will add RoHS for identification.

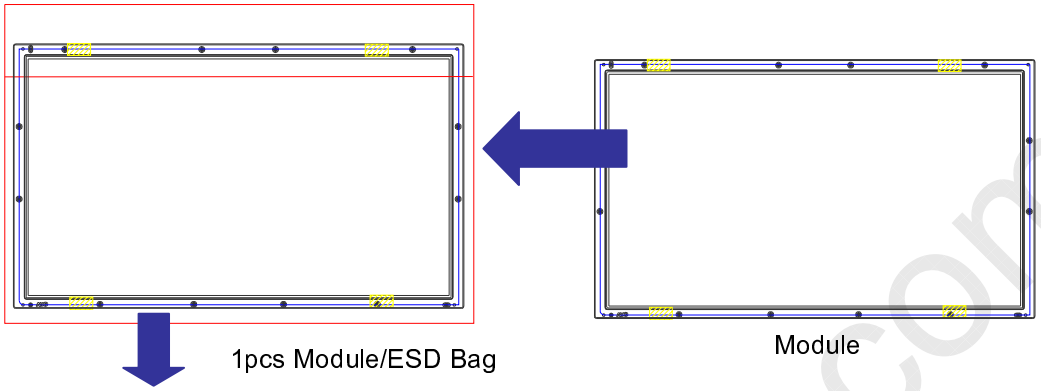
Note: The green Mark will be present only when the green documents have been ready by AUO internal green team. (definition of green design follows the AUO green design checklist.)

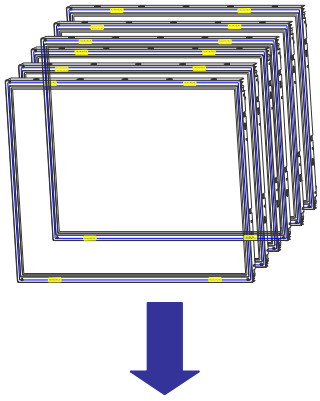
B. Carton Label

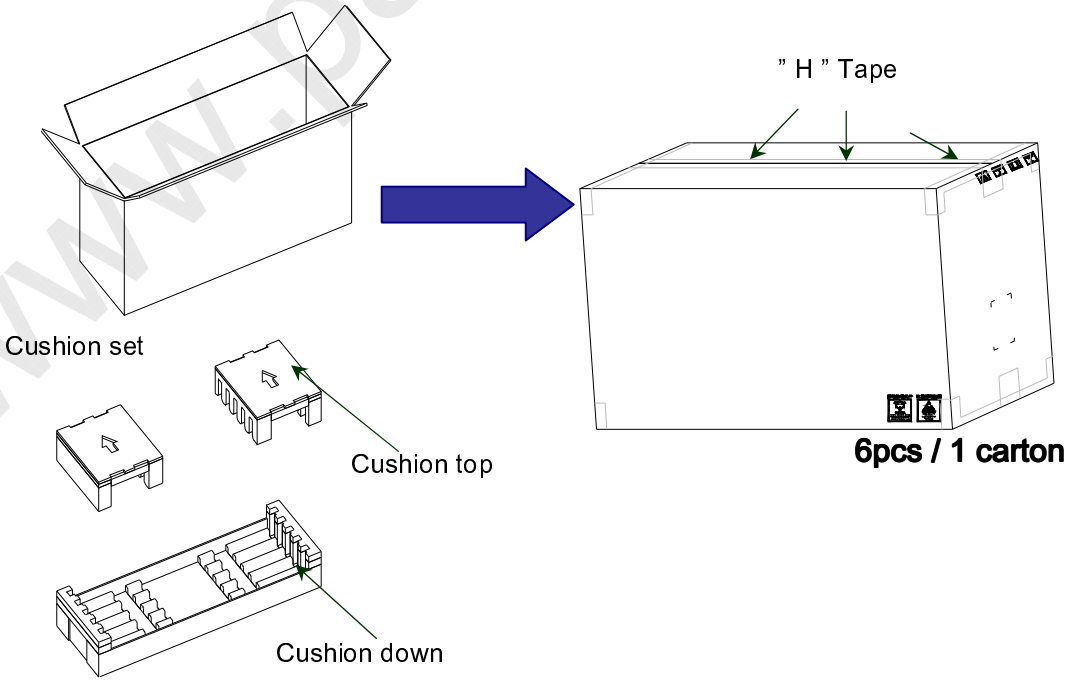
Catton label outline(P/N：82.15B06.004)：80mm*40mm

C. Packing Instruction

Carton dimension: 1634 (L) x 555 (W) x 1035 (H) ; One Box weight ：198kg





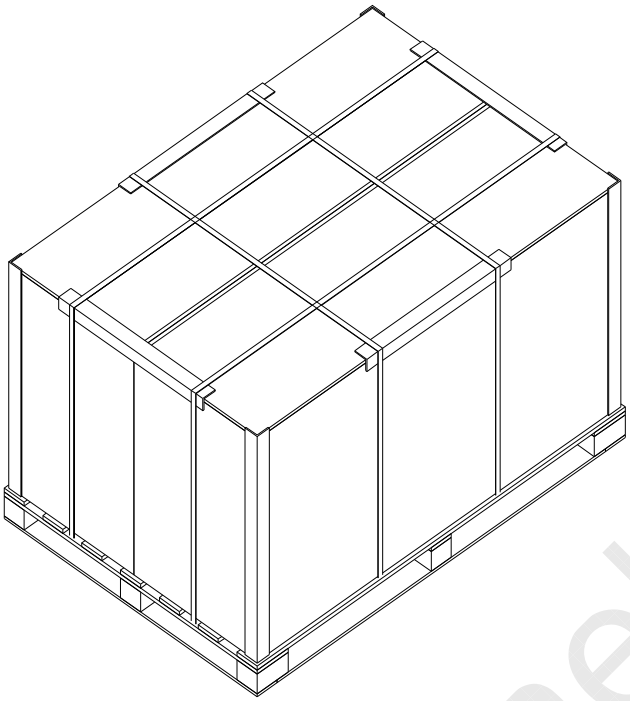


D. Packing Specification

By air cargo：(2x1) x 1 layer, one pallet put 2 boxes, total 12pcs module.

Dimension：1150mm*1660mm*1167mm

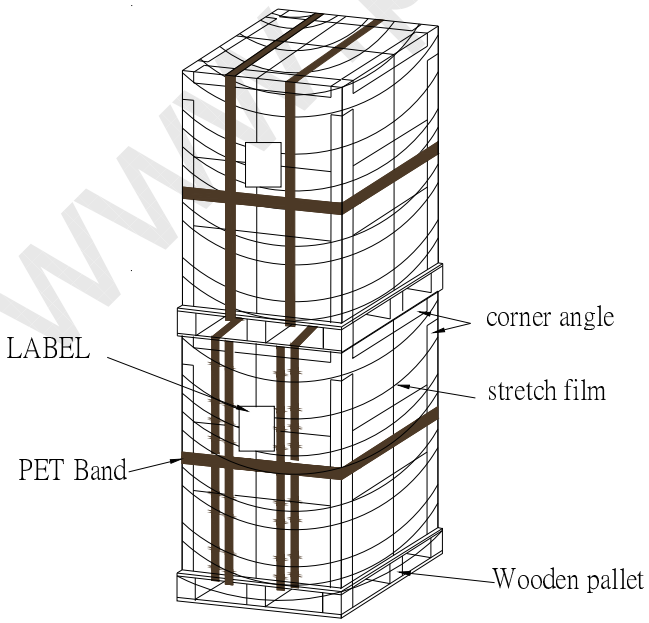
Weight：416kg



By sea：(2x1) x 2layer, one pallet put 2 boxes, stack 2 layers, total 24pcs module.

Dimension：1150mm*1660mm*2334mm

Weight：832 kg



	Item	Specification			Packing Remark
		Qty.	Dimension	Weight (kg)	
1	Packing BOX	6 pcs/box	1634(L)mm*555(W)mm*1035(H)mm	198	
2	Pallet	1	1660(L)mm*1150(W)mm*132(H)mm	20	
3	Boxes per Pallet	2 boxes/Pallet (By Air) ; 2 Boxes/Pallet (By Sea)			
4	Panels per Pallet	12pcs/pallet(By Air) ; 12 pcs/Pallet (By Sea)			
5	Pallet after packing	12 (by Air)	1660(L)mm*1150(W)mm*1167(H)mm (by Air)	416(by Air)	
		24 (by Sea)	1660(L)mm*1150(W)mm*2334(H)mm (by Sea)	832 (by Sea)	

9. Precautions

Please pay attention to the followings when you use this TFT LCD module.

9.1 MOUNTING PRECAUTIONS

(1) You must mount a module using holes arranged on back or edge side of panel.
(2) You should consider the mounting structure so that uneven force (ex. twisted stress) is not applied to module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
(3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.
(4) You should adopt radiation structure to satisfy the temperature specification.
(5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter cause circuit break by electro-chemical reaction.
(6) Do not touch, push or rub the exposed polarizer with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of polarizer for bare hand or greasy cloth. (Some cosmetics are detrimental to the polarizer.)
(7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front/rear polarizer. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
(8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
(9) Do not open the case because inside circuits do not have sufficient strength.

9.2 OPERATING PRECAUTIONS

(1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage: V=±200mV (over and under shoot voltage)
(2) Response time depends on the temperature. (In lower temperature, it becomes longer.)
(3) Brightness of CCFL depends on the temperature. (In lower temperature, it becomes lower.) And in lower temperature, response time (required time that brightness is stable after turned on) becomes longer.
(4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
(5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
(6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interface.

9.3 ELECTROSTATIC DISCHARGE CONTROL

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

9.4 PRECAUTIONS FOR STRONG LIGHT EXPOSURE

Strong light exposure causes degradation of polarizer and color filter.

9.5 STORAGE

When storing modules as spares for a long time, the following precautions are necessary.

(1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5℃ and 35℃ at normal humidity.
(2) The polarizer surface should not come in contact with any other object. It is recommended that they be stored in the container in which they were shipped.

9.6 HANDLING PRECAUTIONS FOR PROTECTION FILM

(1) The protection film is attached to the bezel with a small masking tape. When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
(2) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of flue still on the Bezel after the protection film is peeled off.
(3) You can remove the glue easily. When the glue remains on the Bezel or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

9.7 Operating Condition in PID Application

(1) If the continuous static display is required, periodically inserting a motion picture is strongly recommended.
(2) Recommend to periodically change the background color and background image.
(3) Recommend not to continuously operate over 18 hours a day.
(4) Recommend to adopt one of the following actions after long time display.
    I. Running the screen saver (motion picture or black pattern)
    II. Power off the system for a while
(5) Try not to run the LCD in a closed environment. Suitable venting on the system cover would be helpful for cooling.
(6) It is better to adapt active cooling with fans for long time displaying, especially for high luminance LCD model.