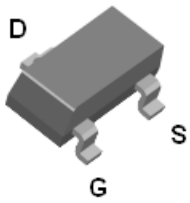
UNIKC Semiconductor

P7004EM

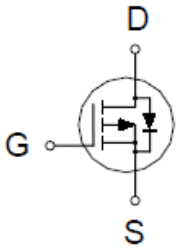
P-Channel Logic Level Enhancement Mode MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
-40V	70mΩ @V_{GS} = -10V	-2.5A



SOT-23



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	-40	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_A = 25 °C	I_D	-2.5	A
	T_A = 70 °C		-2	
Pulsed Drain Current[1]		I_{DM}	-20	
Avalanche Current		I_{AS}	-19	
Avalanche Energy	L = 0.1mH	E_{AS}	18	mJ
Power Dissipation	T_A = 25 °C	P_D	0.75	W
	T_A = 70 °C		0.48	
Operating Junction & Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient	Steady state	$R_{\theta JA}$		166	°C / W

[1]Pulse width limited by maximum junction temperature.

UNIKC Semiconductor

RoHS Compliant

P7004EM

P-Channel Logic Level Enhancement Mode MOSFET

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-40			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1.5	-2	-2.5	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -32V, V_{GS} = 0V			-1	μA
		V_{DS} = -30V, V_{GS} = 0V , T_J = 125 °C			-10	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = -5V, V_{GS} = -10V	-20			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = -10V, I_D = -2.5A		45	70	mΩ
Forward Transconductance[1]	g_{fs}	V_{DS} = -10V, I_D = -2.5A		6		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -20V, f = 1MHz		650		pF
Output Capacitance	C_{oss}			137		
Reverse Transfer Capacitance	C_{rss}			92		
Total Gate Charge[2]	Q_g	V_{DS} = 0.5$V_{(BR)DSS}$, V_{GS} = -10V, I_D = -2.5A		12		nC
Gate-Source Charge[2]	Q_{gs}			2		
Gate-Drain Charge[2]	Q_{gd}			4		
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DS} = -20V, I_D ≅ -1A, V_{GEN} = -10V, R_{GS} = 6Ω		7		nS
Rise Time[2]	t_r			10		
Turn-Off Delay Time[2]	$t_{d(off)}$			30		
Fall Time[2]	t_f			22		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICE (T_J = 25 ˚C)						
Continuous Current	I_S				-0.75	A
Forward Voltage[1]	V_{SD}	I_F = -2.5A, V_{GS} = 0V			-1	V

[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[2]Independent of operating temperature.

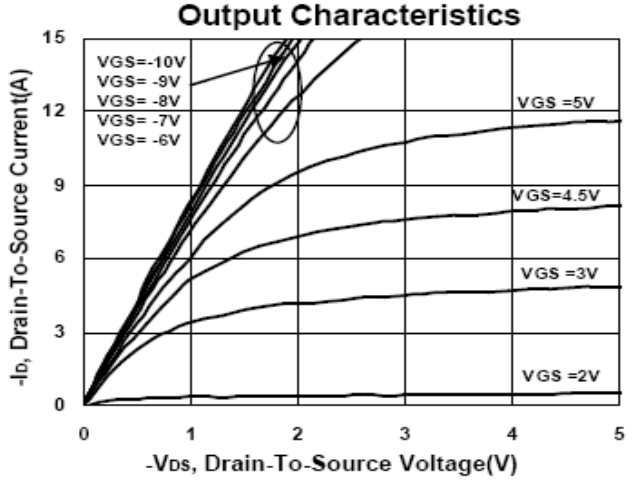
UNIKC Semiconductor

RoHS Compliant

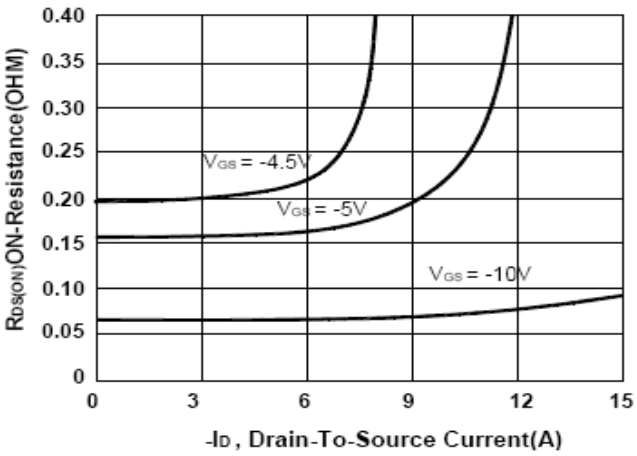
P7004EM

P-Channel Logic Level Enhancement Mode MOSFET

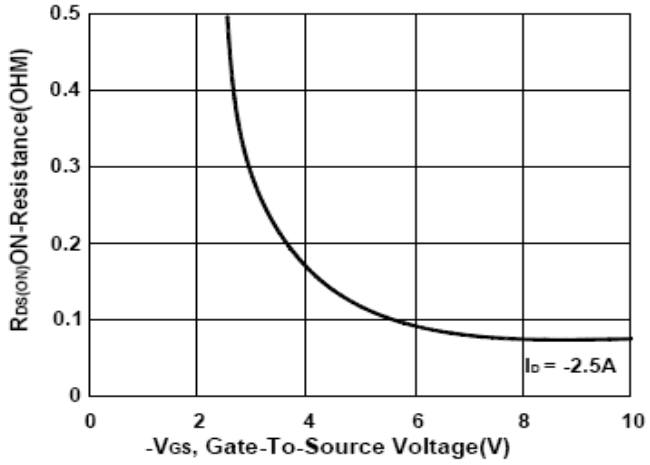
Output Characteristics



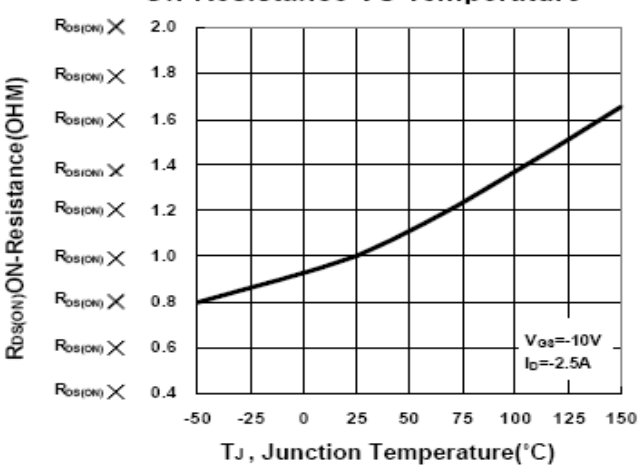
On-Resistance VS Drain Current



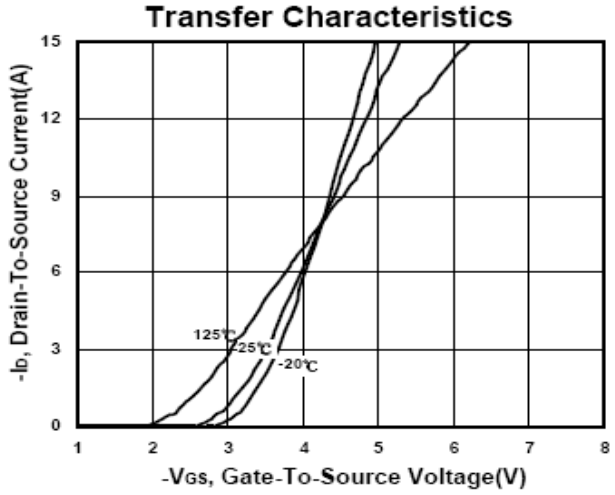
On-Resistance VS Gate-To-Source



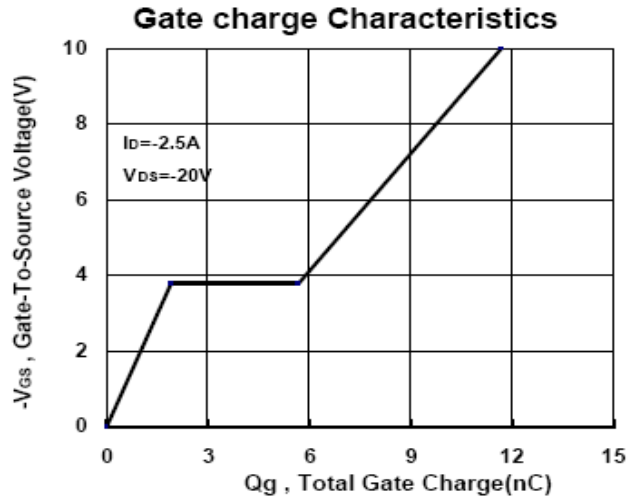
On-Resistance VS Temperature



Transfer Characteristics



Gate charge Characteristics



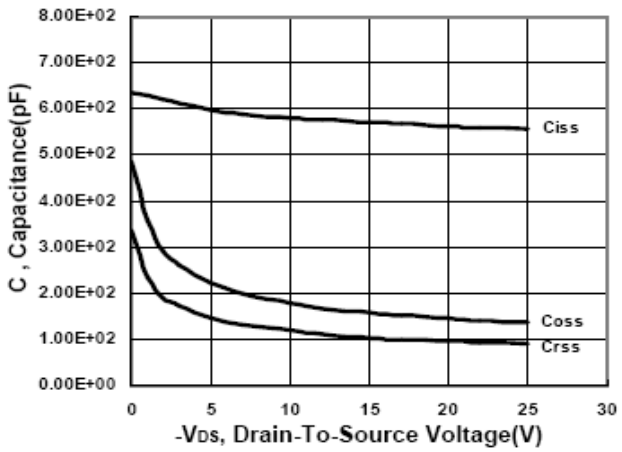
UNIKC Semiconductor

RoHS Compliant

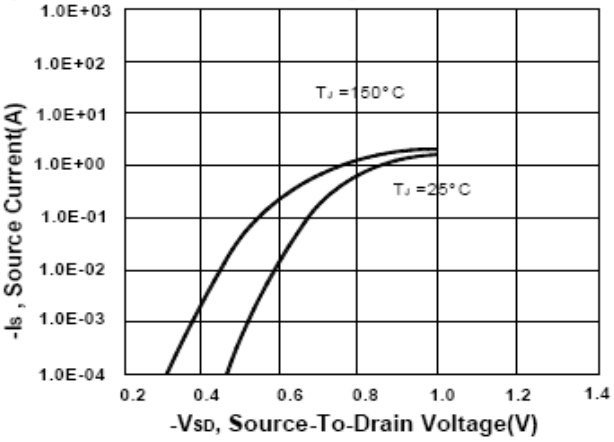
P7004EM

P-Channel Logic Level Enhancement Mode MOSFET

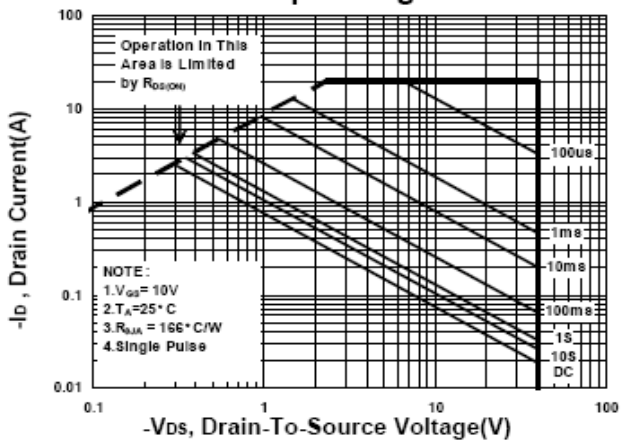
Capacitance Characteristic



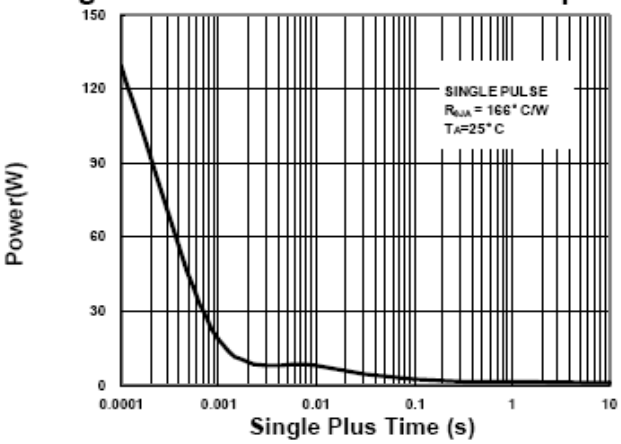
Body Diode Forward Voltage VS Source current



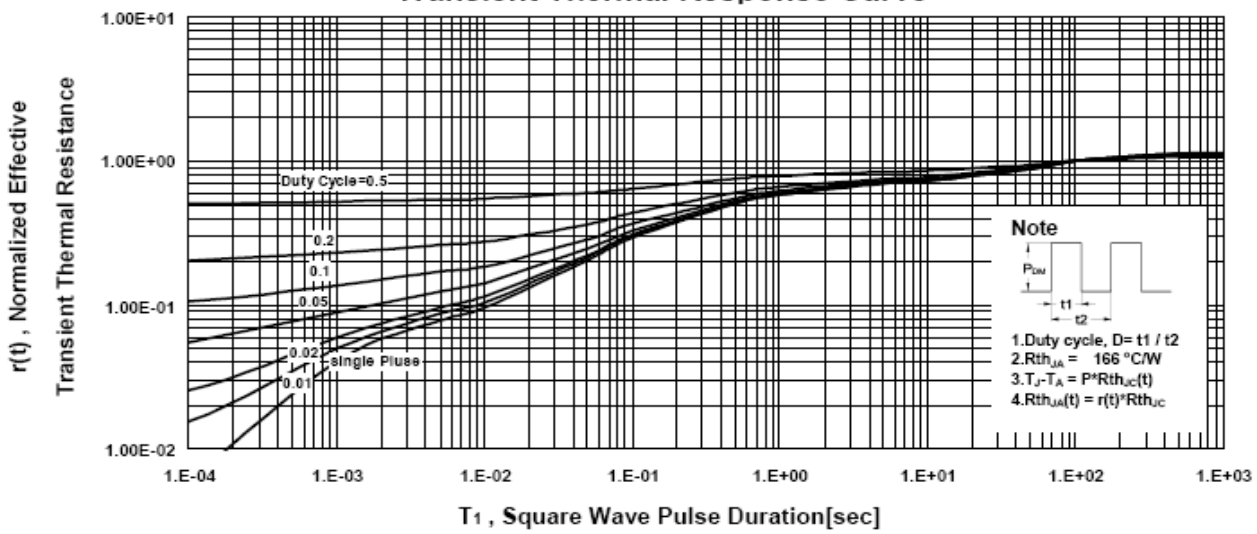
Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve



UNIKC Semiconductor

RoHS Compliant

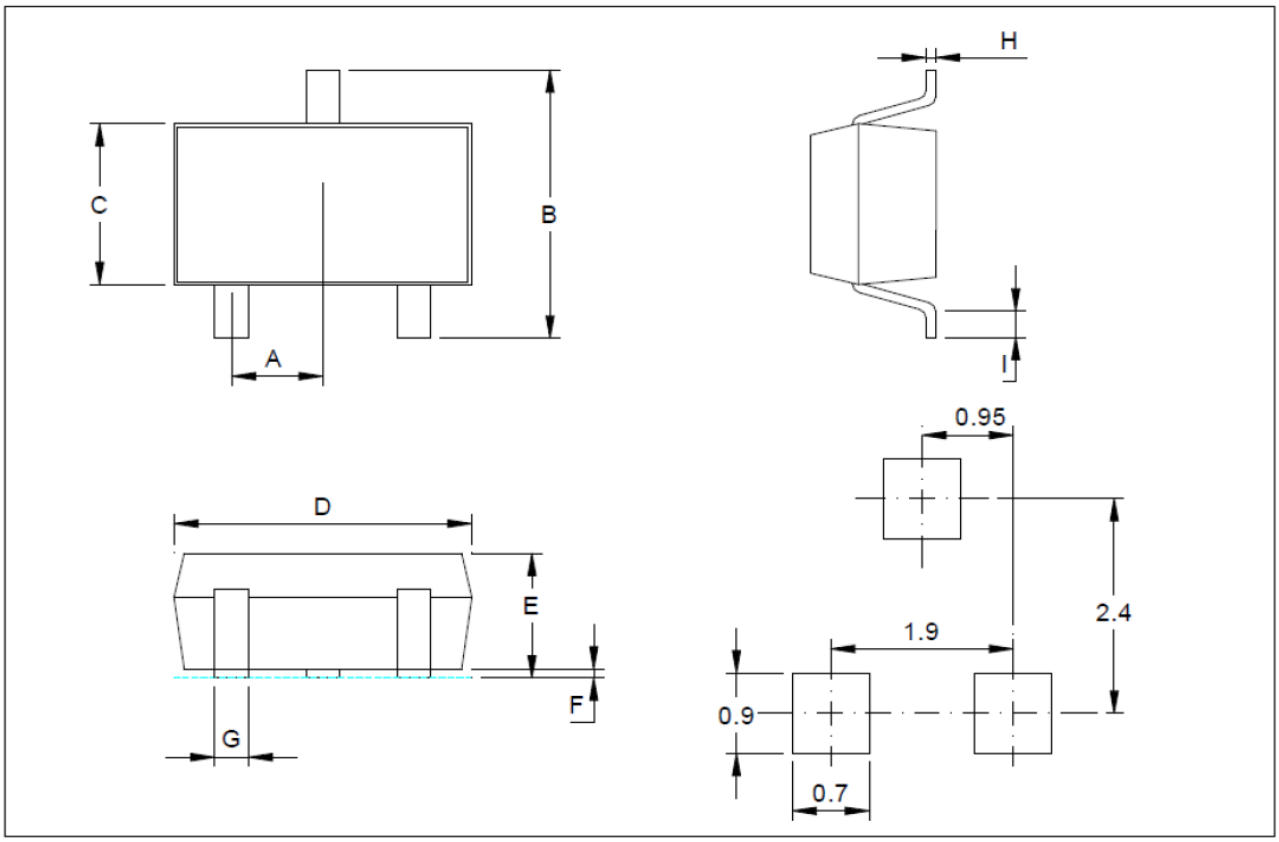
P7004EM

P-Channel Logic Level Enhancement Mode MOSFET

Package Dimension

SOT-23 MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A		1.05		H	0.1		0.2
B	2.4		3	I	0.3		0.6
C	1.4		1.73				
D	2.7		3.1				
E	1		1.31				
F	0		0.15				
G	0.3		0.5				



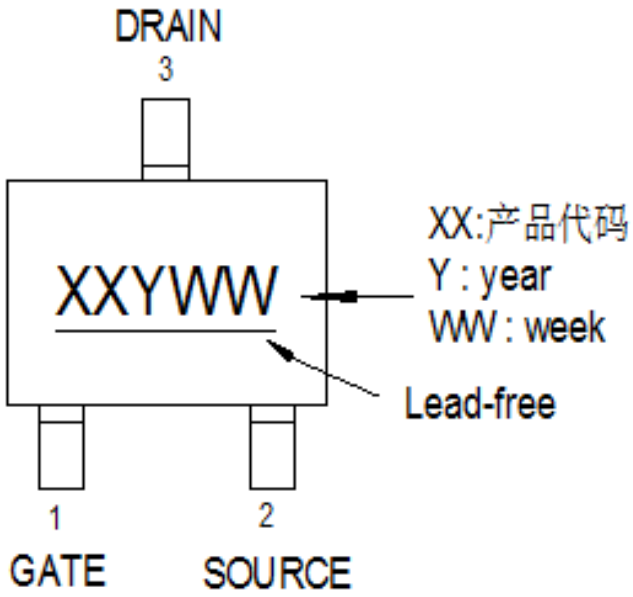
UNIKC Semiconductor

RoHS Compliant

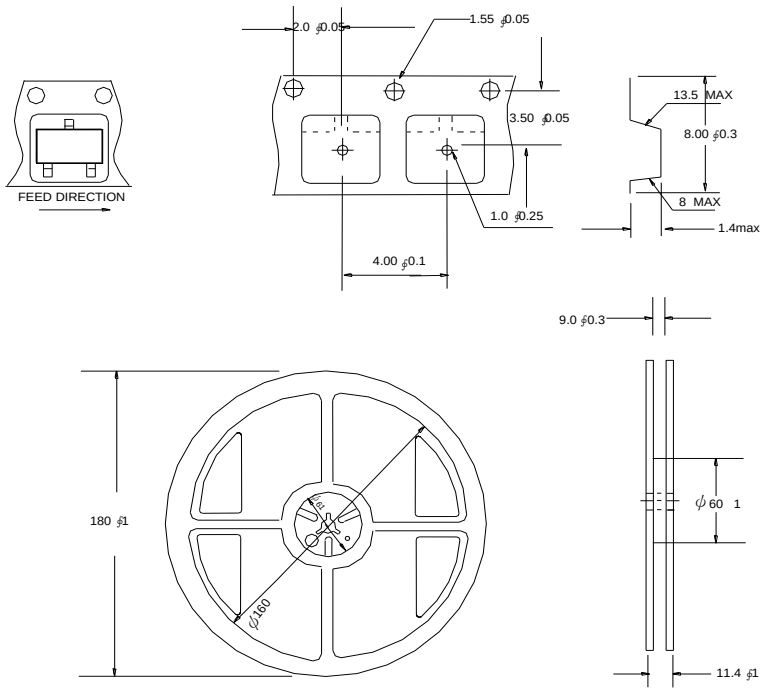
P7004EM

P-Channel Logic Level Enhancement Mode MOSFET

A. Marking Information (此产品代码为：2J)



B. Tape&Reel Information:3000pcs/Reel

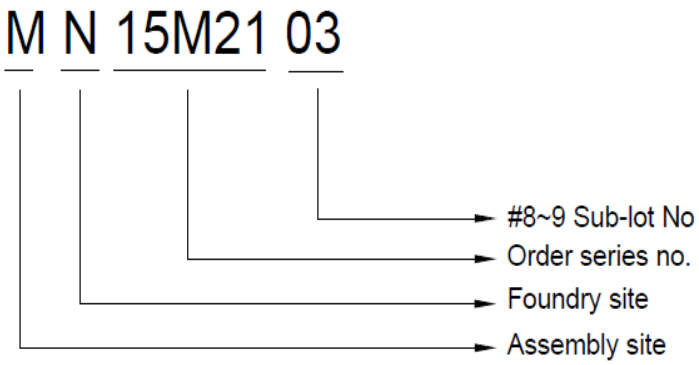


P7004EM

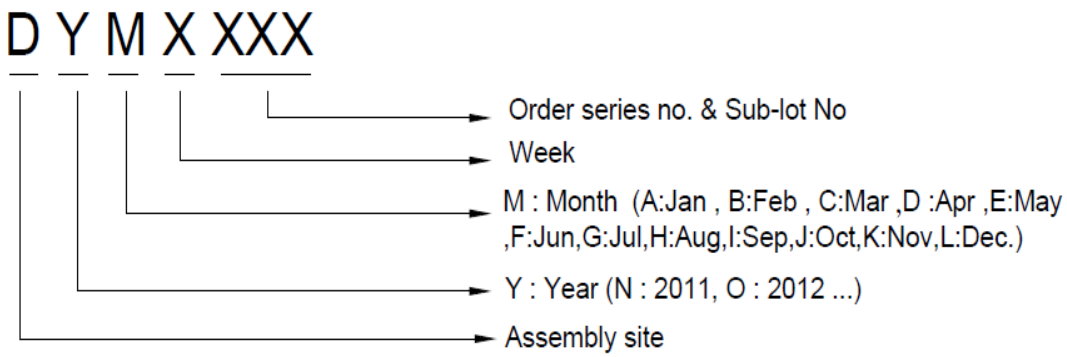
P-Channel Logic Level Enhancement Mode MOSFET

C. Lot.No. & Date Code rule

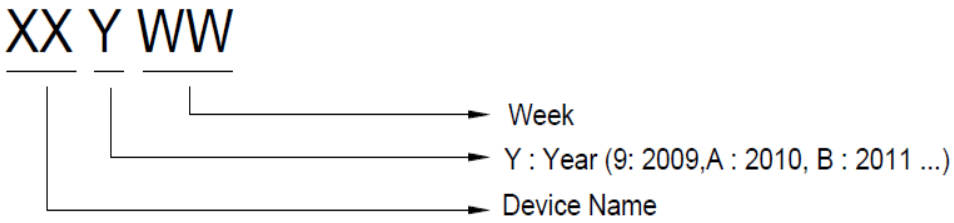
1.LOT.NO.



2.Date Code



3.Date Code (for Small package)



UNIKC Semiconductor

RoHS Compliant

P7004EM

P-Channel Logic Level Enhancement Mode MOSFET

D.Label rule

标签内容(Label content)

1	Label Size	30 * 90 mm
2	Font style	Times New Roman or Arial （或可区分英文”0”和数字”0”，”G和”Q”的字型即可）
3	Great Power	Height: 4 mm
4	Package	Height: 2 mm
5	Date	Height: 2 mm Shipping date: YYYY/MM/DD, ex. 2008/09/12
6	Device	Height: 3 mm (Max: 16 Digit)
7	Lot	Height: 3 mm (Max: 9 Digit) Sub lot
8	D/C	Height: 3 mm (Max: 7 Digit)
9	QTY	Height: 3 mm (Max: 6 Digit) Thousand mark is no needed
10	Pb Free label	Diameter: 1 cm bottom color: Green Font color: Black Font style: Arial
11	Halogen Free label	Diameter: 1 cm bottom color: Green Font color: Black Font style: Arial
12	Scan info	Device / Lot / D/C / QTY , Insert “ / “ between every parts. for example: P3055LDG/G12345601/GGG2301/2000 DPI (Dots per inch): Over 300 dpi Code : Code 128 Height: 6 mm at least