8031AH/8051AH/8053AH

Single-Chip 8-Bit Microcontroller

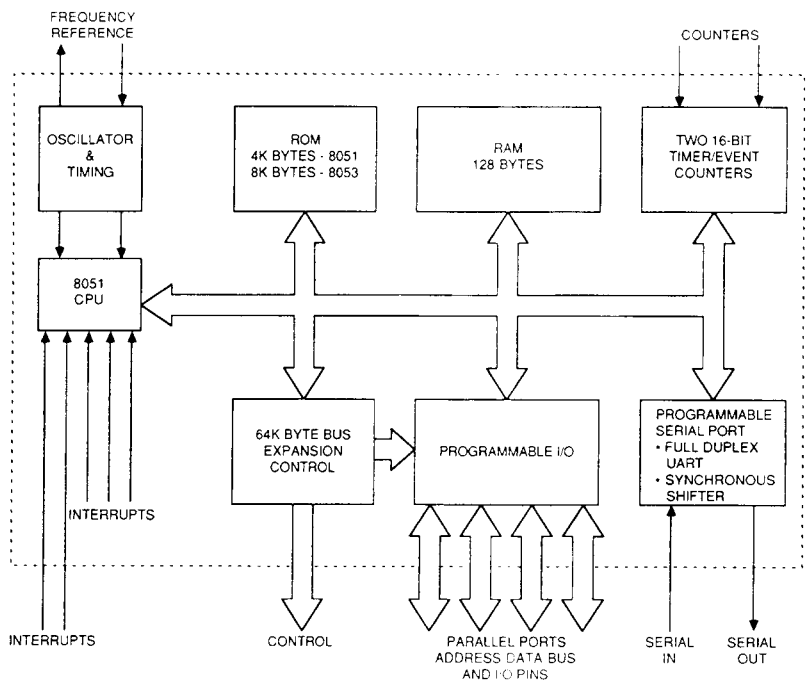
DISTINCTIVE CHARACTERISTICS

- 4K x 8 ROM (8051 only)
- 8K x 8 ROM (8053 only)
- 128 x 8 RAM
- Four 8-bit ports, 32 I/O lines
- Two 16-bit timer/event counters
- 64K addressable Program Memory
- All versions are pin-compatible
- Boolean processor
- Programmable Serial Port
- Five interrupt sources/two priority levels
- On-chip Oscillator/Clock Circuit
- 64K addressable Data Memory

GENERAL DESCRIPTION

The 8051 Family is optimized for control applications. Byte processing and numerical operations on small data structures are facilitated by a variety of fast addressing modes for accessing the internal RAM. The instruction set provides a convenient menu of 8-bit arithmetic instructions, including multiply and divide instructions. Extensive on-chip support is provided for 1-bit variables as a separate data type. This allows direct bit manipulation and testing in control and logic systems that require Boolean processing. Efficient use of program memory results from an instruction set consisting of 44% 1-byte, 41% 2-byte, and 15% 3-byte instructions. With a 12 MHz crystal, 58% of the instructions execute in 1 μs, 40% in 2 μs, and multiply and divide require only 4 μs.

BLOCK DIAGRAM

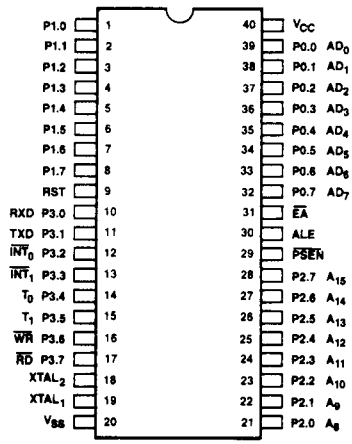


Publication #	Rev.	Amendment
07839	B	/0

Issue Date: June 1987

CONNECTION DIAGRAMS
Top View

DIPS



CD005551

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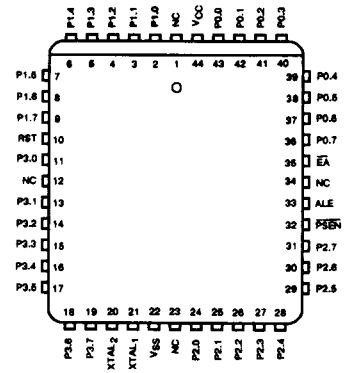

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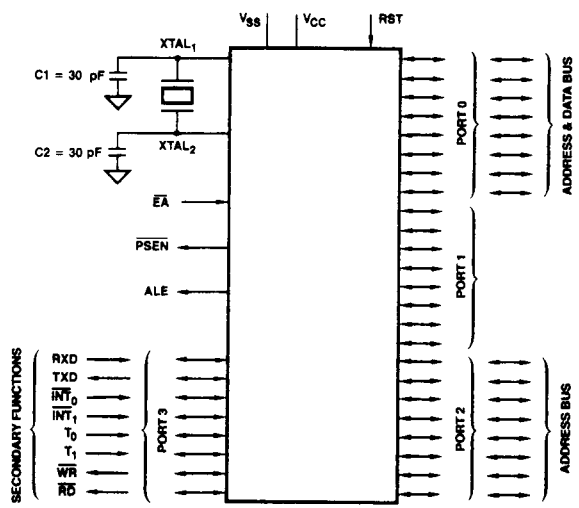
LOGIC SYMBOL

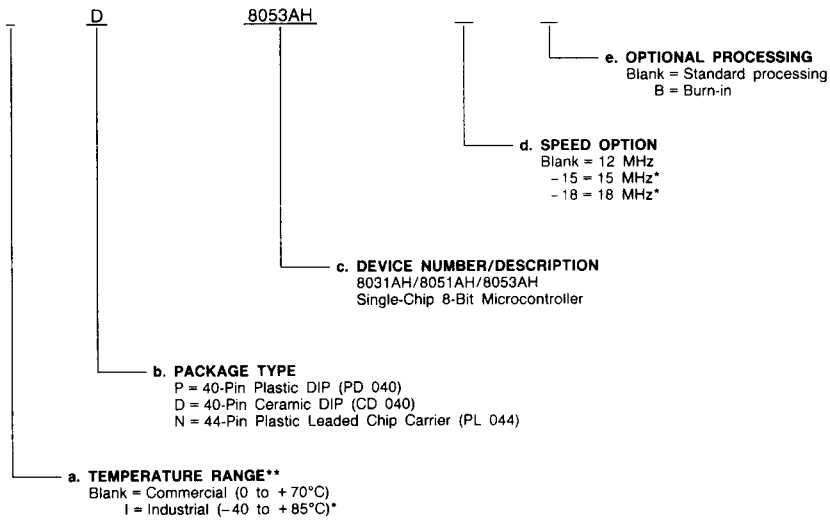


LS001322

ORDERING INFORMATION

Commodity Products

AMD commodity products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Temperature Range**
b. Package Type
c. Device Number
d. Speed Option
e. Optional Processing



Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

*Available only for the 8031AH at time of printing.

**This device is also available in Military temperature range. See MOS Microprocessors and Peripherals Military Handbook (Order # 09275A/0) for electrical performance characteristics.

Valid Combinations	
P, D, N	8031AH-18
	8031AH-15
	8031AH
	8051AH
	8053AH
ID	8031AHB

PIN DESCRIPTION

Port 0 (Bidirectional, Open Drain)

Port 0 is an open-drain I/O port. As an Output Port, each pin can sink eight LS TTL inputs. Port 0 pins that have "1"s written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed LOW-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting "1"s. Port 0 also outputs the code bytes during program verification in the 8051AH and 8053AH. External pullups are required during program verification.

Port 1 (Bidirectional)

Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four LS TTL inputs. Port 1 pins that have "1"s written to them are pulled HIGH by the internal pullups and — while in this state — can be used as inputs. As inputs, Port 1 pins that are externally being pulled LOW will source current (I_{IL} on the data sheet) because of the internal pullups.

Port 1 also receives the LOW-order address bytes during program verification.

Port 2 (Bidirectional)

Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source four LS TTL inputs. Port 2 pins having "1"s written to them are pulled HIGH by the internal pullups and — while in this state — can be used as inputs. As inputs, Port 2 pins externally being pulled LOW will source current (I_{IL}) because of the internal pullups.

Port 2 emits the HIGH-order address byte during fetches from external Porgram Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting "1"s. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function register.

Port 2 also receives the HIGH-order address bits during ROM verification.

Port 3 (Bidirectional)

Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four LS TTL inputs. Port 3 pins having "1"s written to them are pulled HIGH by the internal pullups and — while in this state — can be used as inputs. As inputs, Port 3 pins externally being pulled LOW will source current (I_{IL}) because of pullups.

Port 3 also serves the functions of various special features as listed below:

Port Pin	Alternate Function
$P_{3.0}$	RxD (Serial Input Port)
$P_{3.1}$	TxD (Serial Output Port)
$P_{3.2}$	$\overline{INT_0}$ (External Interrupt 0)
$P_{3.3}$	$\overline{INT_1}$ (External Interrupt 1)
$P_{3.4}$	T_0 (Timer 0 External Input)
$P_{3.5}$	T_1 (Timer 1 External Input)
$P_{3.6}$	$\overline{WR}$ (External Data Memory Write Strobe)
$P_{3.7}$	$\overline{RD}$ (External Data Memory Read Strobe)

RST Reset (Input; Active HIGH)

A HIGH on this pin — for two machine cycles while the oscillator is running — resets the device.

ALE Address Latch Enable (Output; Active HIGH)

Address Latch Enable output pulse for latching the LOW byte of the address during accesses to external memory. ALE can drive eight LS TTL inputs.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, allowing use for external-timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

$\overline{PSEN}$ Program Store Enable (Output; Active LOW)

$\overline{PSEN}$ is the read strobe to external Program Memory. $\overline{PSEN}$ can drive eight LS TTL inputs. When the device is executing code from an external program memory, $\overline{PSEN}$ is activated twice each machine cycle — except that two $\overline{PSEN}$ activations are skipped during each access to external Data Memory. $\overline{PSEN}$ is not activated during fetches from internal Program Memory.

$\overline{EA}$ External Access Enable (Input; Active LOW)

$\overline{EA}$ must be externally held LOW to enable the device to fetch code from external Program Memory locations 0000H to 0FFFH (0000H to 1FFFH in the 8053AH). If $\overline{EA}$ is held HIGH, the 8051AH executes from internal Program Memory unless the program counter contains an address greater than 0FFFH (1FFFH in the 8053AH).

$XTAL_1$ Crystal (Input)

Input to the oscillator's high-gain amplifier. Required when a crystal is used. Connect to V_{SS} when external source is used on $XTAL_2$.

$XTAL_2$ Crystal (Output)

Output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal or external source can be used.

V_{CC} Power Supply

V_{SS} Circuit Ground

FUNCTIONAL DESCRIPTION

The term "8051" shall be used to refer collectively to the 8051AH, 8031AH, and 8053AH.

8051 CPU Architecture

The 8051 CPU manipulates operands in three memory spaces. These are the 64K-byte Program Memory, 64K-byte External Data Memory and 256-byte Internal Data Memory. Of the 64K bytes of Program Memory space, the lower 4K bytes on the 8051AH (addr. 0000H to 0FFFH) and the lower 8K bytes of the 8053AH (addr. 0000H to 1FFFH) may reside on-chip. The Internal Data Memory address space is further divided into the 128-byte Internal Data RAM and 128-byte Special Function Register (SFR) address spaces shown in Figure 1.

Four Register Banks (each with eight registers), 128 addressable bits and the stack reside in the Internal Data RAM. The stack depth is limited only by the available Internal Data RAM and its location is determined by the 8-bit stack pointer. All registers except the four 8-Register Banks reside in the Special Function Register address space. These memory mapped registers include arithmetic registers, pointers, I/O ports, interrupt system registers, timers, and a serial port. Ninety-two bit locations in the SFR address space are addressable as bits. The 8051 contains 128 bytes of Internal Data RAM and 20 SFRs.

The 8051 provides a non-paged Program Memory address space to accommodate relocatable code. Conditional branches are performed relative to the Program Counter. The base-register-plus-index register-indirect jump permits branching relative to a 16-bit base register with an offset provided by an 8-bit index register. Sixteen-bit jumps and calls permit branching to any location in the contiguous 64K Program Memory address space.

The 8051 has five methods for addressing source operands: Register, Direct, Register-Indirect, Immediate, and Base-Register-plus-Index-Register-Indirect Addressing. The first three methods can be used for addressing destination operands. Most instructions have a "destination, source" field that specifies the data type, addressing methods, and operands involved. For operations other than moves, the destination operand is also a source operand.

Registers in the four 8-Register Banks can be accessed through Register, Direct, or Register-Indirect Addressing; the 128 bytes of Internal Data RAM through Direct or Register-Indirect Addressing; and the Special Function Registers through Direct Addressing. External Data Memory is accessed through Register-Indirect Addressing. Look-Up-Tables resident in Program Memory can be accessed through Base-Register-plus-Index-Register-Indirect Addressing.

The 8051 is classified as an 8-bit machine since the internal ROM, RAM, Special Function Registers, Arithmetic Logic Unit, and external data bus are each 8-bits wide. The 8051 performs operations on bit, nibble, byte, and double-byte data types.

The 8051 has extensive facilities for byte transfer, logic, and integer arithmetic operations. It excels at bit handling since data transfer, logic, and conditional branch operations can be performed directly on Boolean variables.

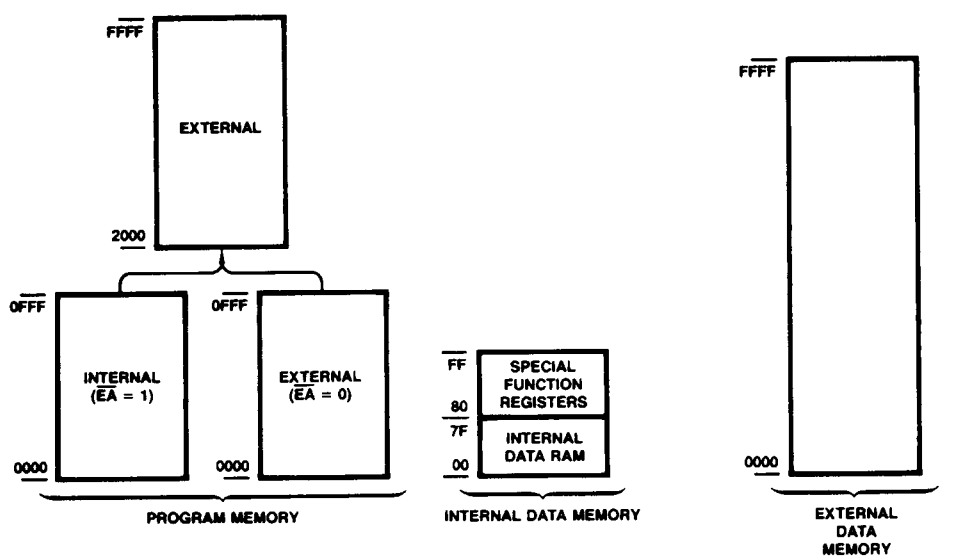


Figure 1. 8051 Memory Organization

Special Function Register Map

Addr (Hex)	Symbol	Name	Default Power-On Reset
80 *	P0	Port 0	11111111
81	SP	Stack Pointer	00000111
82	DPL	Data Pointer Low	00000000
83	DPH	Data Pointer High	00000000
87	PCON	Power Control	0XXX0000
88 *	TCON	Timer/Counter Control	00000000
89	TMOD	Timer/Counter Mode Control	00000000
8A	TLO	Timer/Counter 0 Low Byte	00000000
8B	TL1	Timer/Counter 1 Low Byte	00000000
8C	TH0	Timer/Counter 0 High Byte	00000000
8D	TH1	Timer/Counter 1 High Byte	00000000
90 *	P1	Port 1	11111111
98 *	SCON	Serial Control	00000000
99	SBUF	Serial Data Buffer	Indeterminate
A0 *	P2	Port 2	11111111
A8 *	IE	Interrupt Enable Control	0XX00000
B0 *	P3	Port 3	11111111
B8 *	IP	Interrupt Priority Control	XXX00000
D0 *	PSW	Program Status Word	00000000
E0 *	ACC	Accumulator	00000000
F0 *	B	B Register	00000000

* Bit Addressable

8051 Instruction Set

The 8051AH, 8031AH, and 8053AH share the same instruction set. It allows expansion of on-chip CPU peripherals and optimizes byte efficiency and execution speed. Efficient use of program memory results from an instruction set consisting of 49 single-byte, 45 two-byte,and 17 three-byte instructions. When using a 12-MHz oscillator, 64 instructions execute in 1 μs and 45 instructions execute in 2 μs. The remaining instructions (multiply and divide) execute in only 4 μs. The number of bytes in each instruction and the number of cycles required for execution are listed in Table 1.

On-Chip Peripheral Functions

In addition to the CPU and memories, an interrupt system, extensive I/O facilities, and several peripheral functions are integrated on-chip to relieve the CPU of repetitious, complicated, or time-critical tasks and to permit stringent real-time control of external system interfaces. The extensive I/O facilities include the I/O pins, parallel I/O ports, bidirectional address/data bus, and the serial port for I/O expansion. The CPU peripheral functions intergrated on-chip are the two 16-bit counters and the serial port. All of these work together to boost system performance.

Interrupt System

External events and the real-time-driven on-chip peripherals require service by the CPU asynchronous to the execution of any particular section of code. To tie the asynchronous activities of these functions to normal program execution, a sophisticated multiple-source, two-priority-level, nested interrupt system is provided. Interrupt response latency ranges from 3 μs to 7 μs when using a 12 MHz crystal.

The 8051 acknowledges interrupt request from five sources: Two from external sources via the $\overline{INT_0}$ and $\overline{INT_1}$ pins, one from each of the two internal counters and one from the serial I/O port. Each interrupt vectors to a separate location in Program Memory for its service program. Each of the five sources can be assigned to either of two priority levels and can be independently enabled and disabled. Additionally all enabled sources can be globally disabled or enabled. Each external interrupt is programmable as either level- or transition-activated and is active-LOW to allow the "wire or-ing" of several interrupt sources to the input pin. The interrupt system is shown diagrammatically in Figure 2.

I/O Facilities

The 8051 has instructions that treat its 32 I/O lines as 32 individually addressable bits and as four parallel 8-bit ports addressable as Ports 0, 1, 2 and 3. Ports 0, 2, and 3 can also assume other functions. Port 0 provides the multiplexed low-order address and data bus used for expanding the 8051 with standard memories and peripherals. Port 2 provides the high-order address bus when expanding the 8051 with External Program Memory or External Data Memory. The pins of Port 3 can be configured individually to provide external interrupt request inputs, counter inputs, the serial port's receiver input and transmitter output, and to generate the control signals used for reading and writing External Data Memory. The generation or use of an alternate function on a Port 3 pin is done automatically by the 8051 as long as the pin is configured as an input. The configuration of the ports is shown on the 8051 Logic Symbol.

Open-Drain I/O Pins

Each pin of Port 0 can be configured as an open drain output or as a high-impedance input. Resetting the microcomputer programs each pin as an input by writing a one (1) to the pin. If a zero (0) is later written to the pin it becomes configured as an output and will continuously sink current. Rewriting a one (1) to the pin will place its output driver in a high-impedance state and configure the pin as an input. Each I/O pin of Port 0 can sink/source eight LS TTL loads.

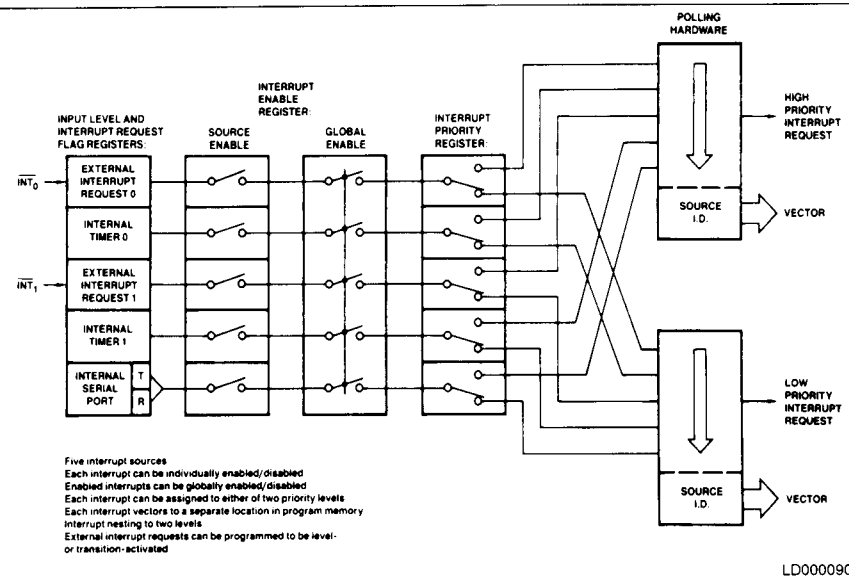


Figure 2. 8051 Interrupt System

Quasi-Bidirectional I/O Pins

Ports 1, 2 and 3 are quasi-bidirectional buffers. Resetting the microcomputer programs each pin as an input by writing a one (1) to the pin. If a zero (0) is later written to the pin it becomes configured as an output and will continuously sink current. Any pin that is configured as an output will be reconfigured as an input when a one (1) is written to the pin. Simultaneous to this reconfiguration, the output driver of the quasi-bidirectional port will source current for two oscillator periods. Since current is sourced only when a bit previously written to a zero (0) is updated to a one (1), a pin programmed as an input will not source current into the TTL gate that is driving it if the pin is later written with another one (1). Since the quasi-bidirectional output driver sources current for only two oscillator periods, an internal pull-up resistor of approximately 20 to 40 kΩ is provided to hold the external driver's loading at a TTL HIGH level. Ports 1, 2, and 3 can sink/source four LS TTL loads.

Microprocessor Bus

When accessing external memory the HIGH-order address is emitted on Port 2 and the LOW-order address on Port 0. The ALE signal is provided for strobing the address into an external latch. The program store enable ($\overline{PSEN}$) signal is provided for enabling an external memory device to Port 0 during a read from the Program Memory address space. When the MOVX instruction is executed, Port 3 automatically generates the read ($\overline{RD}$) signal for enabling an External Data Memory device to Port 0 or generates the write ($\overline{WR}$) signal for strobing the external memory device with the data emitted by Port 0. Port 0 emits the address and data to the external memory through a push/pull driver that can sink/source eight LS TTL loads. At the end of the read/write bus cycle, Port 0 is automatically reprogrammed to its high-impedance state and Port 2 is returned to the state it had prior to the bus cycle. The 8053AH generates the address, data, and control signals needed by memory and I/O devices in a manner that minimizes the requirements placed on external program and data memories.

Timer Event Counters

The 8051 contains two 16-bit counters for measuring time intervals and pulse widths, for counting events, as well as for generating precise, periodic interrupt requests. Each can be programmed independently to one of the following three modes:

Mode 0 – similar to an 8048 8-bit timer or counter with divide by 32 prescaler.

Mode 1 – 16-bit time-interval or event counter.

Mode 2 – 8-bit time-interval or event counter with automatic reload upon overflow.

Additionally, counter 0 can be programmed to a mode that divides it into one 8-bit time-interval or event counter and one 8-bit time-interval counter (Mode 3). When counter 0 is in Mode 3, counter 1 can be programmed to any of the three aforementioned modes, although it cannot set an interrupt request flag or generate an interrupt. This mode is useful because counter 1's overflow can be used to pulse the serial port's transmission-rate generator. Along with their multiple operating modes and 16-bit precision, the counters can also handle very high input frequencies. These range from 0.1 MHz to 1.0 MHz (from 1.2 MHz to 12 MHz crystal) when programmed to increment once every machine cycle and from 0 Hz to an upper limit of 50 kHz to 0.5 MHz (for 1.2 MHz to 12 MHz crystal) when programmed for external inputs. Both internal and external inputs can be gated to the counter by a second external source for directly measuring pulse widths.

The counters are started and stopped under software control. Each counter sets its interrupt request flag when it overflows from all ones to all zeroes (or auto-reload value). The operating modes and input sources are summarized in Figures 3 and 4. The effects of the configuration flags and the status flags are shown in Figures 5 and 6.

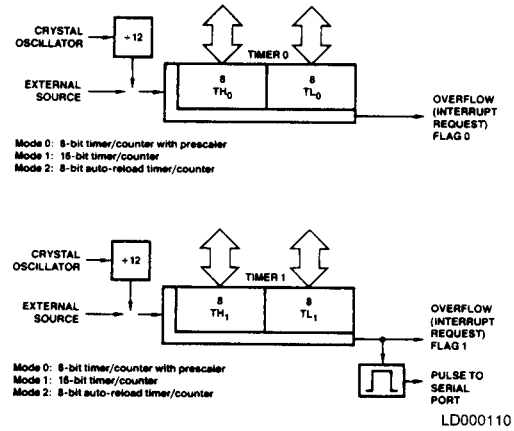


Figure 3. Timer/Event Counter Modes 0, 1 and 2

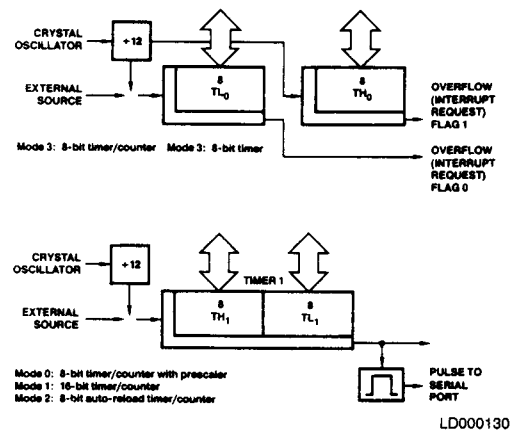


Figure 4. Timer/Event Counter 0 in Mode 3

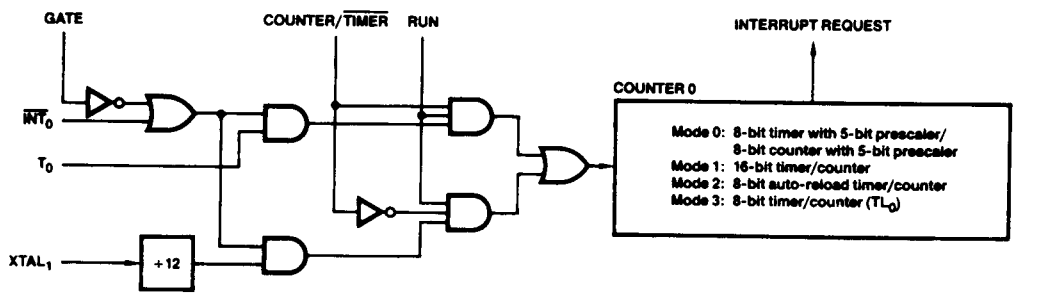


Figure 5. Timer/Counter 0 Control and Status Flag Circuitry

Serial Communications

The 8051's serial I/O port is useful for serially linking peripheral devices as well as multiple 8051s through standard asynchronous protocols with full-duplex operation. The serial port also has a synchronous mode for expansion of I/O lines using CMOS and TTL shift registers. This hardware serial communications interface saves ROM code and permits a much higher tranmission rate than could be achieved through software. In response to a serial port interrupt request, the CPU has only to read/write the serial port's buffer to service the serial link. A block diagram of the serial port is shown in Figures 7 and 8. Methods for linking UART (universal asynchronous receiver/transmitter) devices are shown in Figure 9 and a method for I/O expansion is shown in Figure 10.

The full-duplex serial I/O port provides asynchronous modes to faciliate communications with standard UART devices, such as printers and CRT terminals, or communications with other 8051s in multi-processor systems. The receiver is double buffered to eliminate the overrun that would occur if the CPU failed to respond to the receiver's interrupt before the beginning of the next frame. The 8051 can generally maintain the serial link at its maximum rate so double buffering of the transmitter is not needed. A minor degradation in transmission rate can occur in rare events such as when the servicing of the transmitter has to wait for a lengthy interrupt service program to complete. In asynchronous modes, false start-bit rejection is provided on received frames. For noise rejection a best two-out-of-three vote is taken on three samples near the center of each received bit.

When interfacing with standard UART devices, the serial channel can be programmed to Mode 1 which transmits/receives a ten-bit frame or programmed to Mode 2 or 3 which transmits/receives an eleven-bit frame as shown in Figure 11. The frame consists of a start bit, eight or nine data bits, and one stop bit. In modes 1 and 3, the transmission-rate timing circuitry receives a pulse from counter 1 each time the counter overflows. The input to counter 1 can be an external source or a division by 12 of the oscillator frequency. The auto-reload mode of the counter provides communication rates of 0.05 to 62,500 bits per second (including start and stop bits) for a 12-MHz crystal. In Mode 2 the communication rate is a division by 64 or 32 of the oscillator frequency yielding a transmission rate of 187,500 bits per second or 375,000 bits per second (including start and stop bits) for a 12-MHz crystal.

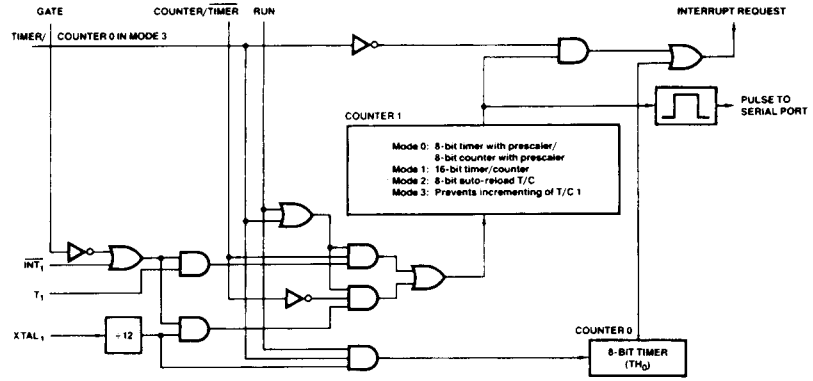


Figure 6. Timer/Counter 1 Control and Status Flag Circuitry

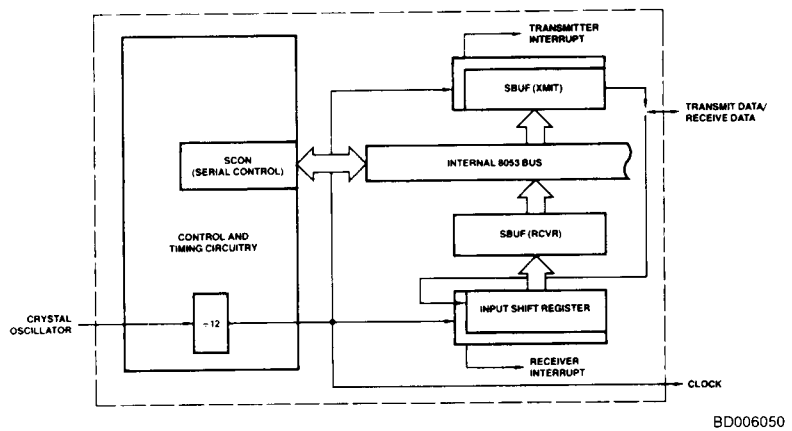


Figure 7. Serial Port — Synchronous Mode 0

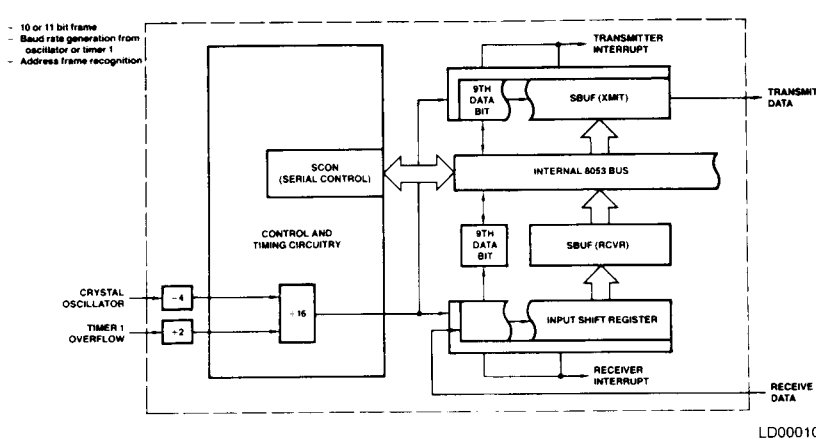


Figure 8. Serial Port — UART Modes 1, 2 and 3

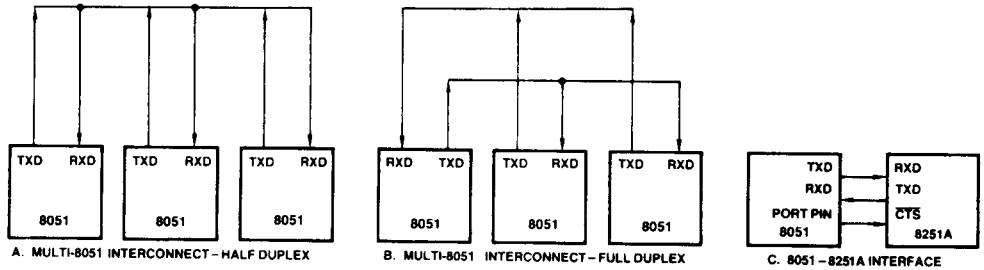


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Figure 9. UART Interfacing Schemes

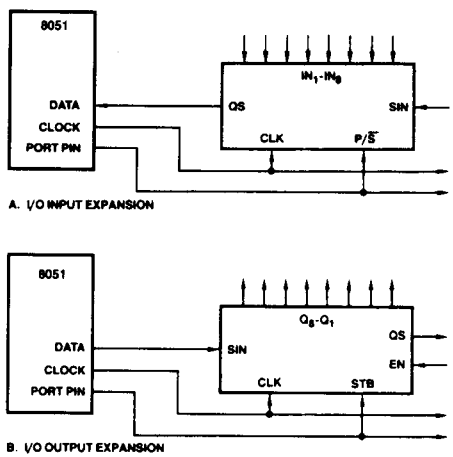

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Figure 10. I/O Expansion Technique

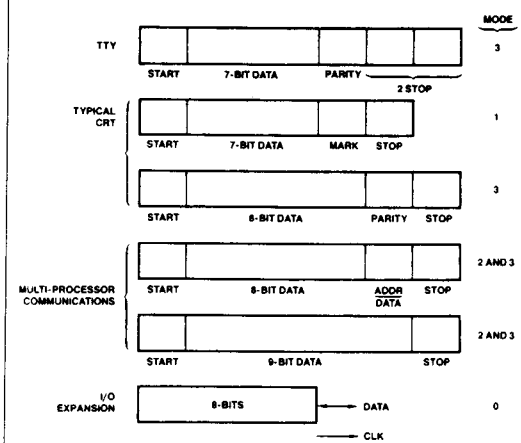

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Figure 11. Typical Frame Formats

Distributed processing offers a faster, more powerful system than a single CPU can provide. This results from hierarchy of interconnected processsors, each with its own memories and I/O. In a multiprocessing environment, a single host 8051 controls other slave 8051s configured to operate simultaneously on separate portions of a program. The interconnected 8051s reduce the load on the host processor and result in a lower-cost system of data transmission. This form of distributed processing is especially effective in a complex process where controls are required at physically separated locations.

In Modes 2 and 3 interprocessor communication is facilitated by the automatic wake-up of slave processors through interrupt driven address-frame recognition. The protocol for interprocessor communications is shown in Table 1. In synchronous mode (Mode 0) the high speed serial port provides an efficient, low-cost method of expanding I/O lines using standard TTL and CMOS shift registers. The serial channel provides a clock output for synchronizing the shifting of bits to/from an external register. The data rate is a division by 12 of the oscillator frequency and hence is 1M bits per second at 12 MHz.

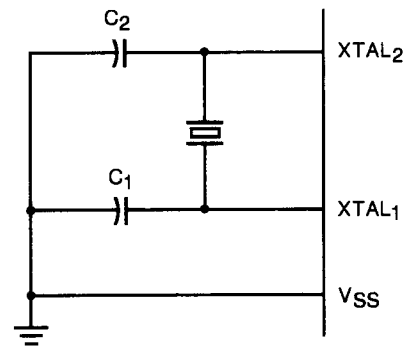
TABLE 1. PROTOCOL FOR MULTI-PROCESSOR COMMUNICATIONS

Slaves	Configure serial port to interrupt CPU if the received ninth data bit is a one (1).
Master	Transmit frame containing address in first 8 data bits and set ninth data bit (i.e., ninth data bit designates address frame).
Slaves	Serial port interrupts CPU when address frame is received. Interrupt service program compares received address to its address. The slave which has been addressed reconfigures its serial port to interrupt the CPU on all subsequent transmissions.
Master	Transmit control frames and data frames (these will be accepted only by the previously addressed slave).

Oscillator Characteristics

$XTAL_1$ and $XTAL_2$ are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 12. Either a quartz crystal or ceramic resonator may be used.

To drive the device from an external clock source, $XTAL_1$ should be grounded, while $XTAL_2$ is driven, as shown in Figure 13. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum HIGH and LOW times specified on the data sheet must be observed.



C_1, C_2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 12. Oscillator Connections

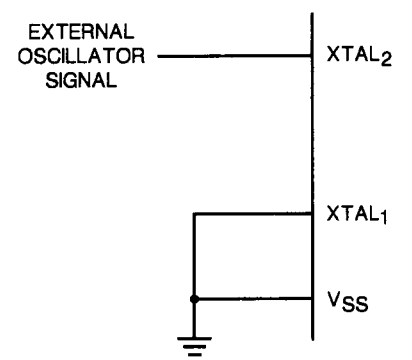


Figure 13. External Drive Configuration

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Voltage on Any Pin
with Respect to Ground ..... −0.5 to +7.0 V
Power Dissipation ..... 1 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.5 to +5.5 V
Ground (V_{SS}) ..... 0 V

Industrial (I) Devices (8031AH only)
Temperature (T_A) ..... −40 to +85°C
Supply Voltage (V_{CC}) ..... +4.5 to +5.5 V
Ground (V_{SS}) ..... 0 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameters	Description		Test Conditions	Min.	Max.	Units
V_{IL}	Input LOW Voltage			−0.5	0.8	V
V_{IH}	Input HIGH Voltage (Except RST/V_{PD} and $XTAL_2$)			2.0	V_{CC} +0.5	V
V_{IH1}	Input HIGH Voltage to RST/V_{PD}, $XTAL_2$		$XTAL_1 = V_{SS}$	2.5	V_{CC} +0.5	V
V_{PD}	Power-Down Voltage to RST/V_{PD}		V_{CC} = 0 V	4.5	5.5	V
V_{OL}	Output LOW Voltage, Ports 1, 2, 3 (Note 1)		I_{OL} = 1.6 mA		0.45	V
V_{OL1}	Output LOW Voltage, Port 0, ALE, $\overline{PSEN}$ (Note 1)		I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output HIGH Voltage, Ports 1, 2, 3		I_{OH} = −80 μA	2.4		V
V_{OH1}	Output HIGH Voltage, Port 0, ALE, $\overline{PSEN}$		I_{OH} = −400 μA	2.4		V
I_{IL}	Logical 0 Input Current, Ports 1, 2, 3		V_{IL} = 0.45 V		−500	μA
I_{IL2}	Logical 0 Input Current for $XTAL_2$		$XTAL_1 = V_{SS}$ V_{IN} = 0.45 V		−3.2	mA
I_{IH1}	Input HIGH Current to RST/V_{PD} for Reset		$V_{IN} < (V_{CC} - 1.5\ V)$		500	μA
I_{LI}	Input Leakage Current to Port 0, $\overline{EA}$		$0.45 < V_{IN} < V_{CC}$		±10	μA
I_{CC}	Power-Supply Current	8051AH/8031AH/ 8053AH	$\overline{EA} = V_{CC}$		125	mA
			All Outputs Disconnected		160	
I_{PD}	Power-Down Current		V_{CC} = 0 V; V_{PO} = 5.0 V		10	mA
C_{IO}	Capacitance of I/O Buffer		fc = 1 MHz		10	pF

Notes: 1. Capacitive load on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL}s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.

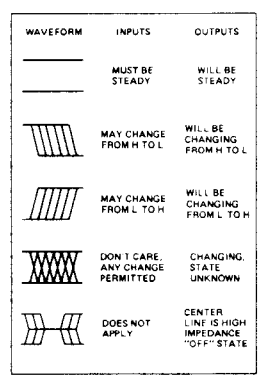
SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Load Capacitance for Port 0, ALE, and $\overline{PSEN}$ = 100 pF; Load Capacitance for all other outputs = 80 pF)

Parameter Symbol	Parameter Description	12 MHz Clock		18 MHz Clock (Note 1)		Variable Clock		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
TCY 1/TCLCL	Oscillator Frequency					1.2	18	MHz
TLHLL	ALE Pulse Width	127		71		2TCLCL-40		ns
TAVLL	Address Setup to ALE	43		15		TCLCL-40		ns
TLLAX	Address Hold After ALE	48		20		TCLCL-35		ns
TLLIV	ALE to Valid Instruction In		233		122		4TCLCL-100	ns
TLLPL	ALE to $\overline{PSEN}$	58		30		TCLCL-25		ns
TPLPH	$\overline{PSEN}$ Pulse Width	215		131		3TCLCL-35		ns
TPLIV	$\overline{PSEN}$ to Valid Instruction In		125		41		3TCLCL-125	ns
TPXIX	Input Instruction Hold After $\overline{PSEN}$	0		0		0		ns
TPXIZ	Input Instruction Float After $\overline{PSEN}$		63		35		TCLCL-20	ns
TPXAV	Address Valid After $\overline{PSEN}$	75		47		TCLCL-8		ns
TAVIV	Address to Valid Instruction In		302		162		5TCLCL-115	ns
TPLAZ	Address Float After $\overline{PSEN}$		20		20		20	ns
TRLRH	$\overline{RD}$ Pulse Width	400		233		6TCLCL-100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		233		6TCLCL-100		ns
TRLDV	$\overline{RD}$ to Valid Data In		250		112		5TCLCL-165	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		0		ns
TRHDZ	Data Float After $\overline{RD}$		97		41		2TCLCL-70	ns
TLLDV	ALE to Valid Data In		517		294		8TCLCL-150	ns
TAVDV	Address to Valid Data In		585		334		9TCLCL-165	ns
TLLWL	ALE to $\overline{WR}$ or $\overline{RD}$	200	300	116	216	3TCLCL-50	3TCLCL+50	ns
TAVWL	Address to $\overline{WR}$ or $\overline{RD}$	203		92		4TCLCL-130		ns
TQVWX	Data Valid to $\overline{WR}$ Transition	23		0		TCLCL-60		ns
TQVWH	Data Setup Before $\overline{WR}$	433		238		7TCLCL-150		ns
TWHQX	Data Hold After $\overline{WR}$	33		5		TCLCL-50		ns
TRLAZ	Address Float After $\overline{RD}$		20		20		20	ns
TWHLH	$\overline{WR}$ or $\overline{RD}$ High to ALE High	43	123	16	96	TCLCL-40	TCLCL+40	ns

Notes: 1. 18 MHz clock pertains only to 8031AH in the Commercial operating range.

SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS



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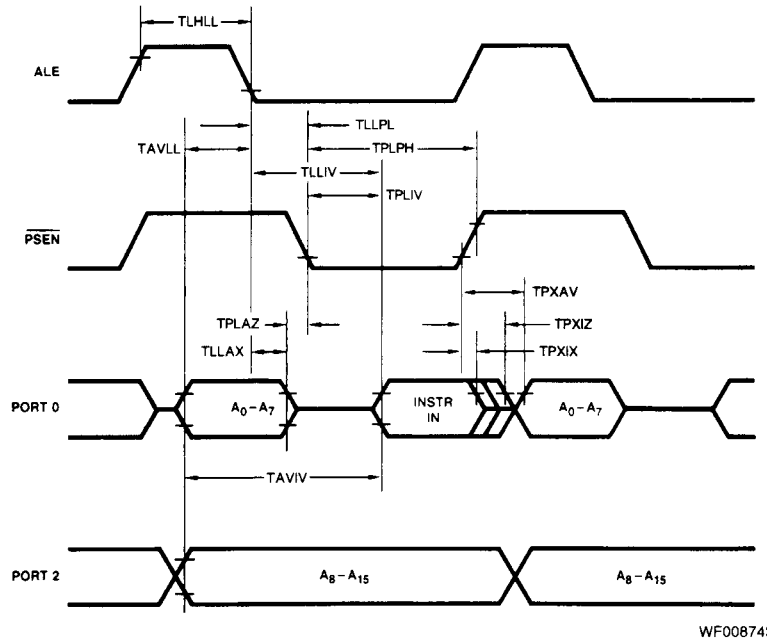
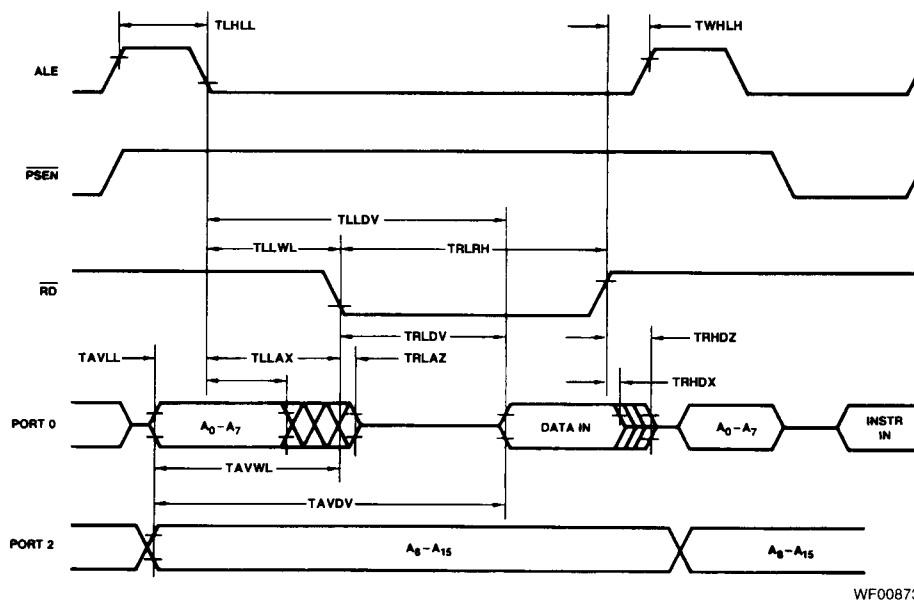
SWITCHING WAVEFORMS (Cont'd.)

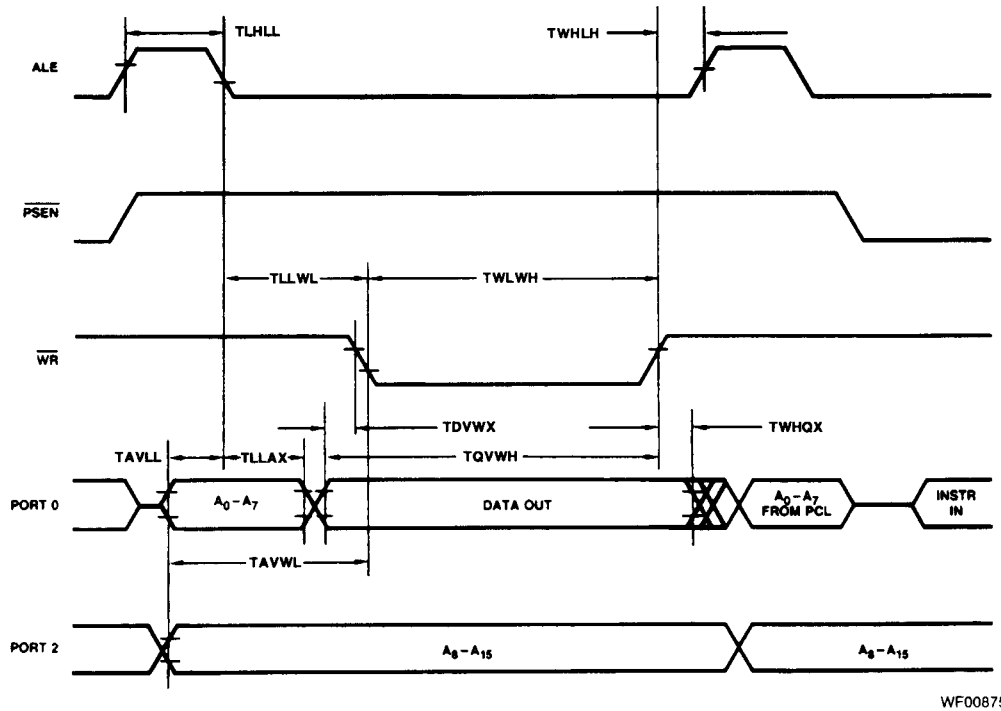


External Program Memory Read Cycle



External Data Memory Read Cycle

SWITCHING WAVEFORMS (Cont'd.)



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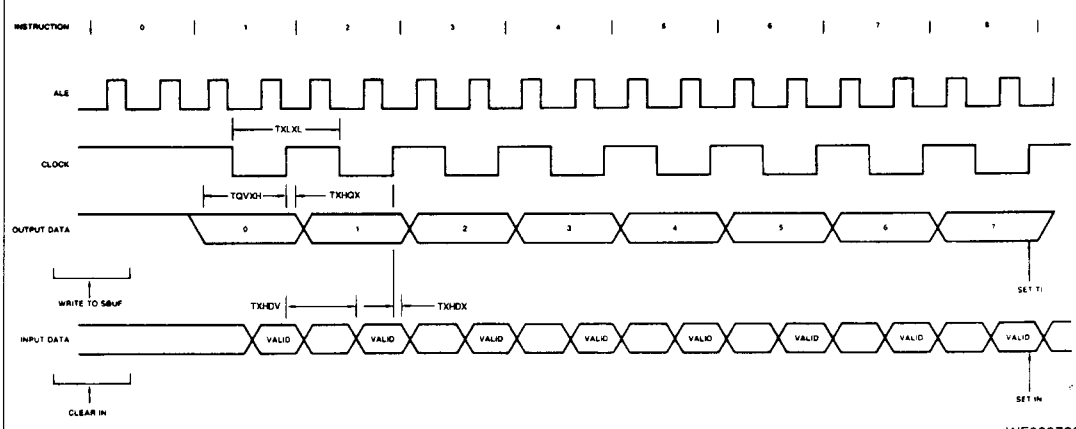
External Data Memory Write Cycle

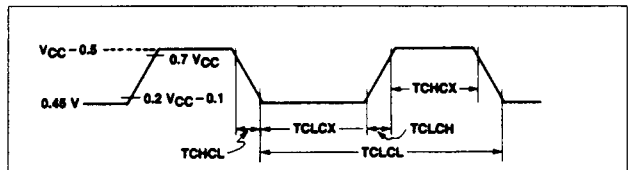


WF008722

Shift Register Timing Waveforms

EXTERNAL CLOCK DRIVE

Parameter Symbol	Parameter Description	Min.	Max.	Units
1/TCLCL	Oscillator Frequency	1.2	12	MHz
TCHCX	HIGH Time	20		ns
TCLCX	LOW Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns



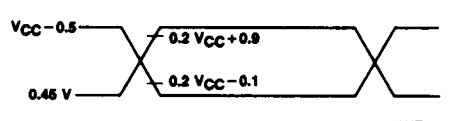
External Clock Drive Waveform

SERIAL PORT TIMING — SHIFT REGISTER MODE

(Load Capacitance = 80 pF)

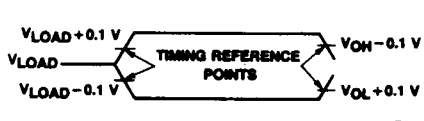
Parameter Symbol	Parameter Description	12 MHz Osc.		Variable Oscillator		Units
		Min.	Max.	Min.	Max.	
TXLXL	Serial Port Clock Cycle Time	1.0		12TCLCL		μs
TQVXH	Output Data Setup to Clock Rising Edge	700		10TCLCL - 133		ns
TXHQX	Output Data Hold After Clock Rising Edge	50		2TCLCL - 117		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		10TCLCL - 133	ns

AC Testing



AC INPUTS DURING TESTING ARE DRIVEN AT V_{CC} - 0.5 FOR A LOGIC "1" AND 0.45 V FOR A LOGIC "0." TIMING MEASUREMENTS ARE MADE AT V_{IH} MIN. FOR A LOGIC "1" AND V_{IL} MAX. FOR A LOGIC "0."

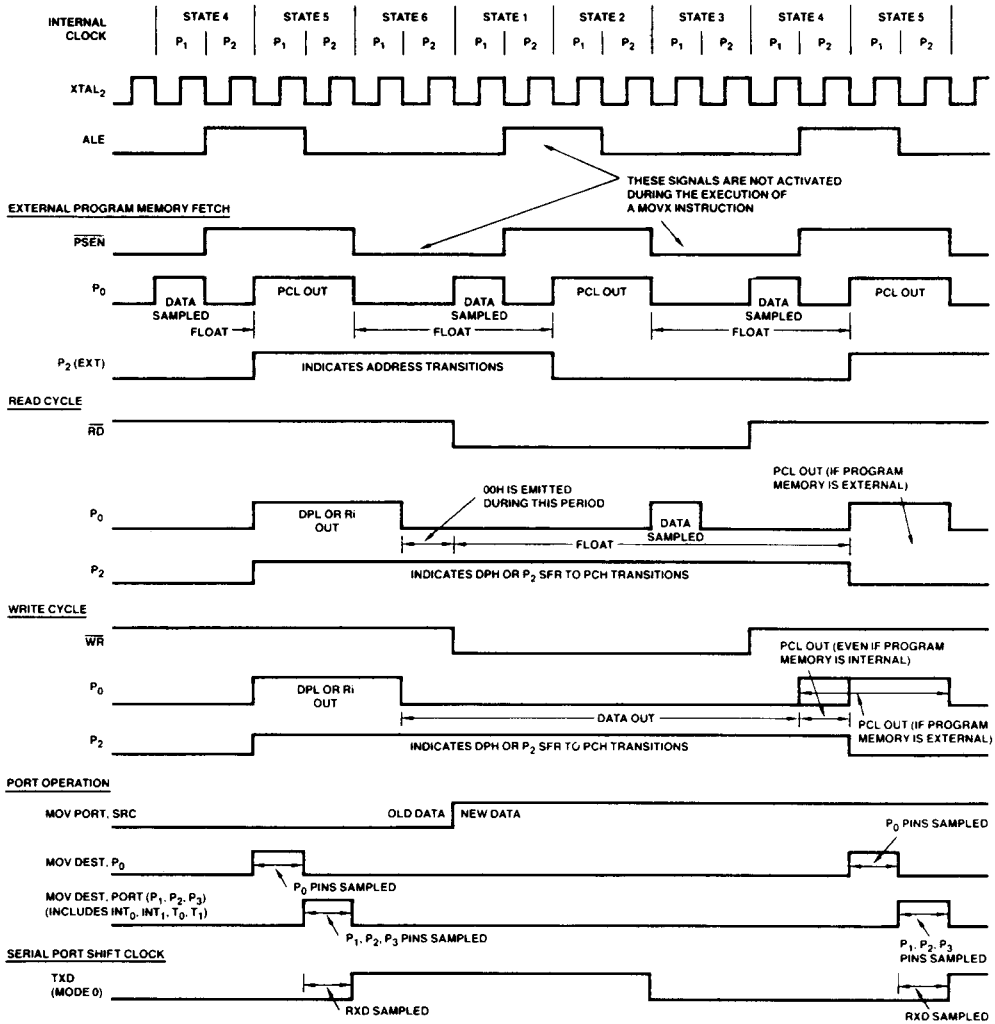
Input/Output Waveform



FOR TIMING PURPOSES A PORT PIN IS NO LONGER FLOATING WHEN A 100 mV CHANGE FROM LOAD VOLTAGE OCCURS, AND BEGINS TO FLOAT WHEN A 100 mV CHANGE FROM THE LOADED V_{OH}/V_{OL} LEVEL OCCURS. $I_{OL}/I_{OH} \geq \pm 20$ mA.

Float Waveform

CLOCK WAVEFORMS



WF007070

All internal timing is referenced to the internal time state shown on the top of the page. This waveform represents the signal on the X_2 input of the oscillator. This diagram represents when these signals are actually clocked within the chip. However, the time it takes a signal to propagate to the pins is in the range of 25 to 125 ns. Prop delays are dependent on many variables, such as temperature, pin loading. Propagation also varies from output to output and component to component. Typically though, /RD and /WR have prop delays of approximately 50 ns and the other timing signals approximately 85 ns, at room temperature, fully loaded. These differences in prop delays between signals have been integrated into the timing specs.

TABLE 3. 8051 FAMILY INSTRUCTION SET

Instructions That Affect Flag Setting*

Instruction	Flag			Instruction	Flag		
	C	OV	AC		C	OV	AC
ADD	X	X	X	CLR C	O		
ADDC	X	X	X	CPL C	X		
SUBB	X	X	X	ANL C, bit	X		
MUL	O	X		ANL C,/bit	X		
DIV	O	X		ORL C, bit	X		
DA	X			ORL C,/bit	X		
RRC	X			MOV C, bit	X		
RLC	X			CJNE	X		
SETB C	1						

Interrupt Response Time: To finish execution of current instruction, respond to the interrupt request and push the PC; to vector to the first instruction of the interrupt service program requires 38 to 81 oscillator periods (3 to 7 μs @ 12 MHz).

*Note that operations on SFR byte address 208 or bit addresses 209 – 215 (i.e., the PSW or bits in the PSW) will also affect flag settings.

DATA TRANSFER

Mnemonic		Description	Byte	Cyc
MOV	A,Rn	Move register to Accumulator	1	1
MOV	A,direct	Move direct byte to Accumulator	2	1
MOV	A,@Ri	Move indirect RAM to Accumulator	1	1
MOV	A,#data	Move immediate data to Accumulator	2	1
MOV	Rn,A	Move Accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move Accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct byte	3	2
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move Accumulator to indirect RAM	1	1
MOV	@Ri,direct	Mode direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data16	Move 16-bit constant to Data Pointer	3	2
MOVC	A,@A + DPTR	Move Code byte relative to DPTR to Accumulator	1	2
MOVC	A,@A + PC	Move Code byte relative to PC to Accumulator	1	2
MOVX	A,@Ri	Move External RAM (8-bit address) to Accumulator	1	2
MOVX	A,@DPTR	Move External RAM (16-bit address) to Accumulator	1	2
MOVX	@Ri,A	Move Accumulator to External RAM (8-bit address)	1	2
MOVX	@DPTR,A	Move Accumulator to External RAM (16-bit address)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte off of stack	2	2
XCH	A,Rn	Exchange register with Accumulator	1	1
XCH	A,direct	Exchange direct byte with Accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with Accumulator	1	1
XCHD	A,@Ri	Exchange indirect RAM's least sig nibble with A's LSN	1	1

BOOLEAN VARIABLE MANIPULATION

Mnemonic		Description	Byte	Cyc
CLR	C	Clear Carry Flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set Carry Flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement Carry Flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to Carry Flag	2	2
ANL	C,/bit	AND complement of direct bit to Carry	2	2
ORL	C,bit	OR direct bit to Carry Flag	2	2
ORL	C,/bit	OR complement of direct bit to Carry	2	2
MOV	C,bit	Move direct bit to Carry Flag	2	1
MOV	bit,C	Move Carry flag to direct bit	2	2

LOGIC (Cont'd.)

Mnemonic		Description	Byte	Cyc
ANL	A,Rn	AND register to Accumulator	1	1
ANL	A,direct	AND direct byte to Accumulator	2	1
ANL	A,@Ri	AND indirect RAM to Accumulator	1	1
ANL	A,#data	AND immediate data to Accumulator	2	1
ANL	direct,A	AND Accumulator to direct byte	2	1

LOGIC (Cont'd.)

Mnemonic		Description	Byte	Cyc
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to Accumulator	1	1
ORL	A,direct	OR direct byte to Accumulator	2	1
ORL	A,@Ri	OR indirect RAM to Accumulator	1	1
ORL	A,#data	OR immediate data to Accumulator	2	1
ORL	direct,A	OR Accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive-OR register to Accumulator	1	1
XRL	A,direct	Exclusive-OR direct byte to Accumulator	2	1
XRL	A,@Ri	Exclusive-OR indirect RAM to Accumulator	1	1
XRL	A,#data	Exclusive-OR immediate data to Accumulator	2	1
XRL	direct,A	Exclusive-OR Accumulator to direct byte	2	1
XRL	direct,#data	Exclusive-OR immediate data to direct	3	2
CLR	A	Clear Accumulator	1	1
CPL	A	Complement Accumulator	1	1
RL	A	Rotate Accumulator Left	1	1
RLC	A	Rotate Accumulator Left through Carry Flag	1	1
RR	A	Rotate Accumulator Right	1	1
RRC	A	Rotate Accumulator Right through Carry Flag	1	1
SWAP	A	Exchange nibbles within the Accumulator	1	1

ARITHMETIC

Mnemonic		Description	Byte	Cyc
ADD	A,Rn	Add register to Accumulator	1	1
ADD	A,direct	Add direct byte to Accumulator	2	1
ADD	A,@Ri	Add indirect RAM to Accumulator	1	1
ADD	A,#data	Add immediate data to Accumulator	2	1
ADDC	A,Rn	Add register to Accumulator with carry	1	1
ADDC	A,direct	Add direct byte to Accumulator with Carry Flag	2	1
ADDC	A,@Ri	Add indirect RAM and Carry Flag to Accumulator	1	1
ADDC	A,#data	Add immediate data and Carry Flag to Accumulator	2	1
SUBB	A,Rn	Subtract register from Accumulator with Borrow	1	1
SUBB	A,direct	Subtract direct byte from Accumulator with Borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from Accumulator with Borrow	1	1
SUBB	A,#data	Subtract immediate data from Accumulator with Borrow	2	1
INC	A	Increment Accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement Accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment Data Pointer	1	2
MUL	AB	Multiply Accumulator times B	1	4
DIV	AB	Divide Accumulator by B	1	4
DA	A	Decimal Adjust Accumulator	1	1

OTHER

Mnemonic	Description	Byte	Cyc
NOP	No Operation	1	1

CONTROL TRANSFER (BRANCH)				
Mnemonic		**Description**	**Byte**	**Cyc**
AJMP	addr11	Absolute Jump	2	2
LJMP	addr16	Long Jump	3	2
SJMP	rel	Short Jump (relative addr)	2	2
JMP	@A + DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if Accumulator is zero	2	2
JNZ	rel	Jump if Accumulator is not zero	2	2
JC	rel	Jump if Carry Flag is set	2	2
JNC	rel	Jump if carry is not set	2	2
JB	bit,rel	Jump relative if direct bit is set	3	2
JNB	bit,rel	Jump relative if direct bit is not set	3	2
JBC	bit,rel	Jump relative if direct bit is set, then clear bit	3	2
CJNE	A,direct,rel	Compare direct byte to Accumulator and Jump if not Equal	3	2
CJNE	A,#data,rel	Compare immediate to Accumulator and Jump if not Equal	3	2
CJNE	Rn,#data,rel	Compare immediate to reg and Jump if not Equal	3	2
CJNE	@Ri,#data,rel	Compare immediate to indirect RAM and Jump if not Equal	3	2
DJNZ	Rn,rel	Decrement register and Jump if not zero	2	2
DJNZ	direct,rel	Decrement direct byte and Jump if not zero	3	2

CONTROL TRANSFER (SUBROUTINE)				
Mnemonic		**Description**	**Byte**	**Cyc**
ACALL	addr11	Absolute Subroutine Call	2	2
LCALL	addr16	Long Subroutine Call	3	2
RET		Return from Subroutine Call	1	2
RETI		Return from Interrupt Call	1	2

Notes on Data Addressing Modes:

- Rn –Working register R0 – R7 of the currently selected Register bank.
- direct –128 internal RAM locations, any I/O port, control, or status register.
- @Ri –Indirect internal RAM location addressed by register R0 or R1.
- #data –8-bit constant included in instruction.
- #data16 –16-bit constant included as bytes 2 and 3 of instruction.
- bit –128 software flags, any I/O pin, control, or status bit.

Notes on Program Addressing Modes:

- addr16 –Destination address for LCALL and LJMP may be anywhere within the 64-Kilobyte program memory address space.
- addr11 –Destination address for ACALL and AJMP will be within the same 2-Kilobyte page of program memory as the first byte of the following instruction.
- rel –SJMP and all conditional jumps include as 8-bit offset by Range is +127, –128 bytes relative to first byte of the following instruction.

TABLE 4. INSTRUCTION OPCODES IN HEXADECIMAL ORDER (Cont'd.)

Hex Code	Bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	Code addr
02	3	LJMP	Code addr
03	1	RR	A
04	1	INC	A
05	2	INC	Data addr
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	Bit addr,code addr
11	2	ACALL	Code addr
12	3	LCALL	Code addr
13	1	RRC	A
14	1	DEC	A
15	2	DEC	Data addr
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	Bit addr,code addr
21	2	AJMP	Code addr
22	1	RET	
23	1	RL	A
24	2	ADD	A,#data
25	2	ADD	A,data addr
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	Bit addr,code addr
31	2	ACALL	Code addr
32	1	RETI	
33	1	RLC	A
34	2	ADDC	A,#data
35	2	ADDC	A,data addr
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R6
3F	1	ADDC	A,R7
40	2	JC	Code addr
41	2	AJMP	Code addr
42	2	ORL	Data addr,A
43	3	ORL	Data addr,#data
44	2	ORL	A,#data
45	2	ORL	A,data addr
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	Code addr
51	2	ACALL	Code addr
52	2	ANL	Data addr,A
53	3	ANL	Data addr,#data
54	2	ANL	A,#data
55	2	ANL	A,data addr
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3

Hex Code	Bytes	Mnemonic	Operands
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	Code addr
61	2	AJMP	Code addr
62	2	XRL	Data addr,A
63	3	XRL	Data addr,#data
64	2	XRL	A,#data
65	2	XRL	A,data addr
66	1	XRL	A,@R0
67	1	XRL	A,@R1
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	Code addr
71	2	ACALL	Code addr
72	2	ORL	C,bit addr
73	1	JMP	@A +DPTR
74	2	MOV	A,#data
75	3	MOV	Data addr,#data
76	2	MOV	@R0,#data
77	2	MOV	@R1,#data
78	2	MOV	R0,#data
79	2	MOV	R1,#data
7A	2	MOV	R2,#data
7B	2	MOV	R3,#data
7C	2	MOV	R4,#data
7D	2	MOV	R5,#data
7E	2	MOV	R6,#data
7F	2	MOV	R7,#data
80	2	SJMP	Code addr
81	2	AJMP	Code addr
82	2	ANL	C,bit addr
83	1	MOVC	A,@A +PC
84	1	DIV	AB
85	3	MOV	Data addr,data addr
86	2	MOV	Data addr,@R0
87	2	MOV	Data addr,@R1
88	2	MOV	Data addr,R0
89	2	MOV	Data addr,R1
8A	2	MOV	Data addr,R2
8B	2	MOV	Data addr,R3
8C	2	MOV	Data addr,R4
8D	2	MOV	Data addr,R5
8E	2	MOV	Data addr,R6
8F	2	MOV	Data addr,R7
90	3	MOV	DPTR,#data
91	2	ACALL	Code addr
92	2	MOV	Bit addr,C
93	1	MOVC	A,@A +DPTR
94	2	SUBB	A,#data
95	2	SUBB	A,data addr
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/bit addr
A1	2	AJMP	Code addr
A2	2	MOV	C,bit addr
A3	1	INC	DPTR
A4	1	MUL	AB
A5		Reserved	
A6	2	MOV	@R0,data addr
A7	2	MOV	@R1,data addr
A8	2	MOV	R0,data addr
A9	2	MOV	R1,data addr
AA	2	MOV	R2,data addr
AB	2	MOV	R3,data addr
AC	2	MOV	R4,data addr
AD	2	MOV	R5,data addr
AE	2	MOV	R6,data addr
AF	2	MOV	R7,data addr
B0	2	ANL	C,/bit addr
B1	2	ACALL	Code addr
B2	2	CPL	Bit addr
B3	1	CPL	C
B4	3	CJNE	A,#data,code addr
B5	3	CJNE	A,data addr,code addr
B6	3	CJNE	@R0,#data,code addr
B7	3	CJNE	@R1,#data,code addr
B8	3	CJNE	R0,#data,code addr
B9	3	CJNE	R1,#data,code addr
BA	3	CJNE	R2,#data,code addr
BB	3	CJNE	R3,#data,code addr
BC	3	CJNE	R4,#data,code addr
BD	3	CJNE	R5,#data,code addr
BE	3	CJNE	R6,#data,code addr
BF	3	CJNE	R7,#data,code addr
C0	2	PUSH	Data addr
C1	2	AJMP	Code addr
C2	2	CLR	Bit addr
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,data addr
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7
D0	2	POP	Data addr
D1	2	ACALL	Code addr
D2	2	SETB	Bit addr
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	Data addr,code addr
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,code addr
D9	2	DJNZ	R1,code addr
DA	2	DJNZ	R2,code addr
DB	2	DJNZ	R3,code addr
DC	2	DJNZ	R4,code addr
DD	2	DJNZ	R5,code addr
DE	2	DJNZ	R6,code addr
DF	2	DJNZ	R7,code addr
E0	1	MOVX	A,@DPTR
E1	2	AJMP	Code addr
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,data addr
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	Code addr
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	Data addr,A
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

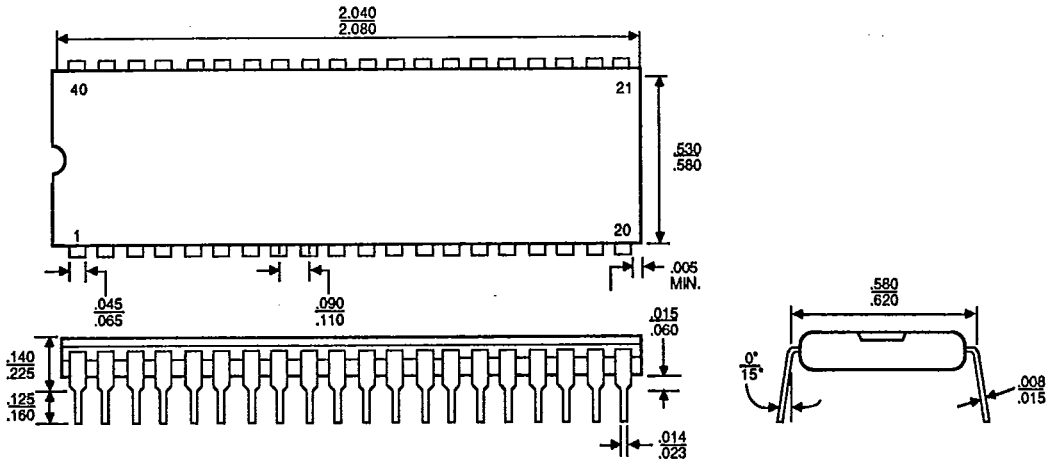
CHAPTER 12

Package Outlines

T-90-20

PHYSICAL DIMENSIONS*

Plastic Dual-In-Line Package (PD)
PD 040



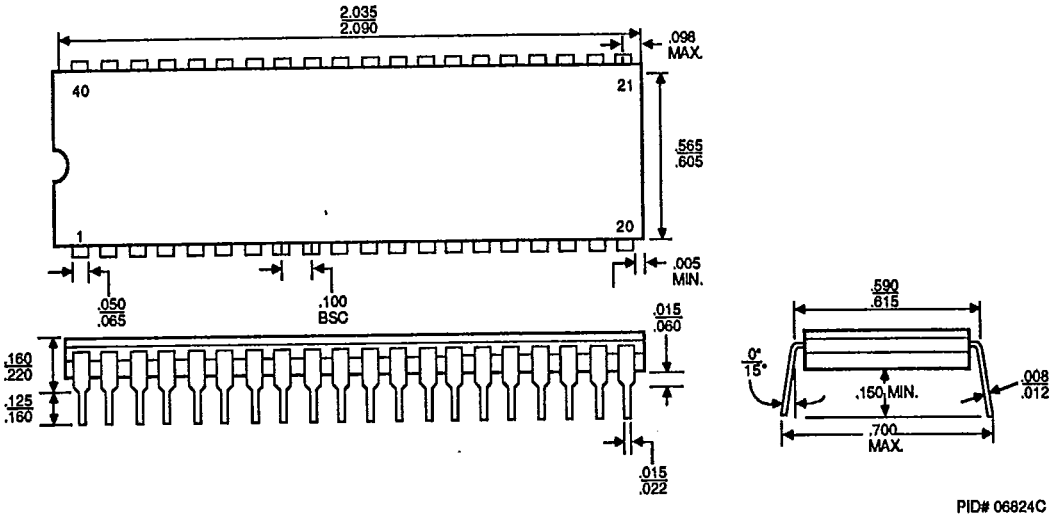
PID# 06823B

* For reference only.

NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.

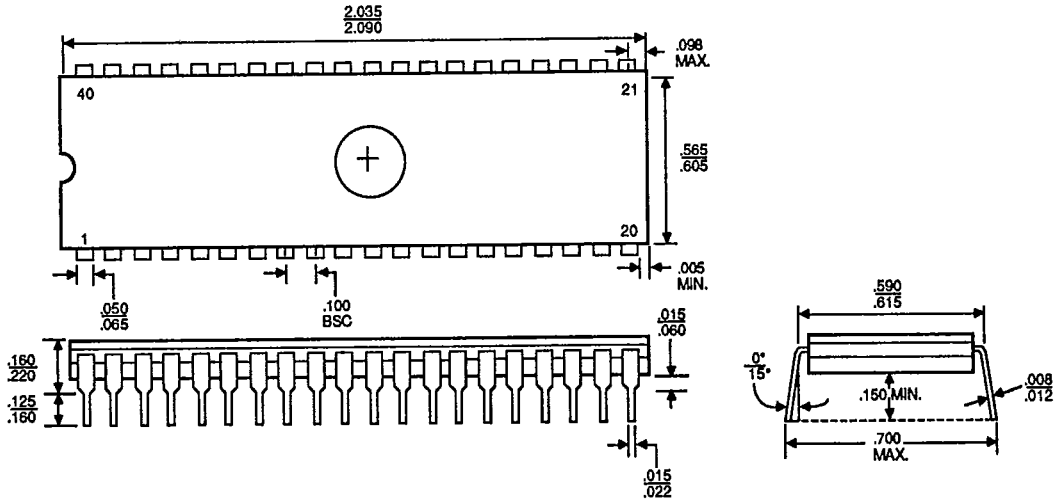
Ceramic Hermetic Dual-In-Line Packages (CD/CDV)

CD 040



PID# 06824C

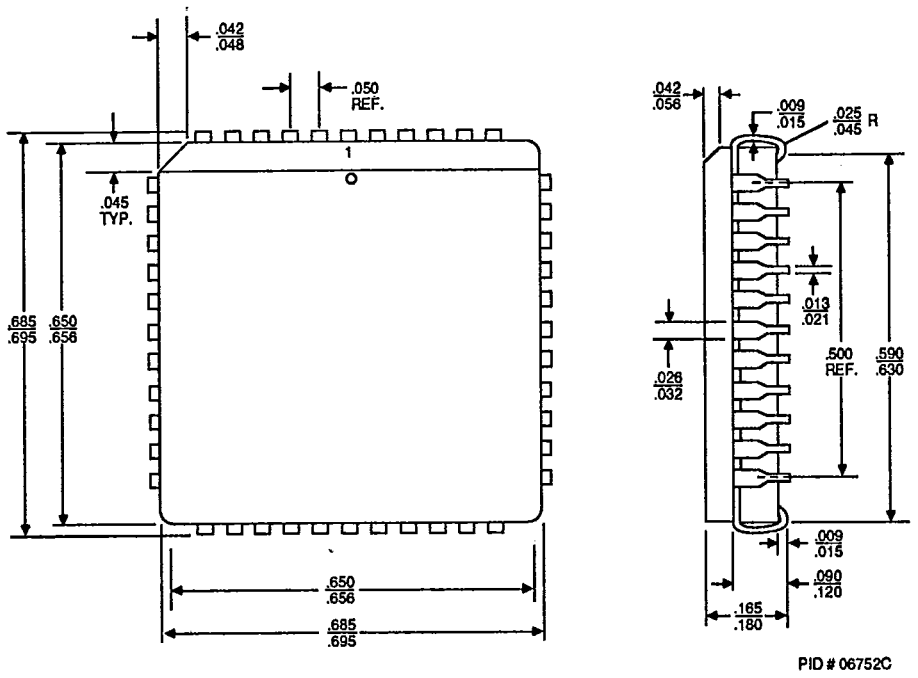
CDV 040



PID# 07880B

NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.

Plastic Leaded Chip Carrier (PL)
PL 044

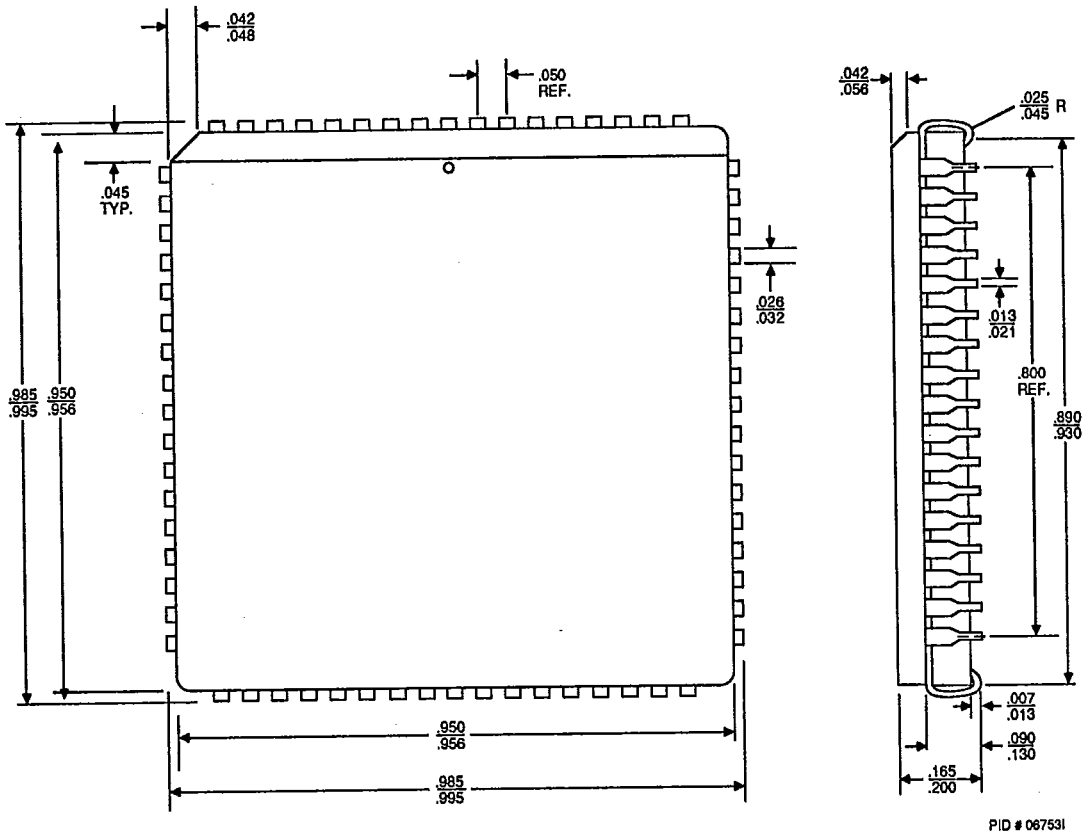


PID # 06752C

NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.

Plastic Leaded Chip Carrier (PL) (Continued)

PL 068

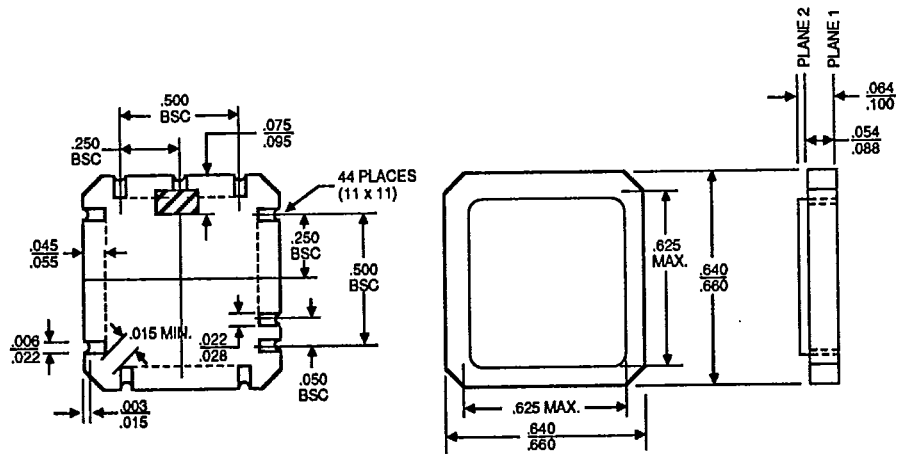


NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.

Ceramic Leadless Chip Carriers (CL/CLV)

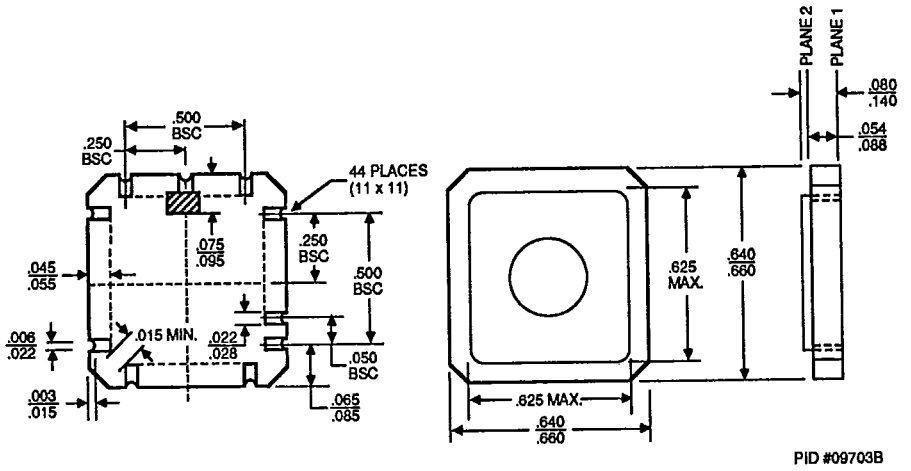
T-90-20

CL 044



PID #06825E

CLV 044



PID #09703B

NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.