82285
CLOCK GENERATOR AND READY INTERFACE FOR I/O COPROCESSORS

82285 is an 18 pin bipolar clock generator/driver designed to provide clock signals for the 82730, 82586, or other master peripherals. It also contains READY multiplexing logic to provide the required RDYO and READY timing and synchronization for the peripheral chips. RESET logic with hysteresis and synchronization is also provided.

- **Uses crystal or TTL signal for Frequency Source.**
- **Provides a 50% duty cycle peripheral clock output with MOS drive characteristics.**
- **Provides synchronous READY for peripherals from synchronous and/or asynchronous sources.**
- **Generates system reset output from Schmitt Trigger input.**
- **Capable of clock synchronization with other 82285's.**

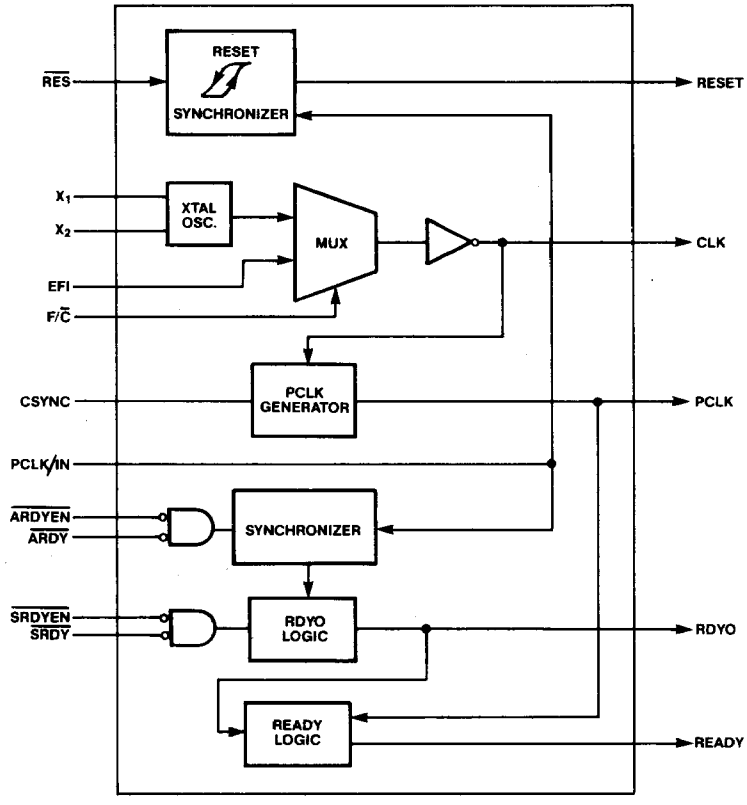

Figure 1. 82285 Block Diagram

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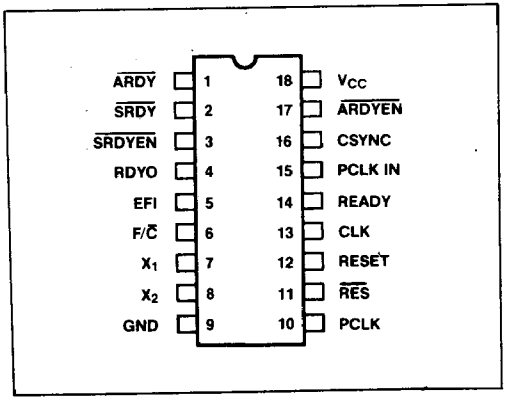

Figure 2. 82285 Pin Configuration

NOTE

1. CLK is a TTL level output and has the same frequency as either the crystal or EFI, depending on the state of F/C.
2. PCLK is a MOS level output and has half the frequency of CLK.
3. ARDY and ARDYEN are interchangeable.
4. SRDY and SRDYEN are interchangeable.

FUNCTIONAL DESCRIPTION

Clock Generator

The CLK and PCLK clock outputs may be generated either by an external crystal or by an external TTL frequency input. If the frequency/crystal select input (F/C) is high, the EFI input is used. If F/C is low, a crystal attached to X_1 and X_2 pins is used. CLK is a TTL output at the crystal or EFI frequency. PCLK is a MOS-level output which has a 50% duty cycle, operates at 1/2 the CLK frequency, and can be used to drive the clock inputs of the 82586, 82730, or other devices.

Reset Logic

The reset logic provides a Schmitt Trigger input (RES) and two synchronization flip-flops to synchronize the reset timing. The reset signal is synchronized at the falling edge of PCLK IN. A simple RC network can be used to provide power-on reset of proper duration.

Table 1. Pin Description

Symbol	Pin Number	Type	Name and Function
RES	11	I	RESET IN: RES is an active low signal which is used to generate RESET. A Schmitt trigger input is provided so that a RC connection can be used to establish the power up reset of proper duration.
RESET	12	O	RESET: RESET is an active high signal which is the synchronized version of the RES input.
X_1, X_2	7,8	I	CRYSTAL INPUT: X_1 and X_2 are attached to a parallel resonant, fundamental mode crystal. If F/C is strapped low to select the internal oscillator as the clock source, CLK will be the same frequency as the crystal, PCLK will be ½ that frequency.
CLK	13	O	CLOCK: CLK is a TTL output and has the same frequency as either the crystal or the external frequency input (EFI), dependent upon the state of F/C.
PCLK	10	O	PERIPHERAL CLOCK: PCLK is a clock output at half the frequency of the crystal input or EFI, depending on F/C input. It provides MOS levels to drive the system CLK inputs of 82586 or 82730 or other device. PCLK has a 50% duty cycle.
PCLK IN	15	I	PERIPHERAL CLOCK IN: PCLK IN is a clock input which is used for clocking the RESET flip-flops and the ARDY synchronizing flip-flop. It can be driven by the PCLK output or some other system clock.
F/C	6	I	FREQUENCY/CRYSTAL SELECT: F/C is a strapping option. When low, CLK and PCLK are generated from an external crystal. When high, CLK and PCLK are generated from the EFI input.

Table 1. Pin Description (Cont.)

Symbol	Pin Number	Type	Name and Function
EFI	5	I	EXTERNAL FREQUENCY IN: When F/$\overline{C}$ is strapped high, CLK and PCLK are generated from the EFI input. CLK will be the same frequency as EFI; PCLK will be half that frequency.
$\overline{ARDYEN}$	17	I	ASYNCHRONOUS READY ENABLE: $\overline{ARDYEN}$ is an asynchronous active low input which qualifies $\overline{ARDY}$. Set up and hold times are given only to guarantee recognition on that clock edge.
$\overline{ARDY}$	1	I	ASYNCHRONOUS READY: $\overline{ARDY}$ is an asynchronous active low input which will be synchronized to provide the RDYO output at the falling edge of PCLK IN. Setup and hold times are given only to guarantee recognition on that falling edge of PCLK IN. The RDYO output will also be a function of the $\overline{SRDY}$ input.
$\overline{SRDYEN}$	3	I	SYNCHRONOUS READY ENABLE: $\overline{SRDYEN}$ is a synchronous active low input which qualifies $\overline{SRDY}$.
$\overline{SRDY}$	2	I	SYNCHRONOUS READY: $\overline{SRDY}$ is a synchronous active low input. The RDYO outputs will also be a function of the $\overline{ARDY}$ input.
RDYO	4	O	SYNCHRONOUS READY OUT: RDYO is an active high output which is either the $\overline{SRDY}$ input delayed, or the $\overline{ARDY}$ input synchronized. RDYO will be inactive (low) if the ready inputs are inactive (high).
READY	14	O	READY: READY is an active high output which is the RDYO signal synchronized with the falling edge of PCLK output.
CSYNC	16	I	CLOCK SYNCHRONIZATION: CSYNC is used to provide synchronization of PCLK's among multiple 82285's. The source of CSYNC come from the PCLK output of the reference 82285. When synchronization is not used, CSYNC should be connected to V_{CC}.
GND	9	-	Ground.
V_{CC}	18	-	+5V supply.

RDYO and READY Logic

RDYO is determined by synchronous ready input $\overline{SRDY}$ qualified by $\overline{SRDYEN}$ or asynchronous ready input $\overline{ARDY}$ qualified by $\overline{ARDYEN}$. For the asynchronous input $\overline{ARDY}$, it will be clocked in at the falling edge of PCLK IN; and the RDYO output will become valid at the same falling edge of PCLK IN, provided $\overline{ARDY}$ is stable. The $\overline{ARDY}$ flip-flop is used as the first step in a two flip-flop synchronization method for RDYO. For the synchronous input $\overline{SRDY}$, the RDYO output will become valid when $\overline{SRDY}$ is stable.

The READY output is the RDYO output latched at the falling edge of PCLK out. It provides an additional ready signal in order to optimize the operation of systems using the 82730, 82586, and 8086.

WARNING:

The RDYO output is not fully synchronized when the asynchronous mode ($\overline{ARDY}$) is used.

Clock Synchronization Logic

The clock synchronization logic allows the PCLK signal of the device to be synchronized with the PCLK from other 82285's. A typical application of this synchronization logic is shown in Diagram 5. Diagram 3 and 4 illustrates typical functional sequences of 82285.

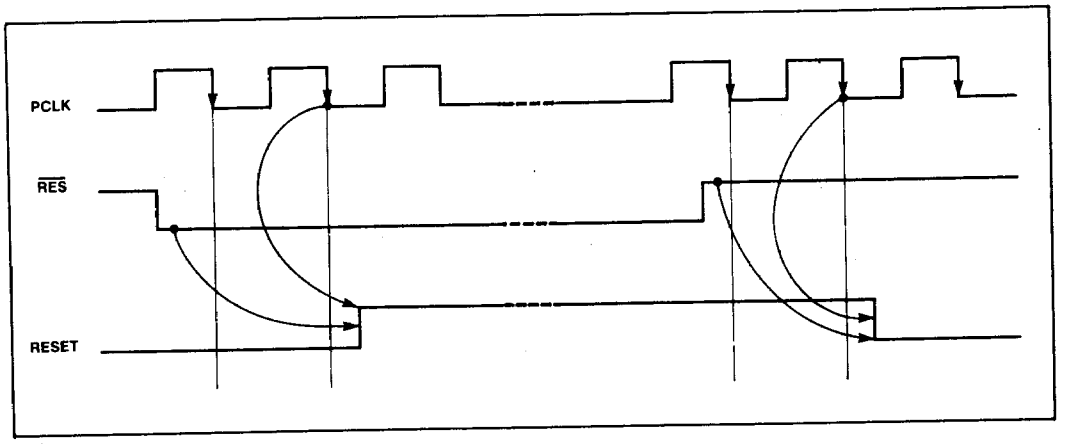

Figure 3. Reset Sequence

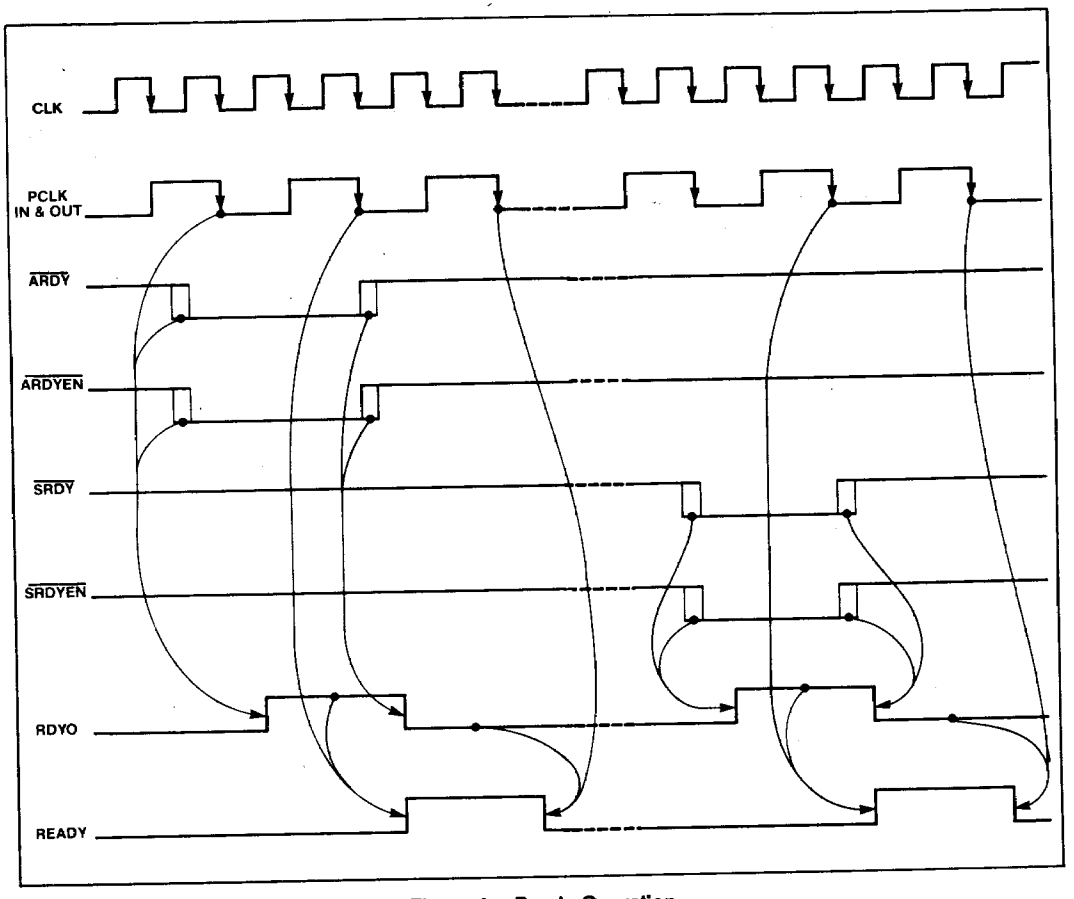

Figure 4. Ready Operation

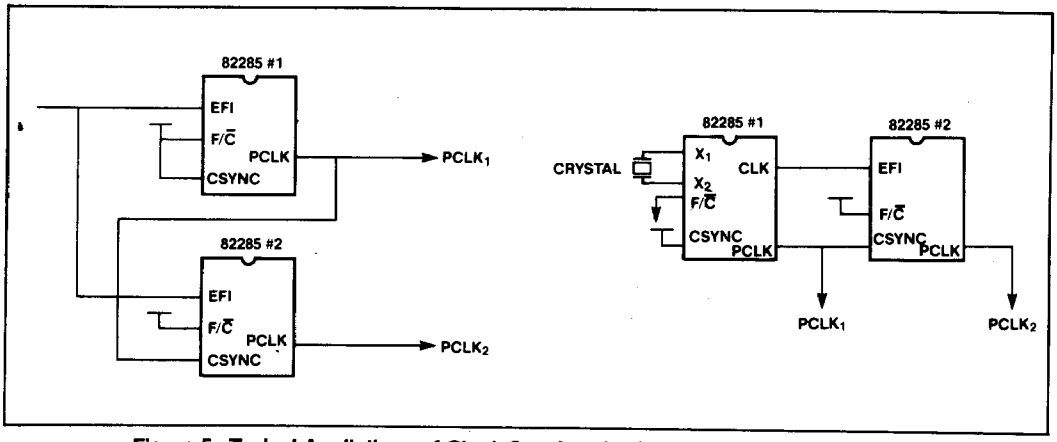

Figure 5. Typical Applictions of Clock Synchronization Among Multiple 82285's

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... −65°C to 150°C
Voltage on any Pin with Respect to Ground ..... −0.5V to +7V
Power Dissipation ..... 1.5 Watt

**NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Electrical Characteristics and Waveforms

D.C. Characteristics for 82285

Conditions: T_A = 0° C to 70° C; V_{CC} = 5V ± 10%

Symbol	Parameter	Min.	Max.	Units	Test Conditions
I_F	Forward Input Current		−0.5	mA	V_F = 0.45V
	For PCLK IN		−0.6	mA	V_F = 0.45V
	For $\overline{\text{SRDYEN}}$, $\overline{\text{SRDY}}$		−0.85	mA	V_F = 0.45V
I_R	Reverse Input Current		50	μA	$V_R = V_{CC}$
V_C	Input Forward Clamp voltage		−1.0	V	I_C = −5 mA
I_{CC}	Power Supply Current		145	mA	
V_{IL}	Input "low" voltage		0.8	V	
V_{IH}	Input "high" voltage	2.0			
V_{IHR}	Reset input "high" voltage	2.6		V	
V_{OL}	Output "low" voltage		0.45	V	I_{OL} = 5.25 mA
V_{OH}	Output "high" voltage PCLK	4.0		V	−1.05 mA
	Other outputs	2.4		V	−1.05 mA
V_{IHR}-V_{ILR}	$\overline{\text{RES}}$ Input Hysteresis	0.25			
C_i	Input Capacitance		10	pF	

82285 A.C. Characteristics (Cont.)

Condition: T_A = 0° C to 70° C; V_{CC} = %V ± 10% (Note 1)

Symbol	Parameter	Min.	Max.	Units	
t_R	CLK and PCLK rise time		10	ns	Note 2
t_F	CLK and PCLK fall time		10	ns	Note 2
t_L	PCLK IN and EFI low time	30		ns	
t_H	PCLK IN and EFI high time	30		ns	
t_1	CLK low time	1/2 t_3-15		ns	
t_2	CLK high time	1/2 t_3-15		ns	
t_3	CLK cycle time	56		ns	
t_4	PCLK low time @ 0.6V	t_3-12.5		ns	
	PCLK low time @ 1.5V	t_3-10		ns	
t_5	PCLK high time @ 3.8V	t_3-17.5		ns	
	PCLK high time @ 1.5V	t_3-10		ns	
t_6	PCLK cycle time	$2t_3$		ns	
t_7	$\overline{RES}$ setup time to PCLK I↓	15		ns	Note 3, 4
t_8	$\overline{RES}$ hold time from PCLK I↓	10		ns	Note 3, 4
t_9	PCLK delay from CLK low	0	40	ns	
t_{10}	RESET delay from PCLK low	0	50	ns	
t_{11}	$\overline{ARDYEN}$ setup time to $\overline{ARDY}$	0		ns	Note 4
t_{12}	$\overline{ARDYEN}$ hold time from $\overline{ARDY}$	0		ns	Note 4
t_{13}	$\overline{ARDY}$ setup time to PCLK I↓	0		ns	Note 3, 4
t_{14}	$\overline{ARDY}$ hold time from PCLK I↓		30	ns	Note 3, 4
t_{15}	$\overline{SRDYEN}$ setup time to $\overline{SRDY}$	0		ns	Note 4
t_{16}	$\overline{SRDYEN}$ hold time from $\overline{SRDY}$	0		ns	Note 4
t_{17}	$\overline{SRDY}$ setup time to PCLK↓		50	ns	
t_{18}	RDYO↑ delay from PCLK I↓		55	ns	
t_{19}	RDYO↓ delay from $\overline{ARDY}$↑		30	ns	
t_{20}	RDYO delay from $\overline{SRDY}$		30	ns	
t_{21}	READY↑ delay from PCLK↓	–20	0	ns	
t_{22}	READY↓ delay from PCLK↓	–20	8	ns	
	Crystal frequency	17.6	4	MHz	Note 6
	EFI frequency	D.C.	17.6	MHz	Note 5

(see notes next page)

NOTE

1. All times are measured at the 1.5V level unless specified otherwise.
2. The rise and fall times for CLK are measured between 0.8V and 2.0V (TTL level drive characteristics). The rise and fall times for PCLK are measured between 1.0V and 3.5V (MOS level drive characteristics).
3. These are asynchronous inputs.
4. The setup and hold times are measured at the 0.8V and 2.0V levels for the inputs and at 1.5V from the PCLK signal.
5. To assure proper operation, the rise time or fall time of EFI cannot exceed 100 ns.
6. The specified timings are given in accordance with the maximum operating fre quency of 17.6 MHz. However, the device will be designed to operate to 24 MHz with all timing specs to be determined.

Loading:

For READY OUTPUT:
C_L = 30 pf, I_{OL} = 5.25 mA, I_{OH} = –1.05 mA

For the CLK output:
C_L = 75 pf, I_{OL} = 5.25 mA, I_{OH} = –1.05 mA

For the RDYO output:
C_L = 75 pf, I_{OL} = 5.25 mA, I_{OH} = –1.05 mA

For the PCLK output:
C_L = 175 pf, I_{OL} = 5.25 mA, I_{OH} =-1.05 mA

All input capacitance will be:
C_i = 10 pf

WAVEFORMS.