Intel 8242BB
Technical Reference Manual

Version 1.0
August 15, 1994

Intel Order # 297545-001

DISCLAIMERS

This document is provided by Intel corporation "as is" with no warranties whatsoever, including any warranty of merchantability or fitness for any particular purpose. Product applications documented herein are provided only for convenience to the use in developing user's choice of design and implementation.

No license, express or implied, to any Intel patent or other intellectual property is granted or intended hereby.

Intel disclaims any liability, including liability for infringement of any patent or other proprietary rights, relating to implementation of information in this document. Intel does not warrant or represent that such implementation will not infringe on such rights.

Intel retains the right to make changes to this document at any time, without notice.

Additional copies of this document or other Intel literature may be obtained from:

Intel Corporation
Literature Sales
P.O. Box 7641
Mt. Prospect, IL 60056-7641

or call 1-800-879-4683

Table of Contents

Tables and Figures

Description

The Intel 8242BB, preprogrammed with IBM keyboard and auxiliary device controller firmware, provides an off the shelf keyboard and auxiliary device controller solution for AT, PS/2, EISA, and PCI architectures.

Input to the keyboard and auxiliary device controller is through two connectors at the rear of the system unit. One connector is dedicated to the keyboard, the other is available for an auxiliary device. An auxiliary device can be any type of serial input device compatible with the Intel 8242BB interface. The device types include:

- Mouse
- Touchpad
- Trackball
- Keyboard

The Intel 8242BB receives the serial data, checks the parity, and presents the data to the system as a byte of data at data port hex 0060. The Intel 8242BB provides one RESEND attempt when a parity error is detected, before reporting an error in the status word. The Intel 8242BB can also translate keyboard scan codes from scan code set 2 to scan code set 1. Translate is not available for the auxiliary device interface.

The Intel 8242BB interrupts the system when data is available or waits for polling from the system microprocessor. Address hex 0064 is the command/status port. When the system reads port hex 0064, it receives status information from the Intel 8242BB. When the system writes to the port, the Intel 8242BB interprets the byte as a command.

Secondary circuit protection is provided on the system board for the +5 V dc line to the keyboard and auxiliary device.

Keyboard Password

Legal password characters are restricted to the 128 ASCII character set. The password can be up to seven bytes long but must be installed using the keyboard scan codes less than hex 80 (the Intel 8242BB does not compare keyboard scan codes greater than hex 7F). The carriage return scan code should be used as the last or eight character. Scan code set 1 is recommended for all password operations.

While the password is enabled, the Intel 8242BB compares the incoming keyboard scan code against the installed password, and it discards all data from the keyboard and auxiliary device that does not match the password. After a match occurs, the Intel 8242BB is restored to normal operation and data is again passed to the system microprocessor.

The Intel 8242BB provides three commands for keyboard password operation; it does not provide a command to verify the installed password.

- **A4h** Test Password Installed
- **A5h** Load Password
- **A6h** Enable Password

The Test Password Installed command **(A4h)** determines if a keyboard password is currently installed. The controlling program can use this command to determine if a keyboard password is loaded before enabling the password.

The Load Password command **(A5h)** allows the system microprocessor to set a keyboard password in the Intel 8242BB. The existing password is lost, and the new password becomes active. The keyboard password can be changed any time the Intel 8242BB is not in secure mode and must be installed in scan-code format.

The Enable Password command **(A6h)** places the Intel 8242BB in the secure mode. While in the secure mode, the Intel 8242BB intercepts the keyboard data stream and continuously compares it to the installed password pattern. The Intel 8242BB does not pass any information to the system microprocessor or accept any commands while the keyboard password is enabled. (To enable the address 20 signal while the password is enabled, use System Control Port A at address hex 0092 or other method provided by the systems chipset.)

Keyboard Password (con't)

The Intel 8242BB provides four internal RAM locations to support the keyboard password: addresses hex 13, 14, 16, and 17. See Controller Commands on page 8 for the commands on reading and writing to these locations.

Hex Address Description

13h Security on:
If this byte is non zero when the password is enabled, the Intel 8242BB loads this byte into the output buffer and generates a system interrupt. The recommended value is FFh so that the keyboard BIOS generates a beep instead of a character.

14h Security off:
If this byte is non zero when the password is matched, the Intel 8242BB loads this byte into the output buffer and generates a system interrupt. The recommended value is an FFh.

16h and 17h Make 1 and 2:
While the password is enabled, the Intel 8242BB first compares the incoming scan code against these two bytes. If the incoming scan code matches one of these two bytes, the scan code is discarded before it is compared to the password. This allows the Intel 8242BB to ignore certain keystrokes such as that for the right and left shift keys.

Controller Status Register

The following table shows the Controller Status register.

Bit	Function
7	Parity Error
6	General Time-Out
5	Auxiliary Device Output Buffer Full
4	Inhibit Switch
3	Command/Data
2	System Flag
1	Input Buffer Full
0	Output Buffer Full

Table 1. Controller Status Register, Read Port Hex 0064

Note: On the Intel 8242BB, commands C2h and C3h place data in bits 7 through 4 of the Controller Status register. See commands C2h and C3h on page 9 for more information.

Bit 7 When set to 0, this bit indicates that the last byte of data received from the keyboard had odd parity. When a parity error occurs, this bit is set to 1 and hex FF is placed in the output buffer (the keyboard and auxiliary device use odd parity). Before this error bit is set, the Intel 8242BB will have detected the first error, sent a RESEND command (FE) to the device, and then detected even parity in the retransmission.

Bit 6 When set to 1, this bit indicates that a transmission was started by the keyboard but did not finish within the receive time-out delay, or that a transmission was started by the Intel 8242BB but the byte transmitted was not clocked out within the specified time limit. When a receive time-out occurs, the Intel 8242BB places a hex FF in the output buffer. When a transmit time-out occurs, the Intel 8242BB places a hex FE in the output buffer. The Intel 8242BB also indicates a transmit time-out if a transmission was started and:

The byte was clocked out, but a response was not received within the time limit (only this bit is set to 1).

The byte was clocked out, but a response indicates a parity error (this bit and bit 7 are both set to 1).

Bit 5 This bit works in conjunction with bit 0. When this bit and bit 0 are set to 1, auxiliary device data is in the output buffer. When this bit is set to 0 and bit 0 is set to 1, keyboard or command controller response data is in the output buffer.

Bit 4 When set to 0, this bit indicates the password state is active and the keyboard is inhibited. When set to 1, this bit indicates the password state is inactive and the keyboard is not inhibited. (See Keyboard Password on page 2 for more information).

Bit 3 The keyboard controller input buffer can be addressed as either address hex 0060 or 0064. Address hex 0060 is defined as the data port, and address hex 0064 is defined as the command/status port. Writing to address hex 0064 sets this bit to 1. The Intel 8242BB uses this bit to determine if the byte in its input buffer should be interpreted as a command byte or a data byte.

Controller Status Register (con't)

Bit 2 This bit is set to 0 or 1 by writing to the system flag bit (bit 2) in the Controller Command byte. This bit is set to 0 after a power-on reset.

Bit 1 When set to 1, this bit indicates that data has been written into the buffer, but the Intel 8242BB has not read the data. When the Intel 8242BB reads the input buffer, this bit returns to 0, indicating that the input buffer is empty.

Bit 0 When set to 1, this bit indicates the Intel 8242BB has placed data into its output buffer but the system microprocessor has not yet read the data. When the system microprocessor reads the output buffer (address hex 0060), this bit returns to 0.

Input and Output Buffers

The output buffer is an 8-bit, read-only register at address hex 0060. When the output buffer is read, the Intel 8242BB sends information to the system microprocessor. The information can be keyboard scan codes, auxiliary device data, or data bytes from a controller command.

The input buffer is an 8-bit, write-only register at address hex 0060 or address hex 0064. When the input buffer is written to, the input-buffer-full bit (bit 1) in the Controller Status Byte is set to 1.

Data written to the input buffer through address hex 0064 is interpreted as a controller command. Data written to address hex 0060 is sent to the keyboard, unless the Intel 8242BB expects a data byte following a controller command. Bit 3 of the Controller Status register indicates whether the contents of the input buffer is a command or a data byte.

Note: Data should be written to the Intel 8242BB input buffer only if the input-buffer-full bit (bit 1) in the Controller Status register (address hex 0064) is 0.

Input Port (P1)

Bit	Function
7-2	User Definable
1	Auxiliary Data In
0	Keyboard Data In

Table 2. Input Port Definitions

Bit 7-2 These bits are user definable.

Bit 1 This bit reflects the state of the data line driven by the auxiliary device. For more information on the auxiliary device Data line, see Auxiliary Device and System timings on page 13.

Bit 0 This bit reflects the state of the Data line driven by the keyboard.

The Intel 8242BB does not internally use inputs from Port 1 other than bits 0 and 1 which are used for the Keyboard and Auxiliary Data lines. Bits 7 through 2 are reserved for system dependent use and are read by the system with the C0h Read Input Port command. For example, bit 7 is sometimes connected to KEYLOCK. The Intel 8242BB instead provides the same type of function through the Keyboard Password function and does not use the bit 7 input directly. However a system program may read these bits (7 through 2) with the C0h command or read the controller status byte after a C2h command and provide KEYLOCK or any other necessary support in software.

Output Port (P2)

Bit	Function
7	Keyboard Data Out
6	Keyboard Clock Out
5	IRQ12
4	IRQ1
3	Auxiliary Clock Out
2	Auxiliary Data Out
1	Gate Address Line A20
0	Reset Microprocessor

Table 3. Output Port Definitions

Bit 7 This bit reflects the state of the data line driven by the Intel 8242BB to the keyboard.

Bit 6 This bit reflects the state of the clock line driven by the Intel 8242BB to the keyboard.

Bit 5 When set to **1**, this bit indicates an interrupt has been generated by data from the auxiliary device in the output buffer. When the system reads the data from address hex 0060, this bit will be set to 0.

Output Port (P2) (con't)

Bit 4 When set to 1, this bit indicates an interrupt has been generated by data from the keyboard or a command in the output buffer. When the system reads the data from address hex 0060, this bit will be set to 0.

Bit 3 This bit reflects the state of the clock line driven by the Intel 8242BB to the auxiliary device.

Bit 2 This bit reflects the state of the data line driven by the Intel 8242BB to the auxiliary device.

Bit 1 When this bit and bit 1 in port hex 0092 are set to 0, the system address line A20 is disabled and set to 0. This bit is set to 0 at power-on. When this bit or bit 1 in port hex 0092 is set to 1, the system address line A20 is enabled. Only bit 1 can be altered with the D1h write output port command.

Bit 0 When set to 0, this bit resets the system microprocessor and holds it reset until the bit is set to 1.

Controller Commands

A command is a data byte written to the Intel 8242BB through address hex 0064. The commands are listed in order of their hex values; commands not listed are reserved.

20h-3Fh Read Controller RAM: This command causes the Intel 8242BB to return the data contained in the internal address specified by bits 5 through 0 of this command. Internal address hex 00 is assigned as the Controller Command byte. Command hex 20 requests a read operation of the Controller Command byte. The Intel 8242BB returns the data to port hex 0060.

Bit	Function
7	Reserved
6	Keyboard Translate
5	Disable Auxiliary Device
4	Disable Keyboard
3	Reserved
2	System Flag
1	Enable Auxiliary Interrupt
0	Enable Keyboard Interrupt

Table 4. Controller Command Byte

Bit 7 This bit is reserved and should not be altered.

Bit 6 When this bit is set to 1, the Intel 8242BB translates the incoming keyboard scan codes from scan code set 2 to scan set 1. When this bit is set to 0, the Intel 8242BB passes the incoming scan codes without translation. Following power-on or a keyboard reset, the keyboard transmits using scan code set 2. For keyboard operations that are compatible with IBM Personal Computers, the Intel 8242BB is placed in the translate mode.
Note: For the Intel 8242BB, this bit must be set to 0 while requesting the keyboard for its scan set. This prevents the Intel 8242BB from translating the keyboard response.

Bit 5 Setting this bit to 1 disables the auxiliary device interface by driving the clock line low. Data is not received while the interface is disabled.

Bit 4 Setting this bit to 1 disables the keyboard interface by driving the clock line low. Data is not received while the interface is disabled.

Bit 3 This bit is reserved and should not be altered.

Bit 2 The value written to this bit is placed in the system flag bit of the Controller Status register.

Bit 1 Setting this bit to 1 causes the Intel 8242BB to generate an interrupt (IRQ 12) when it places auxiliary device data into its output buffer.

Bit 0 Setting this bit to 1 causes the Intel 8242BB to generate an interrupt (IRQ 1) when it places keyboard or command controller response data into its output buffer.

60h-7Fh Write to Controller RAM: Bits 5 through 0 of the command specify the address. Internal address hex 00 is assigned as the Controller Command byte.

Command hex 0060 writes the Controller Command byte. The next byte of data written to address hex 0060 is placed in the Controller Command byte.

A4h Test Password Installed: This command checks for a password currently installed in the Intel 8242BB. The test result is placed in the output buffer (address hex 0060 and IRQ 01). Hex FA means the password is installed; hex F1 means it is not installed.

A5h Load Password: This command initiates the Password Load procedure. Following this command, the Intel 8242BB takes input from the data port until a null (0) is detected. The null terminates password entry. (See Keyboard Password on page 2.)

A6h Enable Password: This command enables the Intel 8242BB password feature. This command is valid only when a password pattern is currently loaded in the Intel 8242BB. (See Keyboard Password on page 2.)

A7h Disable Auxiliary Device Interface: This command sets bit 5 of the Controller Command byte to 1. This disables the auxiliary device interface by driving the clock line low. Data is not received while the interface is disabled.

A8h Enable Auxiliary Device Interface: This command sets bit 5 of the Controller Command byte to 0, releasing the auxiliary device interface.

A9h Auxiliary Device Interface Test: This command causes the Intel 8242BB to test the auxiliary device clock and data lines. The test result is placed in the output buffer (address hex 0060 and IRQ1) as shown in the following figure:

Test Result	Meaning
00	No error detected
01	The auxiliary device clock line is stuck low
02	The auxiliary device clock line is stuck high
03	The auxiliary device data line is stuck low
04	The auxiliary device data line is stuck high

Table 5. Command A9h Test Results

AAh Self-Test: This command causes the Intel 8242BB to perform a diagnostics test of the internal logic and memory. If there is an error the Intel 8242BB will go to its Self Test Wait without posting additional status. If the Self Test completes without error a 55h is placed in the output buffer.

When the Intel 8242BB is at its self test wait and detects input into the Input Buffer, a 1h will be written into bits 7 through 4 of the Controller Status register, The input buffer will then be read to check for an AAh Self Test command. If the input buffer contains data instead of the Self Test command the Intel 8242BB will return to the Self Test Wait leaving the 1h in bits 7 through 4 of the Controller Status Register.

If a valid AAh Self Test command is read, the Intel 8242BB will place a 2h in bits 7 through 4 of the Controller Status register as a check point and perform its first tests. The Self Test increments the check point value between tests. If an error is detected, the last checkpoint value is left in the Controller Status Register and the Intel 8242BB returns to the Self Test wait. The following check point halts would indicate a problem or error in the following areas of the Self Test routine:

1h - Valid AAh Self Test command check.

2h - Controller instruction processing tests.

3h - RAM data and addressing tests.

4h - ROM data checksum and addressing tests.

5h - Timer and Interrupt handling tests.

6h - Initialization routines and checks.

0h - Self Test complete and 55h placed in the Output buffer.

Bit 0 of the Controller Status register will be set to a 1 upon completion of the Self Test. The system should allow one second for the self test to complete before assuming an error occurred and checking the Controller Status Register bits 7 throng 4 for the error indication.

At the completion of the Self Test the Intel 8242BB sets its Controller Command Byte to 30h and enters normal service waiting for additional initialization commands. The controller command byte has both the keyboard and auxiliary devices disabled, the system flag off, and keyboard translate off. Normal operation would then be to enable the keyboard by writing a 65h to the controller command byte or a 47h to enable both the keyboard and auxiliary device interface.

ABh Keyboard Interface Test: This command causes the Intel 8242BB to test the keyboard clock and data lines. The test result is placed in the output buffer (address hex 0060 and IRQ1) as shown in the following figure:

Test Result	Meaning
00	No error detected
01	The keyboard clock line is stuck low
02	The keyboard clock line is stuck high
03	The keyboard data line is stuck low
04	The keyboard data line is stuck high

Table 6. Command ABh Test Results

ADh Disable Keyboard Interface: This command sets bit 4 of the Controller Command byte to 1. This disables the keyboard interface by driving the clock line low. Data is not received while the interface is disabled.

AEh Enable Keyboard Interface: This command clears bit 4 of the Controller Command byte to 0, releasing the keyboard interface.

C0h Read Input Port: This command causes the Intel 8242BB to read its input port and place the data in its output buffer.

C2h Poll Input Port High: This command causes the Intel 8242BB to read its input port bits 7 through 4 and place them in bits 7 through 4 of the Controller Status register.

C3h Poll Input Port Low: This command causes the Intel 8242BB to read its input port bits 3 through 0 and place them in bits 7 through 4 of the Controller Status register.

D0h Read Output Port: This command causes the Intel 8242BB to read its output port and place the data in its output buffer. This command should be used only if the output buffer is empty.

D1h Write Output Port: The next byte of data written to address hex 0060 is placed in the Intel 8242BB output port.
Note: Only Bit 1 of the data byte is used. The other bits of the output port are not altered by this command.

Controller Commands (con't)

D2h Write Keyboard Output Buffer: The next byte written to address hex 0060 input buffer is written to address hex 0060 output buffer as if initiated by the keyboard. An interrupt occurs if the interrupt is enabled in the Controller Command Byte.

D3h Write Auxiliary Device Output Buffer: The next byte written to address hex 0060 input buffer is written to address hex 0060 output buffer as if initiated by an auxiliary device. An interrupt occurs if the interrupt is enabled in the Controller Command Byte.

D4h Write to Auxiliary Device: The next byte written to address hex 0060 input buffer is transmitted to the auxiliary device.

E0h Read Test Inputs: This command causes the Intel 8242BB to read its test inputs and place the results in the output buffer. Test 0 (T0) is connected to the keyboard clock line, and test 1 (T1) is connected to the auxiliary device clock line. Data bit 0 represents T0, and data bit 1 represents T1.

F0h-FFh Pulse Output Port: This command pulses selected bits in the Intel 8242BB output port for approximately 6 microseconds. Bits 3 through 0 select the respective bits in the Intel 8242BB output port. For example, when bit 0 of this command is set to 0, bit 0 of the output port is pulsed and the system microprocessor is reset.

8242BB Programming Considerations

The following are some programming considerations for the Intel 8242BB keyboard and auxiliary device controller:

- When the Intel 8242BB is powered on, the Data lines are set high and the clock and interrupt lines are set low. The 8242BB then reads the input port (P1) and places bits 7 through 4 of the input port into bits 7 through 4 of the Controller Status Register. The 8242BB then waits at its Self Test Wait for the system to send the AAh Self Test command.
- Address hex 0064 (Controller Status register) can be read at any time.
- The auxiliary-device-output-buffer-full bit in the Controller Status register indicates that the data in address hex 0060 came from the auxiliary device. This bit is valid only when the output buffer full bit is set to 1
- Address hex 0060 and address hex 0064 should be written to only when the input-buffer-full bit and output-buffer-full bit in the Controller Status register are set to 0.
- To ensure that the buffer data is valid, disable the keyboard and auxiliary devices before initiating a command that causes the Intel 8242BB to generate output at port 60 (such as commands D1 and D3).

8242BB Programming Considerations (con't)

- Address hex 0060 (output buffer) should only be read when the output buffer full bit (bit 0) in the Controller Status Byte is 1. When the output buffer is read, the output-buffer-full bit will go to 0. After the output-buffer-full bit is 0 the Intel 8242BB may execute any pending command in the input buffer or receive data, causing the value in the output buffer to change.

- When polling the Intel 8242BB for the output-buffer-full condition, wait 7 microseconds from the buffer-full indication in the Controller Status register before reading the output buffer.

- External latches hold the level sensitive interrupt requests until the system microprocessor reads address hex 0060.

- When the Intel 8242BB sends a command or data byte to the keyboard or auxiliary device, the device is automatically enabled in the keyboard controller command byte. This allows the required acknowledgment (ACK) or Resend command to be received along with any requested data bytes.

Auxiliary Device and System Timings

Data transmissions to and from the auxiliary device connector consist of an 11-bit data stream sent serially over the data line. The following table shows the function of each bit.

Bit	Function
11	Stop bit (always 1)
10	Parity Bit (odd parity)
9	Data Bit 7 (most-significant)
8	Data Bit 6
7	Data Bit 5
6	Data Bit 4
5	Data Bit 3
4	Data Bit 2
3	Data Bit 1
2	Data Bit 0 (least-significant)
1	Start Bit (always 0)

Table 7. Bit Definitions of Auxiliary-Device Data Stream

The parity bit is either 1 or 0, and the 8 data bits, plus the parity bit, always have an odd number of 1's.

System Receiving Data

The following describes the typical sequence of events when the system is receiving data from the auxiliary device.

1. The auxiliary device checks the clock line. If the line is inactive, output from the device is not allowed.

2. The auxiliary device checks the data line. If the line is inactive, the Intel 8242BB receives data from the system.

3. The auxiliary device checks the clock line during the transmission at intervals not exceeding 100 microseconds. If the device finds the system holding the clock line inactive, the transmission is terminated. The system can terminate transmission anytime during the first 10 clock cycles.

4. A final check for terminated transmission is performed at least 5 microseconds after the 10th clock.

5. The system can hold the clock signal inactive to inhibit the next transmission.

6. The system can set the data line inactive if it has byte to transmit to the device. The data line is set inactive when the start bit (always 0) is placed on the data line.

7. The system raises the clock line to allow the next transmission.

The timing relationship is shown in the following figure.

Timing	Parameter	Min/Max
T1	Time from DATA transition to falling edge of CLK	5/25us
T2	Time from rising edge of CLK to DATA transition	5/T4-5us
T3	Duration of CLK inactive	30/50us
T4	Duration of CLK active	30/50us
T5	Time to auxiliary device inhibit after clock 11 to ensure the auxiliary device does not start another transmission	>0/50us

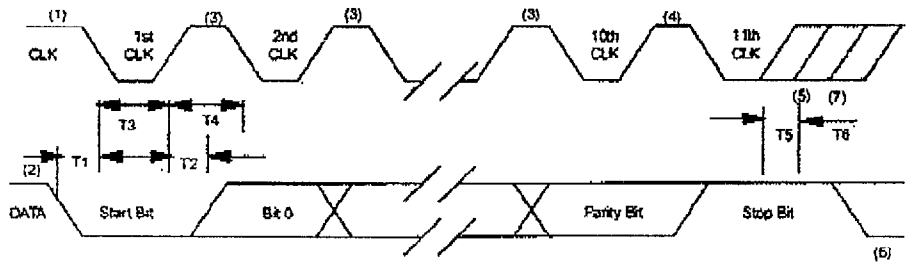

Table 8. Receiving Data Timings and Timing Diagram

System Sending Data

The following describes the typical sequence of events when the system is sending data to the auxiliary device.

1. The system checks for an auxiliary device transmission in process. If a transmission is in process and beyond the 10th clock, the system must receive the data.

2. The auxiliary device checks the clock line. If the line is inactive, an I/O operation is not allowed.

3. The auxiliary device checks the data line. If the line is inactive, the system has data to transmit. The data line is set inactive when the start bit (always 0) is placed on the Data¿ line.

4. The auxiliary device sets the clock line inactive. The system then places the first bit on the data line. Each time the auxiliary device sets the clock line inactive, the system places the next bit on the data line until all bits are transmitted.

5. The auxiliary device samples the data line for each bit while the clock line is active. Data must be stable within 1 microsecond after the rising edge of the clock line.

6. The auxiliary device checks for a positive-level stop bit after the 10th clock. If the data line is inactive, the auxiliary device continues to clock until the data line becomes active. Then it clocks the line-control bit and, at the next opportunity, sends a Resend command to the system.

7. The auxiliary device pulls the data line inactive, producing the line-control bit.

8. The system can pull the clock line inactive, inhibiting the auxiliary device.

The timing relationship is shown in the following table.

Timing	Parameter	Min/Max
T7	Duration of CLK inactive	30/50us
T8	Duration of CLK active	30/50us
T9	Time from inactive to active CLK transition, used to time when the auxiliary device samples DATA	5/25us

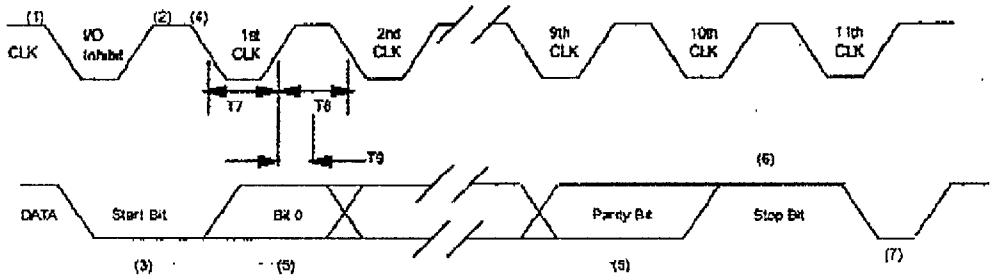

Table 9. Sending Data Timings and Timing Diagram

Signals

The keyboard and auxiliary device signals should be driven by open-collector drivers pulled to 5V DC through a pull-up resistor. The table following lists the characteristics of the signals.

Sink Current	20mA Maximum
High-Level Output	5.0V DC minus pull-up Minimum Voltage
Low-Level Output Voltage	0.5 V DC Maximum
High-Level Input Voltage	2.0 V DC Minimum
Low-Level Input Voltage	0.8 V DC Maximum

Table 10. Keyboard and Auxiliary Device Signal Characteristics

Connector

The keyboard and auxiliary device connectors use 6-pin miniature DIN connectors. The signals and voltages are the same for both connectors and are assigned as shown in the following table.

Pin	I/O	Signal Name
1	I/O	Data
2	NA	Reserved
3	NA	Ground
4	NA	+5 V dc
5	I/O	Clock
6	NA	Reserved

Table 11. Keyboard and Auxiliary Device Connector Information

Schematic

The following figure shows typical connections for the 8242BB is a PS/2 compatible environment. The 8242BB may also be used in an AT compatible (without a PS/2 style mouse connection) environment as well.

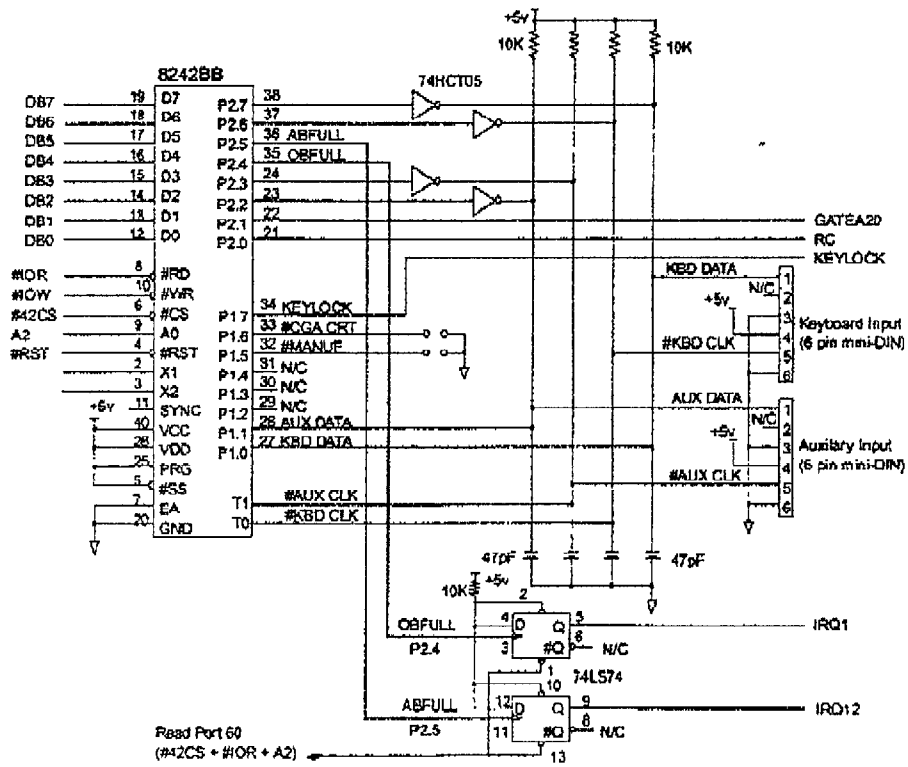

Figure 12. 8242BB Schematic Information (PS/2 Environment)