DATA SHEET

P8xCx66 family
Microcontrollers for PAL/SECAM TV with OSD and VST

Product specification
File under Integrated Circuits, IC20

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CONTENTS

1 FEATURES

1.1 P80C51 CPU core

- 80C51 8-bit CPU
- 64-kbyte Multiple Programming ROM (MTP ROM)
- Two 16-bit timer/event counters
- Crystal oscillator for system clock (up to 12 MHz)
- 12 source, 12 vector interrupt structure with two priority levels
- Enhanced architecture with:
  - Non-page orientated instructions
  - Direct addressing
  - Four 8-byte RAM register banks
  - Stack depth up to 128 bytes
  - Multiply, divide, subtract and compare instructions.

1.2 P8xCx66 family

- ROM/RAM: see Table 1
- Pulse Width Modulated (PWM) outputs:
  - One 14-bit PWM output for Voltage Synthesized Tuning (VST)
  - Eight 7-bit PWM outputs for analog controls.
- 3 Analog-to-Digital (ADC) inputs with 4-bit DAC and comparator
- LED driver port:
  - All I/O port lines with 10 mA LED drive capability (V_O <1.0 V)
  - Up to 5 LEDs can be driven at any one time.
- Serial I/O:
  - Multi-master I^{2}C-bus interface
  - Maximum I^{2}C-bus frequency 400 kHz.
- Watchdog timer
- Improved EMC measures and slope controlled I/Os
- OSD functions:
  - Programmable VSYNC and HSYNC active levels
  - Display RAM: 192 $\times$ 12 bits
  - Display character fonts: 128 (126 customer fonts plus 2 reserved codes)
  - 63 vertical starting positions controlled by software
  - 110 horizontal starting positions controlled by software
  - Character size: 4 different character sizes on a line-by-line basis
  - Character matrix: 12 $\times$ 18 with no spacing between characters
  - Foreground colours: 8 on a character-by-character basis
  - Background/shadowing modes: two primary modes - TV mode and Frame mode on a frame basis. Each primary mode has four sub-modes on a line basis:
    Sub-mode 1: Superimpose (no background)
    Sub-mode 2: North-West shadowing
    Sub-mode 3: Box background
    Sub-mode 4: Border shadowing
  - Background colours: 8 on a word-by-word basis, available in all four sub-modes
  - Display RAM starting address is programmable; fast switching between banks of display (RAM) characters is possible through software control
  - HSYNC driven PLL for OSD clock (4 to 12 MHz)
  - Character blinking ratio: 1 : 1
  - Character blinking frequency: programmable using f_{VSYNC} divisors of 32 and 64, on a character basis
  - Flexible display format using the Carriage Return code and the Space codes
  - Display RAM address post incremented each time new data is written into RAM
  - Vertical jitter cancelling circuit to avoid unstable VSYNC leading edge mismatch with HSYNC signal
  - OSD meshing.
- Power-on reset
- Packages: SDIL42 (PLCC68 for piggy-back only)
- Operating voltage: 4.5 to 5.5 V
- Operating temperature: –20 to +70 °C
- System clock frequency: 4 to 12 MHz
- OSD clock frequency: 4 to 12 MHz.

2 GENERAL DESCRIPTION

The P8xCx66 family consists of the following devices:

- P83C266
- P83C366
- P83C566
- P83C766
- P87C766.

The P8xCx66 family are 80C51-based microcontrollers designed for medium-high to high-end TV control applications. The P8xCx66 devices incorporate many unique features on-chip, giving them a competitive edge over similar devices from other manufacturers.

The Philips 80C51 CPU is object code compatible with the industry standard 80C51. All devices are manufactured in an advanced CMOS technology.

The P8xCx66 family also function as arithmetic processors having facilities for both binary and BCD arithmetic plus bit handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 46 two-byte and 16 three-byte. Multiply and divide instructions are implemented by hardware with a cycle time of 4 μs (f_{CLK} = 12 MHz).

The term P8xCx66 is used throughout this data sheet to refer to all family members; differences between devices are highlighted in the text.

Table 1 Memory structure for the different family members

MEMORY	P83C266	P83C366	P83C566	P83C766	P87C766
ROM	24 kbytes	32 kbytes	48 kbytes	64 kbytes	–
RAM	512 bytes	512 bytes	1 kbyte	1 kbyte	2 kbytes
EPROM	–	–	–	–	64 kbytes
Main memory	256 bytes	256 bytes	256 bytes	256 bytes	256 bytes
Auxiliary RAM	256 bytes	256 bytes	768 bytes	768 bytes	1792 bytes

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
P83C266BDR	SDIP42	plastic shrink dual in-line package; 42 leads (600 mil)	SOT270-1
P83C366BDR			
P83C366CBP			
P83C566BDR			
P83C766BDP			
P87C766BDR			
P87C766CBP			
P83C366BDA	PLCC68	plastic leaded chip carrier; 68 leads	SOT188-2
P83C566BDA			
P83C766BDA			
P87C766CBA			

4 BLOCK DIAGRAM

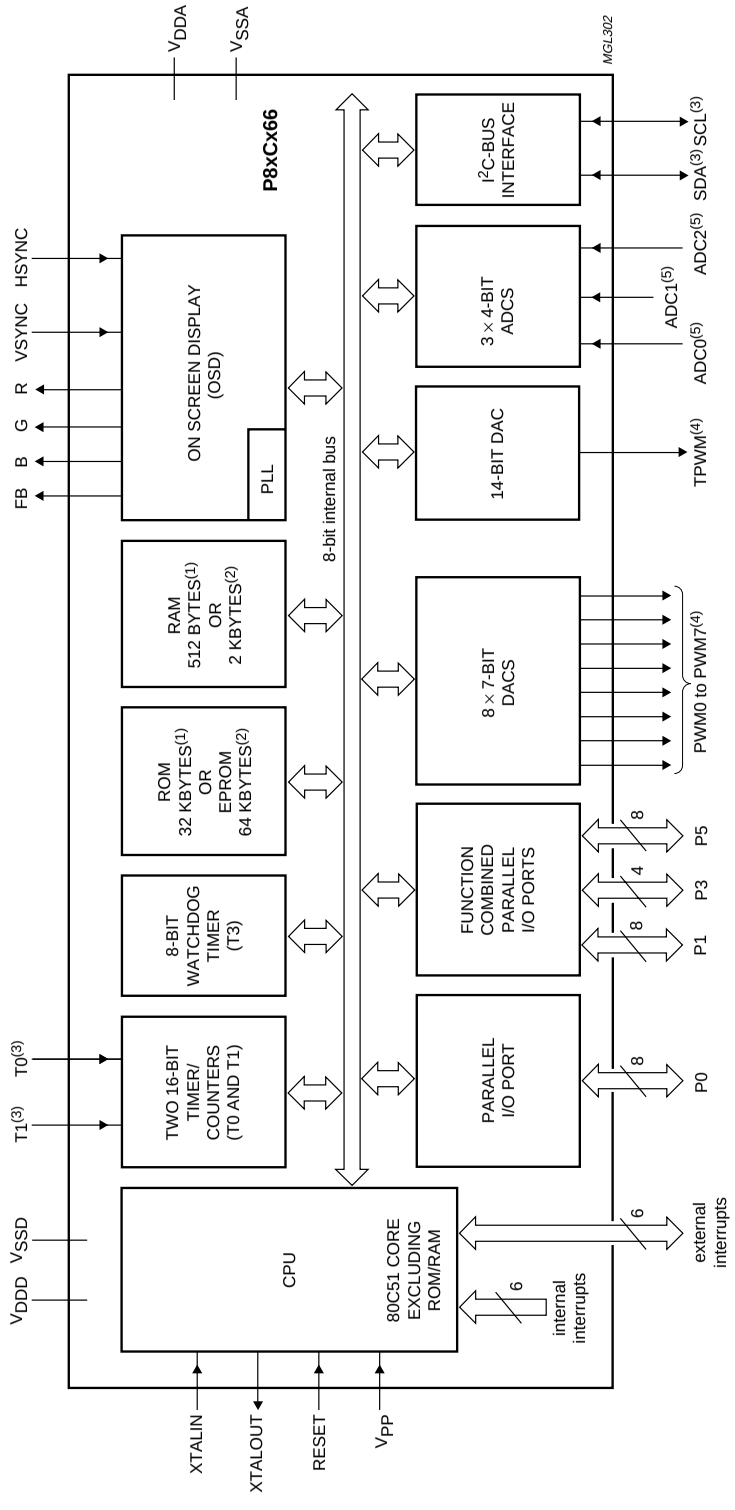


Fig.1 P83C366 and P87C766 block diagram.

(1) For the P83C366.
(2) For the P87C766.
(3) Alternative functions of Port 1.
(4) Alternative functions of Port 5, except PWM7 which is an alternative function of Port 3.
(5) Alternative functions of Port 3.

5 PINNING INFORMATION

5.1 Pinning

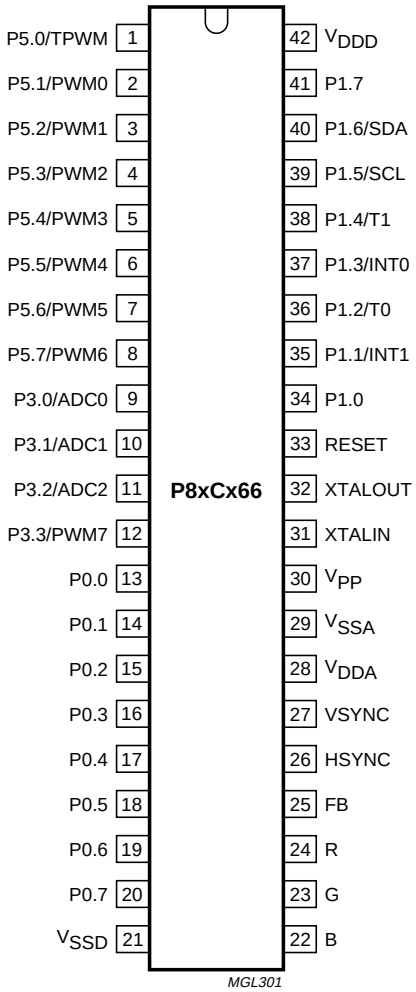


Fig.2 Pin configuration (SDIP42).

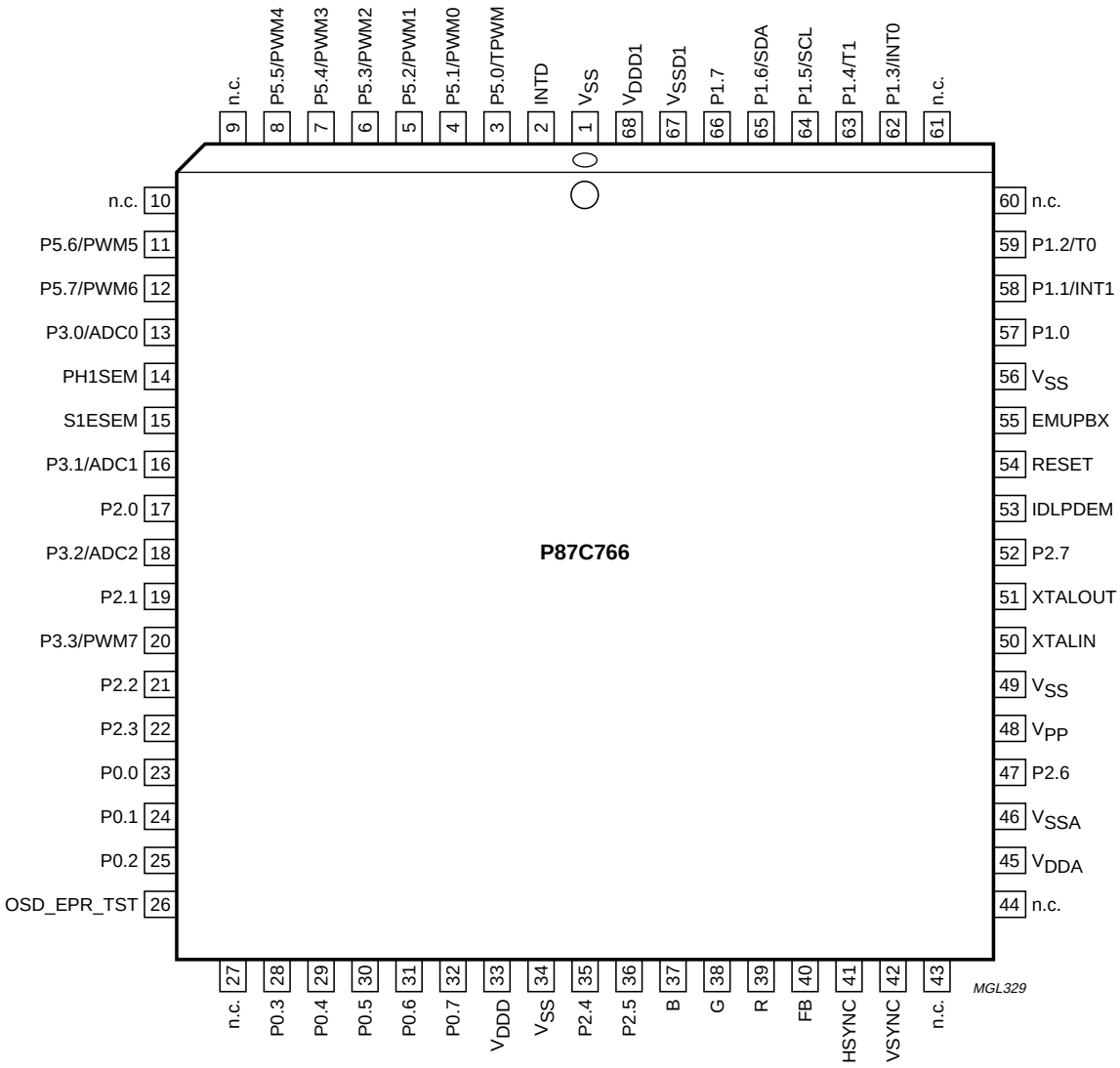


Fig.3 Pin configuration (PLCC68).

5.2 Pin description

Table 2 Pin description for SDIP42 and PLCC68 packages

SYMBOL	PIN		I/O	DESCRIPTION
	SDIP42	PLCC68		
P5.0/TPWM	1	3	I/O	**Port 5**: 8-bit open-drain, bidirectional port.(P5.0 to P5.7) with 8 alternative functions. **TWPM**: 14-bit PWM output. **PWM0 to PWM6**: 7-bit PWM outputs.
P5.1/PWM0	2	4		
P5.2/PWM1	3	5		
P5.3/PWM2	4	6		
P5.4/PWM3	5	7		
P5.5/PWM4	6	8		
P5.6/PWM5	7	11		
P5.7/PWM6	8	12		
P3.0/ADC0	9	13	I/O	**Port 3**: 4-bit open-drain, bidirectional port.(P3.0 to P3.3) with 4 alternative functions. **ADC0 to ADC2**: ADC inputs. **PWM7**: 7-bit PWM output.
P3.1/ADC1	10	16		
P3.2/ADC2	11	18		
P3.3/PWM7	12	20		
P0.0 to P0.7	13 to 20	23 to 25, 28 to 32	I/O	**Port 0**: 8-bit open-drain, bidirectional port (P0.0 to P0.7).
V_{SSD}	21		–	Ground line for digital circuits.
B	22	37	O	OSD blue colour output.
G	23	38	O	OSD green colour output.
R	24	39	O	OSD red colour output.
FB	25	40	O	OSD fast blanking output.
HSYNC	26	41	I	TV horizontal sync Schmitt trigger input (for OSD synchronization).
VSYNC	27	42	I	TV vertical sync Schmitt trigger input (for OSD synchronization).
V_{DDA}	28	45	–	5 V analog power supply.
V_{SSA}	29	46	–	Ground line for analog circuits.
V_{PP}	30	48	I	+12.75 V programming voltage supply (OTP) for EPROM only. 0 V in normal application. For the ROM version this pin is not connected.
XTALIN	31	50	I	Crystal input.
XTALOUT	32	51	O	Crystal output.

SYMBOL	PIN		I/O	DESCRIPTION
	SDIP42	PLCC68		
RESET	33	54	I	Reset input.
P1.0	34	57	I/O	**Port 1**: 8-bit open-drain, bidirectional port (P1.0 to P1.7) with 6 alternative functions. **INT1 and INT0**: external interrupts 1 and 0. **T1 and T0**: 16-bit timer/counter 1 and 0 inputs **SCL**: I^2C-bus clock line **SDA**: I^2C-bus data line
P1.1/INT1	35	58		
P1.2/T0	36	59		
P1.3/INT0	37	62		
P1.4/T1	38	63		
P1.5/SCL	39	64		
P1.6/SDA	40	65		
P1.7	41	66		
V_{DDD}	42	33	–	5 V digital power supply.
V_{SS}	–	1, 49, 56	–	Ground lines.
n.c.	–	9, 10, 27, 43, 44, 60, 61	–	not connected
INTD	–	2	I	These 3 signals are used for metalink+ emulation.
PH1SEM	–	14	I/O	
S1ESEM	–	15	I/O	
P2.0	–	17	I/O	**Port 2:** 8-bit open-drain, bidirectional port (P2.0 to P2.7).
P2.1	–	19		
P2.2	–	21		
P2.3	–	22		
P2.4	–	35		
P2.5	–	36		
P2.6	–	47		
P2.7	–	52		
OSD_EPR_TST	–	26	I/O	OSD EPROM test enable.
IDLPDEM	–	53	I/O	These 2 signals are used for metalink+ emulation.
EMUPBX	–	55	I/O	
V_{SSD1}	–	67	–	Ground line for digital circuits.
V_{DDD1}	–	68	–	5 V digital power supply.

6 MEMORY ORGANIZATION

The P8xCx66 family provides 24, 32, 48 or 64 kbytes of program memory (ROM/EPROM) plus 512, 1024 or 2048 bytes of data memory (RAM) on-chip (see Table 1). The device has separate address spaces for program and data memory (see Fig.4). These devices have no external memory access capability as the $\overline{RD}$ (read), $\overline{WR}$ (write), $\overline{EA}$ (External Access), $\overline{PSEN}$ (read strobe) and ALE (Address Latch Enable) signals are not bonded out.

6.1 Data memory

The P8xCx66 family contains 512, 1024 or 2048 bytes of internal RAM and 56 Special Function Registers (SFRs). Figure 4 shows the internal data memory space divided into the lower 128, the upper 128, AUX-RAM and the SFR space. The lower 128 bytes of internal RAM are organized as shown in Fig.5. The lowest 32 bytes are grouped into 4 banks of 8 registers. Program instructions refer to these registers as R0 to R7. Two bits in the Program Status Word (PSW) select which register bank is in use. The next 16 bytes above the register bank form a block of bit-addressable memory space. The 128 bits in this area can be directly addressed by the single-bit manipulation instructions. The remaining registers (30H to 7FH) are directly and indirectly byte addressable. The registers that reside at addresses above 7FH and up to FFH can only be accessed indirectly. These register addresses overlap the SFR addresses as described in Section 6.2.

6.2 Special Function Registers

The upper 128 bytes are the address locations of the SFRs when accessed directly. SFRs include the port latches, timers, 7-bit PWMs, 14-bit VST PWM, ADCs and OSD control registers. These registers can only be accessed by direct addressing. There are 128 bit-addressable locations in the SFR address space (SFRs with addresses divisible by eight). Their addresses are a multiple of 08H, from 80H to F8H. (i.e., 80H, 88H, 90H, 98H etc.). See Chapter 19 for SFR list.

6.3 AUX RAM

The 1792 byte (P87C766) or 768 byte (P83C766) AUX RAM, while physically located on-chip, logically occupies the first 1792/768 bytes of external data memory. As such, it is indirectly addressed in the same way as external data memory using MOVX instructions in combination with any of the registers R0, R1 or DPTR.

6.4 Addressing

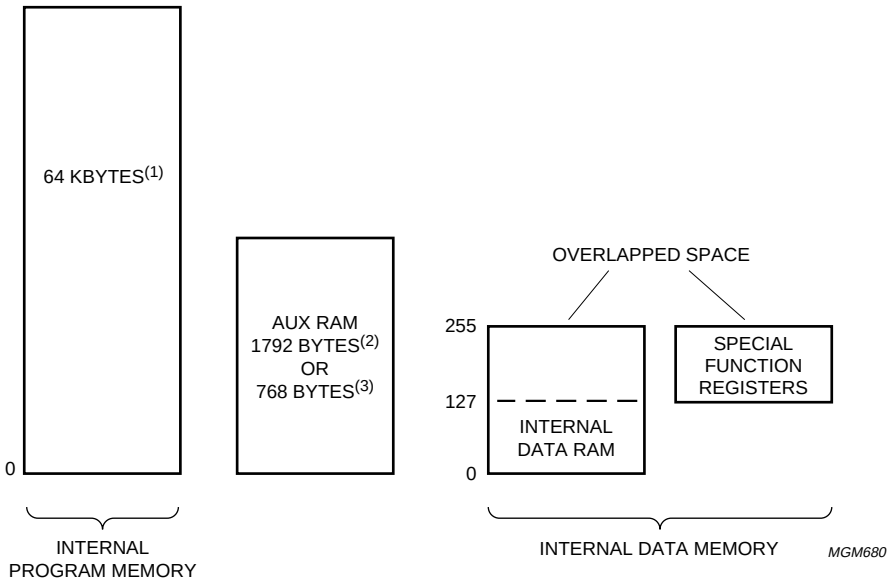
The P80C51 CPU has five methods for addressing source operands

- Register
- Direct
- Register-indirect
- Immediate
- Base-register-plus index-register-indirect.

The first three methods can be used for addressing destination operands. Most instructions have a ‘destination/source’ field that specifies the data type, addressing methods and operands involved.
For operations other than MOVs, the destination operand is also a source operand.

Access to memory addressing is as follows:

- Registers in one of the four register banks through register direct or indirect
- Internal RAM (128 bytes) through direct or register-indirect
- Special Function Registers through direct
- External data memory through register-indirect (for AUX RAM)
- Program memory look-up tables through base-register-plus index-register-indirect.



(1) For the P83C766 and the P87C766.
(2) For the P87C766.
(3) For the P83C566 and the P83C766.

Fig.4 Memory map.

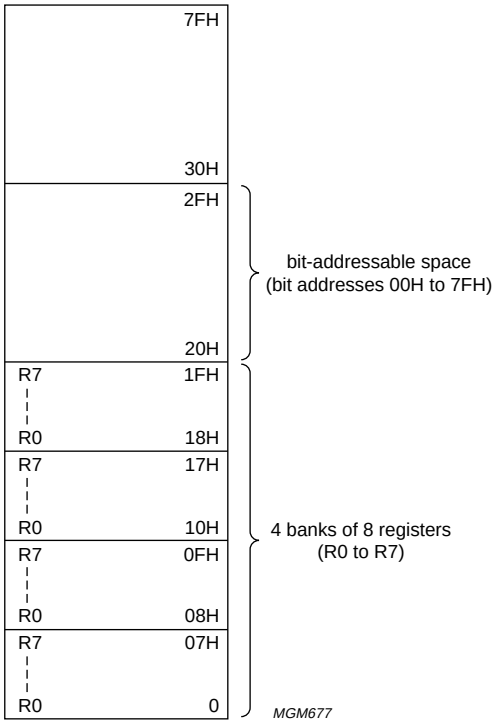


Fig.5 The lower 128 bytes of internal RAM.

7 I/O FACILITY

7.1 I/O ports

The SDIP42 package has 28 I/O lines treated as 28 individual addressable bits or as 3 parallel 8-bit addressable ports (Ports 0, 1 and 5) and one 4-bit port (Port 3).

When these 28 I/O lines are used as input ports, the corresponding bits in SFRs P0, P1, P3 and P5 should be set to a logic 1 to facilitate the external input signal.

Ports 1, 3 and 5 also perform the following alternative functions.

Port 1. Used for a number of special functions:

- Provides the external interrupt inputs (INT0 and INT1)
- Provides the 16-bit timer/counter inputs (T0 and T1)
- Provides the I^2C-bus data and clock signals (SDA and SCL)
- P1.0 and P1.7 can be used as external interrupt inputs.

Port 3. Only 4 lines available for alternative functions:

- 7-bit PWM output (PWM7)
- ADC inputs ADC0 to ADC2.

Port 5.

- Provides the 14-bit PWM output (TPWM)
- 7-bit PWMs outputs (PWM0 to PWM6).

To enable the alternative functions of Ports 1, 3 and 5, the port bit latch of its associated SFR must contain a logic 1.

Each port consists of a latch (SFRs P0, P1, P3 and P5), an output driver and an input buffer.

7.2 Port configurations

1. Open-drain quasi-bidirectional I/O with n-channel pull-down (see Fig.6). Use as an output requires the connection of an external pull-up resistor. Use as an input requires to write a logic 1 to the port latch before reading the port line.
2. Push-pull; gives drive capability of the output in both polarities, see Fig.7.

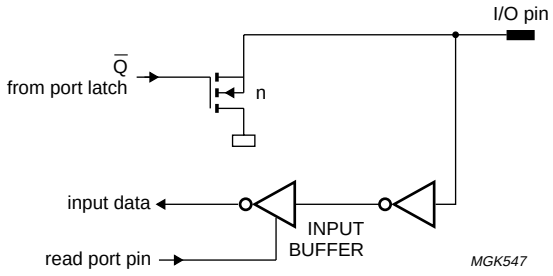


Fig.6 Open-drain port.

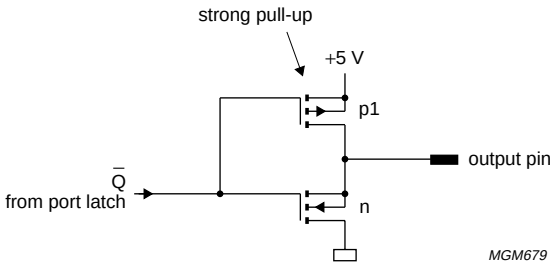


Fig.7 Push-pull port.

8 TIMERS AND EVENT COUNTERS

The P8xCx66 contains two 16-bit timers/counters: Timer 0 and Timer 1 and also an 8-bit Watchdog timer.

8.1 16-bit timer/counters (T0 and T1)

Timer 0 and Timer 1 perform the following functions:

- Measure time intervals and pulse durations
- Count events
- Generate interrupt requests.

Timer 0 and Timer 1 can be independently programmed to operate in one of four modes.

Mode 0 8-bit timer or counter with divide-by-32 prescaler.

Mode 1 16-bit time-interval or event counter.

Mode 2 8-bit time-interval or event counter with automatic reload upon overflow.

Mode 3 Timer 0 establishes TL0 and TL1 as two separate counters.

In the ‘timer’ function, the register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is $\frac{1}{12}f_{osc}$.

In the ‘counter’ function, the register is incremented in response to a HIGH-to-LOW transition. Since it takes 2 machine cycles (24 oscillator periods) to recognize a HIGH-to-LOW transition, the maximum count rate is $\frac{1}{24}f_{osc}$. To ensure that a given level is sampled, it should be held for at least one complete machine cycle.

8.2 Watchdog timer (T3)

In addition to the standard timers, a Watchdog timer is implemented on-chip. The Watchdog timer generates a hardware reset upon overflow. In this way a microcontroller system can recover from erroneous processor states caused by electrical noise, RFI or unexpected ROM code behaviour.

The Watchdog timer consists of an 8-bit timer with an 11-bit prescaler as shown in Fig.8. The prescaler input frequency is $\frac{1}{12}f_{osc}$. The 8-bit timer is incremented every ‘t’ seconds where ‘t’ is calculated as shown below:

$$t = 12 \times 2048 \times \frac{1}{f_{osc}}$$

The 8-bit timer is an up-counter so a value 00H gives the maximum timer interval (510 ms at 12 MHz, 1536 ms at 4 MHz), and a value of FFH gives the minimum timer interval (2 ms at 12 MHz, 6 ms at 4 MHz). When the 8-bit timer produces an overflow a short internal reset pulse is generated which will reset the P8xCx66.

The timer has no disable function. Consequently, all applications must reload the timer within the previously loaded timer interval otherwise a reset will occur. The timer is not stopped in the Idle mode. The interrupt routine for the Idle mode should also service the Watchdog timer.

The Watchdog timer is controlled by the WLE bit in the Power Control Register (see Section 9.6). The WLE bit must be set by the Watchdog timer service routine before the timer interval can be loaded into T3. A load of T3 automatically clears the WLE bit.

A system reset clears the Watchdog timer and the prescaler.

8.2.1 WATCHDOG TIMER REGISTER (WDT)

Table 3 Watchdog timer Register (SFR address FFH)

7	6	5	4	3	2	1	0
T37	T36	T35	T34	T33	T32	T31	T30

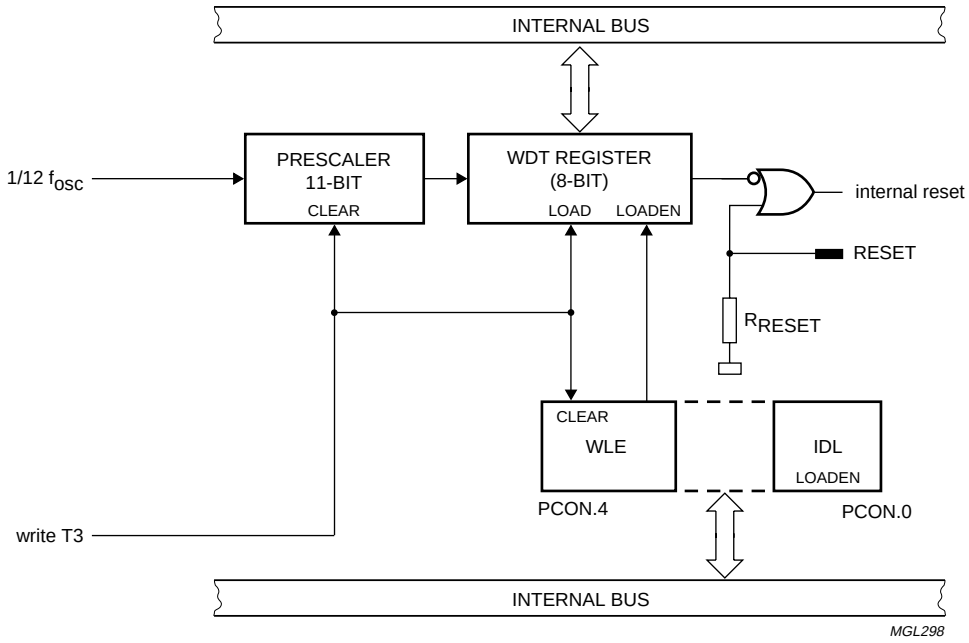


Fig.8 Block diagram of the Watchdog timer.

9 REDUCED POWER MODE

Only one reduced power mode is implemented; this is the Idle mode.

During Idle mode all blocks are inactive except Timer 0, Timer 1, INT0, INT1 and the Watchdog timer. These active functions may generate an interrupt (if their interrupts are enabled) and this will cause the device to leave the Idle mode.

The Idle mode is activated by software using the PCON register; this register is described in Section 9.6.

9.1 Idle mode

The instruction that sets PCON.0 is the last instruction executed before entering the Idle mode. Once in the Idle mode, the internal clock is gated away from the CPU and from all derivative functions (PWM/TPWM/ADC/I^2C-bus), except Timer 0, Timer 1 and interrupts INT0 and INT1. The Watchdog timer remains active. The CPU status is preserved along with the Stack Pointer, Program Counter, Program Status Word and the Accumulator. The RAM and all other registers maintain their data during Idle mode and the port pins retain the logic states held at Idle mode activation. The OSD clock is gated away from OSD circuit in Idle mode.

9.2 Recover from Idle mode

There are 3 methods used to terminate the Idle mode.

9.2.1 VIA AN INTERRUPT

Activation of INT0, INT1 or an interrupt from Timer 0 or Timer 1 will cause PCON to be cleared by hardware thus terminating the Idle mode. The interrupt is serviced and following the RETI instruction, the next instruction to be executed will be the one following the instruction that put the device in the Idle mode. All the other interrupts are disabled and will not generate an interrupt to wake-up the CPU.

9.2.2 VIA RESET

The second method of terminating the Idle mode is with an external hardware reset. Since the oscillator is still running, the hardware reset is required to be active for only two machine cycles to complete the reset operation. Reset redefines all SFRs, but does not effect the on-chip RAM.

9.2.3 VIA A WATCHDOG TIMER OVERFLOW

If the Watchdog timer is allowed to overflow or an erroneous processor state causes an overflow, a hardware reset will be generated, thus terminating the Idle mode.

9.3 General purpose flags (GF0 and GF1)

Flags GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or Idle mode. For example, the instruction that writes to PCON.0 to set the Idle mode can also set or clear one or both flags. When the Idle mode is terminated by an interrupt, the service routine can examine the status of the flag bits.

9.4 Output in Idle mode

- Ports will keep the value they had before entering the Idle mode
- The PWM0 to PWM7 outputs will be LOW
- The TPWM output will be LOW
- The I^2C-bus output is HIGH
- The pins R, G, B and FB will be the ‘inverse of Bp’, (defined by bit 2 of SFR OSCON).

9.5 Pending interrupts in Idle mode

If pending interrupts (I^2C-bus, VSYNC, P1.0 to P1.4 or P1.7) are present at the moment the CPU is switched to Idle mode, then these interrupts will wake-up the CPU. If this is not wanted then before entering the Idle mode all interrupts must be disabled, except those interrupts allowed to wake-up the CPU (INT0, INT1, Timer 0 and Timer1). New interrupts from I^2C-bus, VSYNC, P1.0 to P1.4 or P1.7 are disabled as soon as Idle mode is entered.

For example if a high priority interrupt is serviced just before the instruction which sets PCON.0 and a lower priority interrupt is generated during the interrupt service routine of the high priority interrupt, then the lower priority interrupt is pending. After the high priority interrupt is serviced (last instruction of routine is RETI) the main program will execute at least one more instruction to prevent a deadlock of the main program. In this case, it is the instruction which sets the PCON.0 bit (enter Idle mode). The pending lower level interrupt will, if enabled, immediately wake-up the CPU for an interrupt service, even though this interrupt is not INT0, INT1 or an interrupt from Timer 1 or Timer 0.

9.6 Power Control Register (PCON)

PCON is byte addressable only.

Table 4 Power Control Register (SFR address 87H)

7	6	5	4	3	2	1	0
–	–	–	WLE	GF1	GF0	0	IDL

Table 5 Description of PCON bits

BIT	SYMBOL	DESCRIPTION
7	–	These 3 bits are reserved.
6	–	
5	–	
4	WLE	**Watchdog Load Enable.** If WLE = 1, the Watchdog timer can be loaded. If WLE = 0, the Watchdog timer cannot be loaded.
3	GF1	**General purpose flag 1.**
2	GF0	**General purpose flag 0.**
1	–	This bit is reserved and must be set to a logic 0.
0	IDL	**Idle mode select.** If IDL = 1, the Idle mode is selected. If IDL = 0, the Idle mode is inhibited, i.e. normal operation.

10 I²C-BUS SERIAL I/O

10.1 The I²C-bus

The serial port supports the two line I²C-bus. The I²C-bus consists of a serial data line (SDA) and a serial clock line (SCL). These lines can also function as I/O port lines P1.6 and P1.5 respectively. To utilize this facility pins P1.5/SCL and P1.6/SDA must be configured as alternative functions instead of port lines; see Section 10.8.

The system is unique because data transport, clock generation, address recognition and bus control arbitration are all controlled by hardware.

Full details of the I²C-bus are given in the document *"The I²C-bus and how to use it"*. This document may be ordered using the code 9398 393 40011.

10.2 Operation modes

The I²C-bus serial I/O has complete autonomy in byte handling and operates in four modes

- Master transmitter
- Master receiver
- Slave transmitter
- Slave receiver.

These functions are controlled by the S1CON register. S1STA is the status register whose contents may also be used as a vector to various service routines. S1DAT is the data shift register and S1ADR the slave address register. Slave address recognition is performed by hardware.

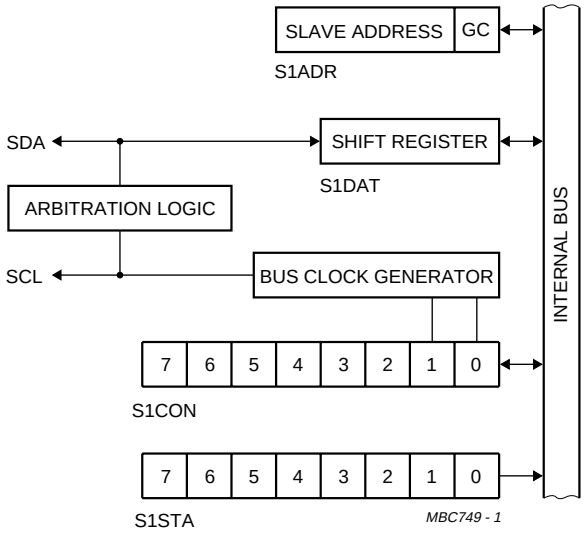


Fig.9 Block diagram of I²C-bus serial I/O.

10.3 Serial Control Register (S1CON)

Table 6 Serial Control Register (SFR address D8H)

7	6	5	4	3	2	1	0
CR2	ENS1	STA	STO	SI	AA	CR1	CR0

Table 7 Description of S1CON bits

BIT	SYMBOL	DESCRIPTION
6	ENSI	**Enable Serial I/O.** When ENSI = 0, the SIO is disabled and reset. The SDA and SCL outputs are in a high-impedance state; P1.5 and P1.6 function as open-drain ports. When ENSI = 1, the SIO is enabled. The P1.5 and P1.6 port latches must be set to logic 1.
5	STA	**START flag.** When the STA bit is set in Slave mode, the SIO hardware checks the status of the I^2C-bus and generates a START condition if the bus is free. If STA is set while the SIO is in Master mode, SIO transmits a repeated START condition.
4	STO	**STOP flag.** With this bit set while in Master mode a STOP condition is generated. When a STOP condition is detected on the bus, the SIO hardware clears the STO flag. In the Slave mode, the STO flag may also be set to recover from an error condition. In this case, no STOP condition is transmitted to the I^2C-bus interface. However, the SIO hardware behaves as if a STOP condition has been received and releases SDA and SCL. The SIO then switches to the ‘not addressed’ slave receiver mode. The STO flag is automatically cleared by hardware.
3	SI	**SIO interrupt flag.** When the SI flag is set, an acknowledge is returned after any one of the following conditions: • A START condition is generated in Master mode • Own slave address received during AA = 1 • General call address received while S1ADR.0 = 1 and AA = 1 • Data byte received or transmitted in Master mode (even if arbitration is lost) • Data byte received or transmitted as selected slave • STOP or START condition received as selected slave receiver or transmitter.
2	AA	**Assert Acknowledge.** When the AA flag is set, an acknowledge (LOW level to SDA) will be returned during the acknowledge clock pulse on the SCL line when: • Own slave address is received • General call address is received (S1ADR.0 = 1) • Data byte received while device is programmed as a Master receiver • Data byte received while device is a selected Slave receiver. With AA = 0, no acknowledge will be returned. Consequently, no interrupt is requested when the ‘own slave address’ or general call address is received.
7	CR2	**Clock Rate selection.** These three bits determine the serial clock frequency when SIO is in a Master mode; see Table 8. The maximum I^2C-bus frequency is 400 KHz.
1	CR1	
0	CR0	

Table 8 Selection of SCL frequency in Master mode

CR2	CR1	CR0	f_{osc} DIVISOR	BIT RATE (kHz) at f_{osc} = 12 MHz
0	0	0	60	200
0	0	1	1600	7.5
0	1	0	40	300
0	1	1	30	400
1	0	0	240	50
1	0	1	3200	3.75
1	1	0	160	75
1	1	1	120	100

10.4 Status Register (S1STA)

S1STA is an 8-bit read-only Special Function Register. The contents of S1STA may be used as a vector to a service routine. This optimizes response time of the software and consequently that of the I^2C-bus. The status codes for all possible modes of the I^2C-bus interface are given in Table 12. The abbreviations used in Table 12 are defined in Table 11.

Table 9 Status Register (SFR address D9H)

7	6	5	4	3	2	1	0
SC4	SC3	SC2	SC1	SC0	0	0	0

Table 10 Description of S1STA bits

BIT	SYMBOL	DESCRIPTION
7 to 3	SC4 to SC0	5-bit status code; see Table 12.
2 to 0	–	These 3 bits are held LOW.

Table 11 Abbreviations used in Table 12

SYMBOL	DESCRIPTION
SLA	7-bit slave address
R	read bit
W	write bit
ACK	acknowledgment (Acknowledge bit = 0)
$\overline{\text{ACK}}$	not acknowledge (Acknowledge bit = 1)
DATA	8-bit byte to or from the I^2C-bus
MST	master
SLV	slave
TRX	transmitter
REC	receiver

Table 12 Status codes

S1STA VALUE	DESCRIPTION
MST/TRX mode	
08H	a START condition has been transmitted
10H	a repeated START condition has been transmitted
18H	SLA and W have been transmitted, ACK received
20H	SLA and W have been transmitted. $\overline{\text{ACK}}$ received
28H	DATA of S1DAT has been transmitted, ACK received
30H	DATA of S1DAT has been transmitted, $\overline{\text{ACK}}$ received
38H	arbitration lost in SLA, R/W or DATA
MST/REC mode	
38H	arbitration lost while returning $\overline{\text{ACK}}$
40H	SLA and R have been transmitted, ACK received
48H	SLA and R have been transmitted, $\overline{\text{ACK}}$ received
50H	DATA has been received, ACK returned
58H	DATA has been received, $\overline{\text{ACK}}$ returned
SLV/REC mode	
60H	own SLA and W have been received, ACK returned
68H	arbitration lost in SLA, R/W as MST; own SLA and W have been received, $\overline{\text{ACK}}$ returned
70H	general CALL has been received, ACK returned
78H	arbitration lost in SLA, R/W as MST; general CALL has been received
80H	previously addressed with own SLA; DATA byte received, ACK returned
88H	previously addressed with own SLA; DATA byte received, $\overline{\text{ACK}}$ returned
90H	previously addressed with general CALL; DATA byte has been received, ACK returned
98H	previously addressed with general CALL; DATA byte has been received, $\overline{\text{ACK}}$ returned
A0H	a STOP condition or repeated START condition has been received while still addressed as SLV/REC or SLV/TRX
SLV/TRX mode	
A8H	own SLA and R have been received. ACK returned
B0H	arbitration lost in SLA, R/W as MST. Own SLA and R have been received, ACK returned
B8H	DATA byte has been transmitted, ACK received
C0H	DATA byte has been transmitted, $\overline{\text{ACK}}$ received
C8H	last DATA byte has been transmitted (AA = logic 0) ACK received
Miscellaneous	
00H	bus error during MST mode or SLV mode, due to an erroneous START or STOP condition

10.5 Data Shift Register (S1DAT)

S1DAT contains the serial data to be transmitted or data that has just been received. Bit 7 is transmitted or received first.

Table 13 Data Shift Register (SFR address DAH)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

10.6 Slave Address Register (S1ADR)

This 8-bit register may be loaded with the 7-bit slave address to which the controller will respond when programmed as slave receiver/transmitter. The LSB bit (GC) is used to determine whether the general CALL address is recognized.

Table 14 Slave Address Register (SFR address DBH)

7	6	5	4	3	2	1	0
SLA6	SLA5	SLA4	SLA3	SLA2	SLA1	SLA0	GC

Table 15 Description of S1ADR bits

BIT	SYMBOL	DESCRIPTION
7 to 1	SLA6 to SLA0	Own slave address.
0	GC	When GC = 0, the general CALL address is not recognized. When GC = 1, the general CALL address is recognized.

10.7 Internal Status Register (S1IST)

S1IST is an 8-bit read-only Special Function Register and will exist in the design but is not mapped for the user.

Table 16 Internal Status Register (SFR address DCH)

7	6	5	4	3	2	1	0
MST	TRX	BB	FB	ARL	SEL	AD0	SHRA

10.8 I^2C-bus Control Register (I^2CCON)

Table 17 I^2C-bus Control Register (SFR address 86H)

7	6	5	4	3	2	1	0
–	–	–	–	–	I^2CE	–	–

Table 18 Description of I^2CCON bits

BIT	SYMBOL	DESCRIPTION
7 to 3	–	These 5 bits are not used.
2	I^2CE	**I^2C-bus enable.** This bit selects the functions of pins 39 and 40 for the SDIP42 package (or pins 64 and 65 for the PLCC68 package). When I^2CE = 1, the alternative functions SCL and SDA are selected. When I^2CE = 0, these pins act as port lines P1.5 and P1.6.
1 to 0	–	These bits are not used.

11 INTERRUPT SYSTEM

External events and the real-time driven on-chip peripherals require service by the CPU asynchronous to the execution of any particular section of code. To tie the asynchronous activities of these functions to normal program execution a multiple-source, two-priority-level, nested interrupt system is provided. The P8xCx66 acknowledges interrupt requests from twelve sources as shown in Table 20.

Each interrupt vectors to a separate location in program memory for its service routine. Each source can be individually enabled or disabled by using corresponding bits in the Interrupt Enable Registers (IEN0 and IEN1). The priority level is selected via the Interrupt Priority Registers (IP0 and IP1). All enabled sources can be globally disabled or enabled. The minimum width of the external interrupt signal is ≥6 XTAL clocks. The maximum width of the interrupt signal is the total length of all instructions in the interrupt service routine until the clear instruction of the IRQ bit. The external interrupts are INT0, INT1, P1.0, P1.1, P1.2, P1.3, P1.4 and P1.7.

11.1 External interrupts INT2 to INT7 and INT9

Port 1 lines also serve as additional interrupts INT2 to INT7 (P1.0, P1.1, P1.2, P1.3, P1.4 and P1.7). INT7 is used by the derivative functional blocks as follows:

X7 VSYNC interrupt 0063H

Using the IX1 register, each pin may be initialized to be either active HIGH or active LOW except INT7 which is fixed active HIGH because this interrupt is from another derivative function. IRQ1 is the Interrupt Request Flag Register. Each flag will be set on interrupt request but it must be cleared by software, i.e. via the interrupt software.

11.2 Interrupt priority

Each interrupt source can be set to either high or low priority. If both priorities are requested simultaneously, the controller will branch to the high priority vector.

A low priority interrupt can only be interrupted by a high priority interrupt. A high priority interrupt routine cannot be interrupted

11.3 Related registers

The following registers are used in conjunction with the interrupt system.

Table 19 Interrupt registers

REGISTER	ADDRESS
Interrupt Polarity Register (IX1)	E9H
Interrupt Request Flag Register (IRQ1)	C0H
Interrupt Enable Register 0 (IEN0)	A8H
Interrupt Enable Register 1 (IEN1); interrupts INT2 to INT9	E8H
Interrupt Priority Register 0 (IP0)	B8H
Interrupt Priority Register 1 (IP1); interrupts INT2 to INT9	F8H

Table 20 Interrupt request (priority within level)

INTERRUPT MNEMONIC	SOURCE	VECTOR ADDRESS
PX0 (highest)	external interrupt 0 (INT0)	0003H
S1	I^2C-bus	002BH
T0	Timer 0 overflow	000BH
PX2	P1.0 port line	0033H
PX6	P1.4 port line	005BH
PX1	external interrupt 1 (INT1)	0013H
PX3	P1.1 port line	003BH
PX7	VSYNC interrupt	0063H
T1	Timer 1 overflow	001BH
PX4	P1.2 port line	0043H
PX5	P1.3 port line	004BH
PX9 (lowest)	P1.7 port line	0073H

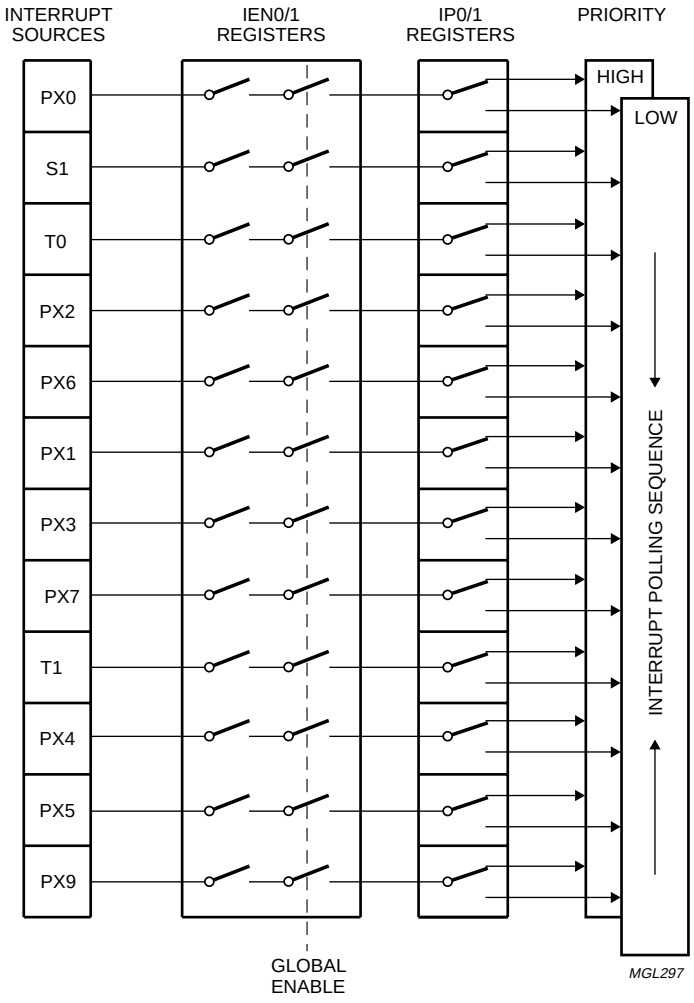


Fig.10 Interrupt system.

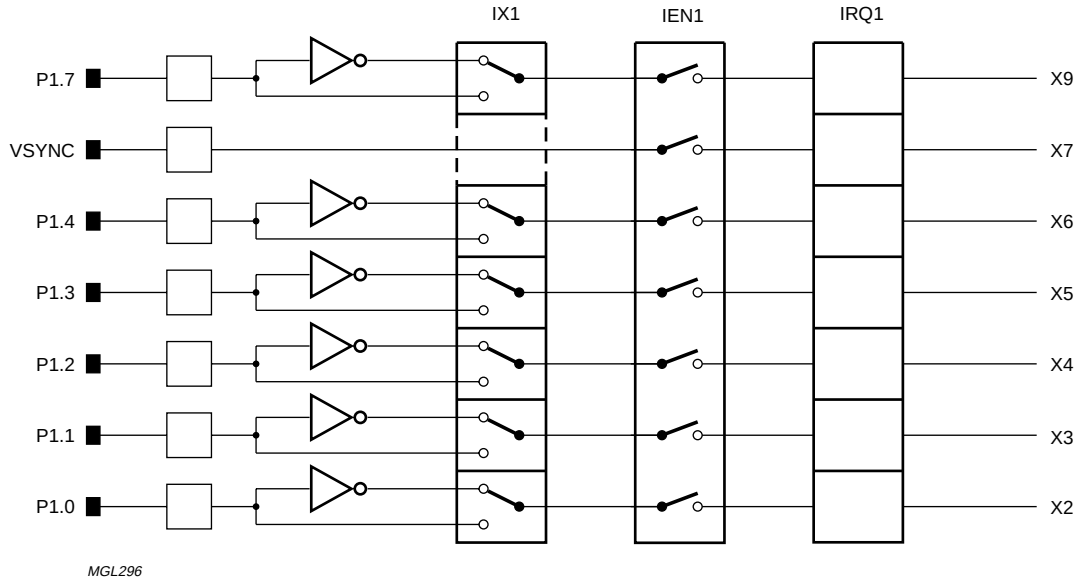


Fig.11 External and derivative interrupt configuration.

11.4 Interrupt Enable Register 0 (IEN0)

Table 21 Interrupt Enable Register (SFR address A8H)

7	6	5	4	3	2	1	0
EA	–	ES1	–	ET1	EX1	ET0	EX0

Table 22 Description of IEN0 bits

A logic 0 disables the interrupt; a logic 1 enables the interrupt.

BIT	SYMBOL	DESCRIPTION
7	EA	**General enable/disable control.** When EA = 0, no interrupt is enabled. When EA = 1, any individually enabled interrupt will be accepted.
6	–	not used
5	ES1	enable I^2C-bus SIO interrupt
4	–	not used
3	ET1	enable Timer 1 interrupt
2	EX1	enable external interrupt 1
1	ET0	enable Timer 0 interrupt
0	EX0	enable external interrupt 0

11.5 Interrupt Enable Register 1 (IEN1)

Table 23 Interrupt Enable Register (SFR address E8H)

7	6	5	4	3	2	1	0
EX9	–	EX7	EX6	EX5	EX4	EX3	EX2

Table 24 Description of IEN1 bits

Where EXx = 0, interrupt disabled. EXx = 1, interrupt enabled

BIT	SYMBOL	DESCRIPTION
7	EX9	enable external interrupt 9 (P1.7 port line)
6	–	not used
5	EX7	enable external interrupt 7 (VSYNC interrupt)
4	EX6	enable external interrupt 6 (P1.4 port line)
3	EX5	enable external interrupt 5 (P1.3 port line)
2	EX4	enable external interrupt 4 (P1.2 port line)
1	EX3	enable external interrupt 3 (P1.1 port line)
0	EX2	enable external interrupt 2 (P1.0 port line)

11.6 Interrupt Priority Register 0 (IP0)

Table 25 Interrupt Priority Register 0 (SFR address B8H)

7	6	5	4	3	2	1	0
–	–	PS1	–	PT1	PX1	PT0	PX0

Table 26 Description of IP0 bits

A logic 0 selects low priority; a logic 1 selects high priority.

BIT	SYMBOL	DESCRIPTION
7	–	These 2 bits are not used.
6	–	
5	PS1	I^2C-bus SIO interrupt priority level
4	–	This bit is not used.
3	PT1	Timer 1 interrupt priority level
2	PX1	external interrupt 1 priority level
1	PT0	Timer 0 interrupt priority level
0	PX0	external interrupt 0 priority level

11.7 Interrupt Priority Register 1 (IP1)

Table 27 Interrupt Priority Register 1 (SFR address F8H)

7	6	5	4	3	2	1	0
PX9	–	PX7	PX6	PX5	PX4	PX3	PX2

Table 28 Description of IP1 bits

Where PXx = 0 selects low priority; PXx = 1 selects high priority.

BIT	SYMBOL	DESCRIPTION
7	PX9	enable external interrupt 9 priority level (P1.7 port line)
6	–	not used
5	PX7	enable external interrupt 7 priority level (VSYNC interrupt)
4	PX6	enable external interrupt 6 priority level (P1.4 port line)
3	PX5	enable external interrupt 5 priority level (P1.3 port line)
2	PX4	enable external interrupt 4 priority level (P1.2 port line)
1	PX3	enable external interrupt 3 priority level (P1.1 port line)
0	PX2	enable external interrupt 2 priority level (P1.0 port line)

11.8 Interrupt Polarity Register (IX1)

Writing a logic 1 to bits IL9, IL6, IL5, IL4, IL3 and IL2 will set the polarity level of the corresponding external interrupt to be active HIGH. Writing a logic 0 to these bits will set the corresponding external interrupt to be active LOW.

External interrupts INT1 and INT0 however can be programmed to be edge sensitive. Writing a logic 1 to bits IL8 and IL7 will activate the external interrupts INT1 and INT0 on a rising edge (LOW-to-HIGH). Writing a logic 0 to bits IL8 and IL7 will activate the external interrupts INT1 and INT0 on a falling edge (HIGH-to-LOW). This feature is useful for pulse width measurement; see Section 11.8.1.

Table 29 Interrupt Polarity Register (SFR address E9H)

7	6	5	4	3	2	1	0
IL9	IL8	IL7	IL6	IL5	IL4	IL3	IL2

Table 30 Description of IX1 bits

BIT	SYMBOL	DESCRIPTION
7	IL9	external interrupt 9 polarity level (P1.7 port line)
6	IL8	external interrupt 1 polarity level (INT1) polarity level
5	IL7	external interrupt 0 polarity level (INT0) polarity level
4	IL6	external interrupt 6 polarity level (P1.4 port line)
3	IL5	external interrupt 5 polarity level (P1.3 port line)
2	IL4	external interrupt 4 polarity level (P1.2 port line)
1	IL3	external interrupt 3 polarity level (P1.1 port line)
0	IL2	external interrupt 2 polarity level (P1.0 port line)

11.8.1 Pulse width measurement example

To determine the LOW time of a signal on the external interrupt pin INT0 the following sequence should be followed.

1. External interrupt 0 must be programmed to edge sensitivity (SFR TCON, address 88H).
2. IL7 must be programmed as shown in Fig.12.
3. The value held in Timer 0 or Timer 1 represents the pulse width of the signal on the INT0 pin.

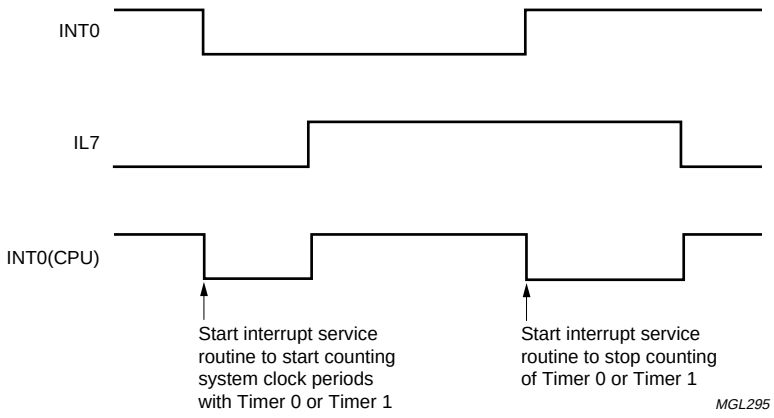


Fig.12 Pulse width measurement timing diagram.

11.9 Interrupt Request Flag Register (IRQ1)

Bits IQ9 and IQ6 to IQ2 will be set to a logic 1, if one of the two conditions specified below is met:

- If its associated port line is programmed to generate an interrupt when HIGH (selected using the Interrupt Polarity Register) and the state of that port line is HIGH
- If its associated port line is programmed to generate an interrupt when LOW (selected using the Interrupt Polarity Register) and the state of that port line is LOW.

IQ7 is set to a logic 1, if the interrupt condition is met within the corresponding derivative function. Therefore, all IRQ1 bits serve not only as pending interrupt request bits but also as interrupt status bits. This means that even if the external interrupts are disabled (using the Interrupt Enable Register 1) the IRQ1 bits can still be set to a logic 1 if the interrupt condition is met within the corresponding derivative function. For example, if the interrupt condition within VSYNC is met then:

- If IEN0.7 = X, IEN1.5 = 0 then IRQ1.5 = 1, no pending interrupt to CPU
- If IEN0.7 = 0, IEN1.5 = 1 then IRQ1.5 = 1, interrupt to CPU is pending
- If IEN0.7 = 1, IEN1.5 = 1 then IRQ1.5 = 1, interrupt will be serviced when either:
  - The CPU finishes current instruction, if not in the interrupt service routine
  - The current interrupt service routine is interrupted if the VSYNC has a higher interrupt priority
  - This VSYNC interrupt becomes pending, waiting until the current higher priority level interrupt is serviced.

Bits IQ9 and IQ7 to IQ2 can be reset by software.

Table 31 Interrupt Request Flag Register (SFR address C0H)

7	6	5	4	3	2	1	0
IQ9	–	IQ7	IQ6	IQ5	IQ4	IQ3	IQ2

Table 32 Description of IRQ1 bits

BIT	SYMBOL	DESCRIPTION
7	IQ9	external interrupt 9 request flag (P1.7 port line)
6	–	reserved
5	IQ7	external interrupt 7 request flag (VSYNC interrupt)
4	IQ6	external interrupt 6 request flag (P1.4 port line)
3	IQ5	external interrupt 5 request flag (P1.3 port line)
2	IQ4	external interrupt 4 request flag (P1.2 port line)
1	IQ3	external interrupt 3 request flag (P1.1 port line)
0	IQ2	external interrupt 2 request flag (P1.0 port line)

11.10 VSYNC interrupt and level status bit

The SFR VINT is read-only. Figure 13 shows the timing diagram of VSYNC interrupt.

Table 33 VSYNC Interrupt Register (SFR address C9H)

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	VLVL

Table 34 Description of VINT bits

BIT	SYMBOL	DESCRIPTION
7 to 1	–	These 7 bits are not used.
0	VLVL	**VSYNC input pin level.** The state of this bit indicates the level of the VSYNC input. As the input polarity of VSYNC is programmable two situations may be defined. If VSYNC is programmed active HIGH then: VLVL = 0, means VSYNC is at a LOW level, i.e. raster scan period VLVL = 1, means VSYNC is at HIGH level, i.e.vertical fly-back period. If VSYNC is programmed to active LOW then: VLVL = 0, means VSYNC is at LOW level, i.e. vertical fly-back period VLVL = 1, means VSYNC is at HIGH level, i.e. raster scan period

11.10.1 External interrupt request (IQ7)

A rising or falling edge (see Fig.13) of the active VSYNC signal generates a pending interrupt to the CPU and drives IQ7 HIGH (IQ7 resides in the SFR IRQ1). In the service routine, this bit should be cleared before return to main routine. As long as this bit is HIGH a pending interrupt is always there. Each time VSYNC is activated by a rising or falling edge, IQ7 is set HIGH. If the interrupt is not serviced before the next leading VSYNC edge, then IQ7 is written HIGH again and no error of overrun is indicated.

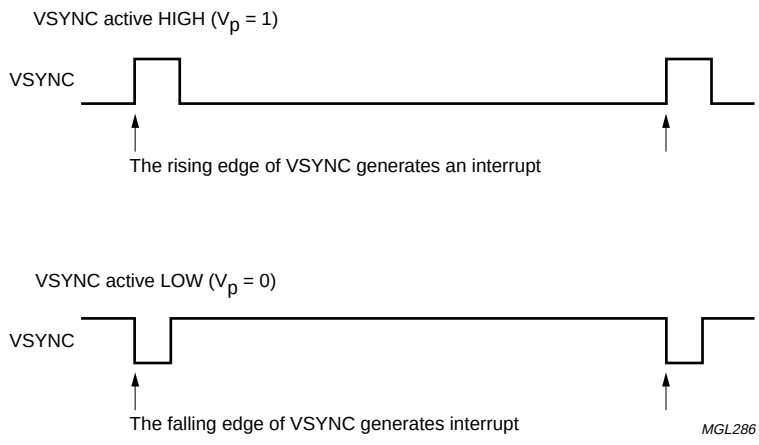


Fig.13 Timing diagram of VSYNC interrupt.

12 OSCILLATOR CIRCUITRY

The on-chip oscillator circuitry of the P8xCx66 is a single-stage inverting amplifier biased by an internal feedback resistor. For operation as a standard quartz oscillator, no external components are needed. When using external ceramic resonators different configurations are supported (see Fig.15). The crystal oscillator operating frequency range is 4 to 12 MHz.

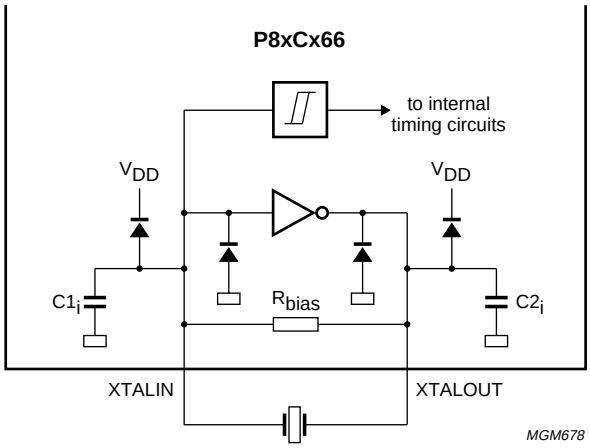


Fig.14 Standard oscillator.

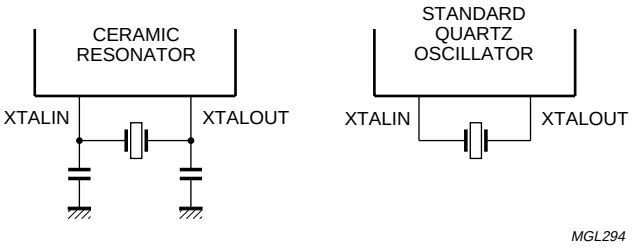


Fig.15 Alternative oscillator configurations.

13 RESET CIRCUITRY

To initialize the P8xCx66 a reset is performed by one of 3 methods:

- Via the RESET pin
- Via a Power-on reset
- Via the Watchdog timer.

A reset leaves the internal registers as shown in Table 35.

The reset input of the P8xCx66 is the RESET pin. A Schmitt trigger input qualifies the input for noise rejection. The output of the Schmitt trigger is sampled by the reset circuitry every machine cycle. A reset is accomplished by holding the RESET pin HIGH for at least two machine cycles (24 oscillator periods), while the oscillator is running. The CPU responds by generating an internal reset. Port pins adopt their reset state immediately after RESET goes HIGH.

The external reset is asynchronous to the internal clock. The RESET pin is sampled during state 5, phase 2 of every machine cycle. After a HIGH is detected at the RESET pin, an internal reset is repeated until RESET goes LOW.

The internal RAM is not affected by reset. When V_{DD} is switched on the RAM contents are indeterminate.

13.1 Reset operation for the OSD SFRs

There are 12 OSD Special Function Registers: OSAT, OSDT, OSAD, OSCON, OSCON2, OSORGV, OSORGH, OSDDEF, OSSTART, HDEL, OSFBD and OSPLL.

The OSD SFRs are only updated when VSYNC and HSYNC are present. If these signals are not present during a reset operation then the OSD SFRs will retain their values held after a Power-on reset.

In existing television systems HSYNC and VSYNC are often generated by a dedicated IC, consequently during start-up these signals may not be present. In this situation, it is mandatory to initialize all the OSD registers before entering the application.

13.2 Power-on reset

The P8xCx66 contains on-chip circuitry which switches the port to the customer defined logic level as soon as V_{DD} exceeds 3.9 V. As soon as the minimum supply voltage is reached, the oscillator will start-up. However, to ensure that the oscillator is stable before the controller starts, the reset is extended internally for 2048 oscillator periods. A hysteresis of approximately 500 mV at a typical power-on switching level of 3.9 V will ensure correct operation.

An automatic reset can be obtained at power-on by connecting the RESET pin to V_{DD} via a 10 µF capacitor. At power-on, the voltage on the RESET pin is equal to V_{DD} minus the capacitor voltage, and decreases from V_{DD} as the capacitor discharges through the internal resistor R_{RESET} to ground. The larger the capacitor, the more slowly V_{RESET} decreases. V_{RESET} must remain above the lower threshold of the Schmitt trigger input long enough to effect a complete reset. The time required is 2048 oscillator cycles plus 2 machine cycles.

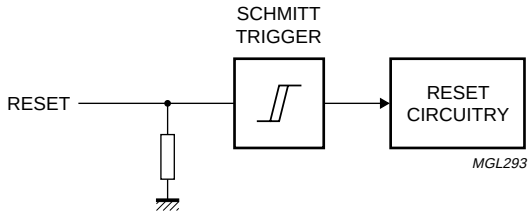


Fig.16 Reset configuration at RESET pin.

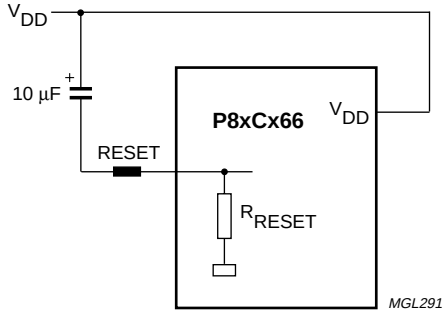


Fig.17 Recommended Power-on reset circuity.

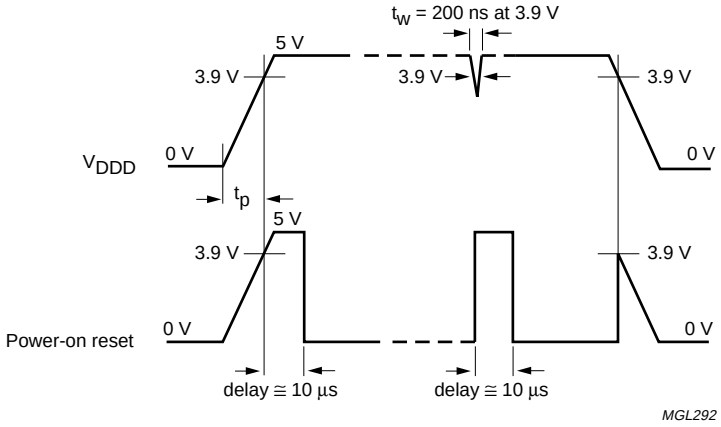


Fig.18 Power-on reset switching level.

Table 35 State of internal registers after a reset

REGISTER	REGISTER ADDRESS	CONTENTS(1)
ACC	E0H	0000 0000
B	F0H	0000 0000
DPL	82H	0000 0000
DPH	83H	0000 0000
IEN0	A8H	0000 0000
IEN1	E8H	0000 0000
IP0	B8H	XX00 0000
IP1	F8H	0000 0000
IX1	E9H	0000 0000
IRQ1	C0H	0000 0000
PSW	D0H	0000 0000
PCON	87H	XXX0 0000
P0	80H	1111 1111
P1	90H	1111 1111
P2	A0H	1111 1111
P3	B0H	XXXX 1111
P5	98H	1111 1111
OSDDEF	9CH	001X 0010
S1ADR	DBH	0000 0000
S1CON	D8H	X000 0000
S1DAT	DAH	0000 0000
S1STA	D9H	1111 1000
SP	81H	0000 0111
TCON	88H	0000 0000
TH0	8CH	0000 0000
TH1	8DH	0000 0000
TL0	8AH	0000 0000
TL1	8BH	0000 0000
TMOD	89H	0000 0000

REGISTER	REGISTER ADDRESS	CONTENTS(1)
I^2CCON	86H	XXXX X0XX
OSAT	99H	XXX1 1111
OSDT	9AH	1111 1111
OSAD	9BH	0000 0000
OSCON	C1H	0001 1100
OSORGV	C2H	XX11 1111
OSORGH	C3H	X111 1111
OSPLL	C4H	0000 0000
OSSTART	C5H	0000 0000
HDEL	C6H	XXXX 0000
OSFBD	C7H	XXXX 0000
SAD	C8H	0000 0000
S1IST	DCH	0000 0000
VINT	C9H	XXXX XXXX
SAD2	CAH	XXXX X000
OSCON2	CFH	XXX0 0010
TDACL	D2H	0000 0000
TDACH	D3H	0X00 0000
PWM0	E4H	0000 0000
PWM1	E5H	0000 0000
PWM2	E6H	0000 0000
PWM3	E7H	0000 0000
PWM4	ECH	0000 0000
PWM5	EDH	0000 0000
PWM6	EEH	0000 0000
PWM7	EFH	0000 0000
WDT	FFH	0000 0000

Note

1. Where X = undefined state.

14 PIN FUNCTION SELECTION

Ports 1, 3 and 5 are dual purpose ports and can be configured as general I/O port lines or selected as alternative functions. Selection of the pin function as an alternative function is achieved by setting the associated port latch bit to a logic 1 and then enabling the alternative function using its associated SFR.

14.1 Port 1 pin function selection

Port 1 is an 8-bit port which can be configured as eight bidirectional port lines (P1.0 to P1.7) or as two external interrupts (INT0 and INT1), two timer/counter inputs (T0 and T1) and the I^2C-bus lines (SDA and SCL). P1.0 and P1.7 have no alternative functions.

To configure these pins as alternative functions the corresponding bit in the Port 1 Latch (P1) should be programmed to a logic 1. The I^2C-bus lines are enabled by setting the I^2CE bit in the I^2C-bus Port Control Register, see Section 10.8. The remaining alternative functions are enabled using the associated SFR.

To use Port 1 pins as general I/O lines the alternative functions must be disabled.

14.2 Port 5 and P3.3 pin function selection

Port 5 pins can be selected as eight bidirectional port lines (P5.0 to P5.7) or as seven 7-bit PWM outputs (PWM0 to PWM6) and one 14-bit PWM output (TPWM).

Each 7-bit PWM output can be selected by setting the PWMnE bit in its associated PWMn register, to a logic 1 (see Section 15.1). When the PWMnE bit is a logic 0 the port line function is selected. The 14-bit PWM output (TPWM) is selected by setting the TPWME bit in SFR TDACH to a logic 1 (see Section 15.2).

P3.3 can also be selected as a bidirectional port line (P3.3) or as a 7-bit PWM output (PWM7). The 7-bit PWM output is enabled by setting the PWME7 bit in SFR PWM7 to a logic 1 (see Section 15.1).

14.3 Port 3 pin function selection

Port 3 is a 4-bit port which can be configured as four bidirectional port lines (P3.0 to P3.3) or as 3 ADC inputs (ADC0 to ADC2) and one 7-bit PWM output (PWM7). The selection of the PWM7 output is discussed in Section 14.2.

To select the alternative function of these port lines the corresponding bit in the Port 3 Latch (P3) should be programmed to a logic 1. The ADC inputs are then enabled using the SFR SAD2 as described in Section 14.3.1.

To use Port 3 pins as general I/O lines the alternative functions must be disabled.

14.3.1 ADC CONTROL REGISTER 2 (SAD2)

Table 36 ADC Control Register 2 (SFR address CAH)

7	6	5	4	3	2	1	0
–	–	–	–	–	ADCE2	ADCE1	ADCE0

Table 37 Description of SAD2 bits

BIT	SYMBOL	DESCRIPTION
7 to 3	–	These 5 bits are not used.
2	ADCE2	**ADC2 input select.** If ADC2 = 1, the ADC2 input is selected. If ADC2 = 0, the open-drain bidirectional port line P3.2 is selected.
1	ADCE1	**ADC1 input select.** If ADC1 = 1, the ADC1 input is selected. If ADC2 = 0, the open-drain bidirectional port line P3.1 is selected.
0	ADCE0	**ADC0 input select.** If ADC0 = 1, the ADC0 input is selected. If ADC0 = 0, the open-drain bidirectional port line P3.0 is selected.

15 ANALOG CONTROL

The P8xCx66 has nine Pulse Width Modulated (PWM) outputs for analog control purposes e.g., volume, balance, brightness, voltage synthesized tuning etc. Each PWM output generates a pulse pattern with a programmable duty cycle.

The nine PWM outputs are specified below:

- 8 PWM outputs with 7-bit resolution (PWM0 to PWM7)
- 1 PWM output with 14-bit resolution (TPWM).

The 7-bit PWM outputs are described in Section 15.1 and the 14-bit PWM output is described in Section 15.2.

15.1 7-bit PWM outputs (PWM0 to PWM7)

The block diagram of a typical 7-bit PWM circuit is shown in Fig.19.

PWM outputs PWM0 to PWM7 share the same pins as general I/O port lines P5.1 to P5.7 and P3.3 respectively. Selection of the pin function as either a PWM output or general I/O port line is achieved by setting the PWMnE bit in the associated PWM register (where n = 0 to 7).
The PWM registers are shown in Table 38.

The clock frequency of each PWM circuit is $\frac{1}{4}f_{osc}$ and therefore the repetition frequency of each 7-bit PWM output is $\frac{1}{512}f_{osc}$.

The polarity of each PWM output is fixed active HIGH. The HIGH period of each PWM output is dependent upon the contents of the PWM data latch and may be calculated as shown below:

$$t_{HIGH} = \frac{4 \times (PWMn)}{f_{osc}}$$

where (PWMn) is the decimal value held in the PWMn data latch

The PWM output analog value is determined by the ratio of the HIGH period and the repetition period. A DC voltage proportional to the PWM control setting is obtained by means of an external integration network (low-pass filter) connected to the PWM output pin.

The rising edge of each of the 8 PWM outputs is separated by one $\frac{1}{4}f_{osc}$ cycle, this is shown in Fig.21. PWM1 will always start at ‘2’, and PWM5 will start at ‘6’ independent of other PWMs value.

Figure 20 shows active HIGH PWM output patterns.

Table 38 7-bit PWM data registers

REGISTER	ADDRESS	7	6	5	4	3	2	1	0
PWM0	E4H	PWM0E	data6	data5	data4	data3	data2	data1	data0
PWM1	E5H	PWM1E	data6	data5	data4	data3	data2	data1	data0
PWM2	E6H	PWM2E	data6	data5	data4	data3	data2	data1	data0
PWM3	E7H	PWM3E	data6	data5	data4	data3	data2	data1	data0
PWM4	ECH	PWM4E	data6	data5	data4	data3	data2	data1	data0
PWM5	EDH	PWM5E	data6	data5	data4	data3	data2	data1	data0
PWM6	EEH	PWM6E	data6	data5	data4	data3	data2	data1	data0
PWM7	EFH	PWM7E	data6	data5	data4	data3	data2	data1	data0

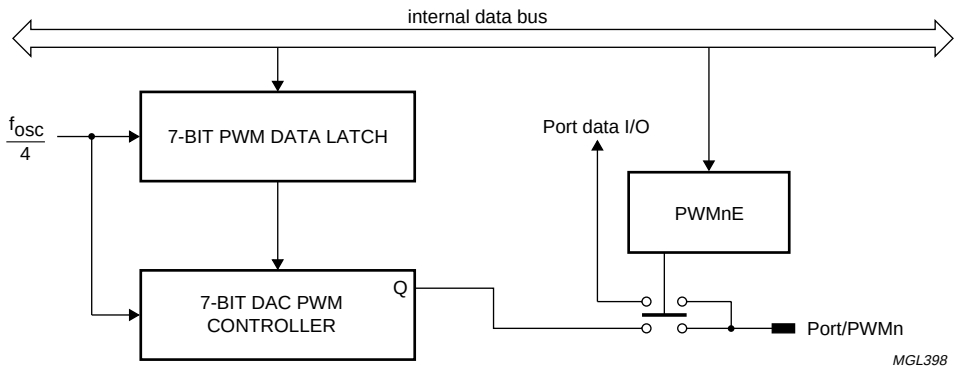


Fig.19 Block diagram of a typical 7-bit PWM circuit.

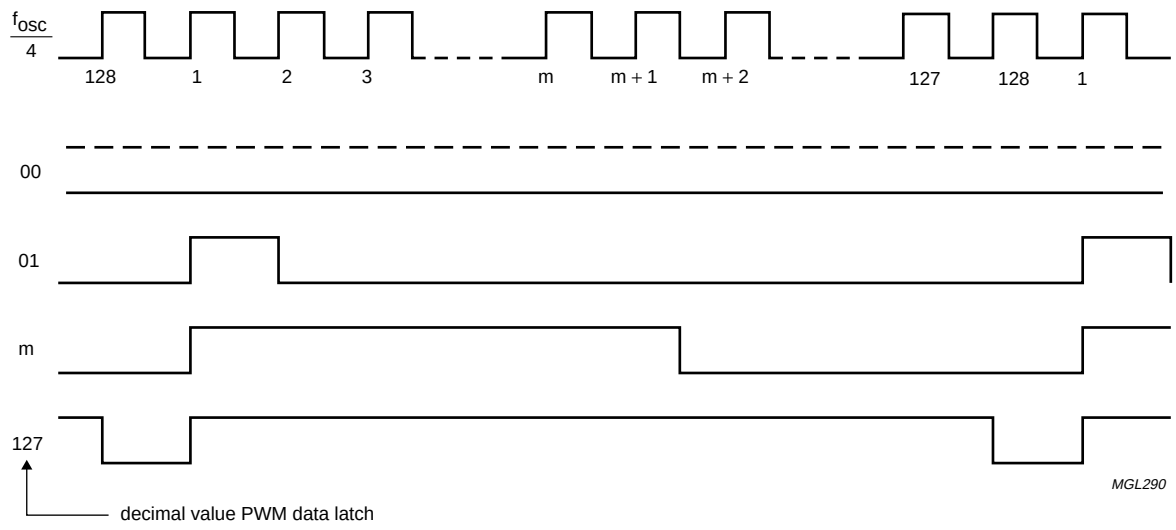
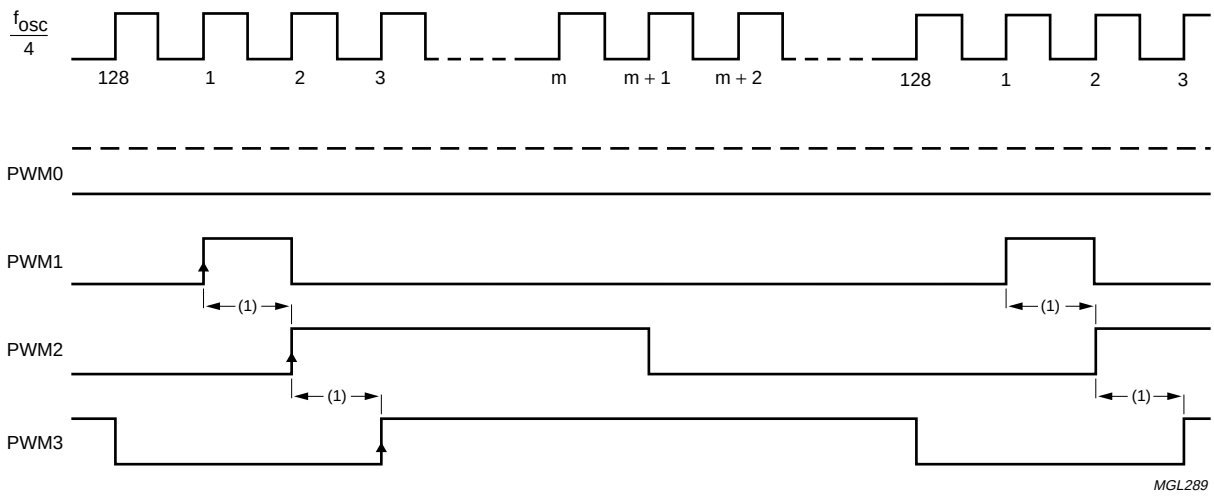


Fig.20 Example of 7-bit PWM output patterns.



(1) PWM outputs displaced by $\frac{1}{4}f_{OSC}$ cycle.

Fig.21 Separation of PWM output rising edges.

15.2 14-bit PWM output (TPWM)

The on-chip 14-bit DAC has one output with a resolution of 16384 levels for Voltage Synthesized Tuning (VST). The output is active HIGH, the HIGH period being determined by the values stored in the SFRs TDACH and TDACL. The 14-bit DAC output is connected to the TPWM pin.

TPWM shares the same pin as port line P5.0. Selection of the pin function as either a PWM output or as a port line is achieved using the TPWME bit in SFR TDACH, see Section 15.2.5.

The block diagram for the 14-bit PWM circuit is shown in Fig.22 and consists of:

- Two 7-bit SFRs: TDACH and TDACL
- One 14-bit register TDACREG
- One coarse control block for the generation of the coarse adjustment pulse
- One fine control block for the generation of the fine adjustment pulses
- One 14-bit counter running at f_{TDAC}
- One mixer block that combines the coarse adjustment pulse and fine tuning pulses; the resultant pulse pattern is fed to the TPWM output.

Data is loaded into the 14-bit data latch (TDACREG) from the two 7-bit data latches (TDACL and TDACH) at the beginning of the first T_{sub} period, after TDACH has been written to. To ensure that correct data is loaded into TDACREG, the data held in TDACL must be valid before the write operation to TDACH is started. In other words, TDACL must be written first before TDACH can be written to. Examples of valid and invalid loading sequences are shown in Fig.23.

Once TDACREG has been loaded it takes one T_{sub} period to generate the appropriate pulse patterns. To ensure correct operation of the DAC, two T_{sub} periods should be allowed before any further changes to the data latches are made.

The upper seven bits of TDACREG, identified as VSTH, are used for coarse adjustment and the lower seven bits, identified as VSTL, are used for fine adjustment.
The outputs OUT1 and OUT2 of the coarse and fine pulse controllers are ‘ORed’ in the mixer to give the TPWM output.

The 14-bit counter is continuously running and is clocked by f_{TDAC} which is $\frac{1}{4}f_{osc}$.

Figure 24 shows the output of the coarse pulse controller when VSTH = 001 1101; Fig.25 shows the output of the fine pulse controller when VSTL = 1111010, and Fig.26 shows a typical TPWM output after the ‘OR’ operation has been carried out by the mixer.

15.2.1 Repetition time of OUT1 and OUT2:

The repetition period of OUT1 (T_{sub}) may be calculated as shown in Equation (1).

$$T_{sub} = \frac{128}{f_{TDAC}} = 128 \times t_0 \quad (1)$$

Where $t_0 = \frac{1}{f_{TDAC}}$

The repetition period of OUT2 (T_{std}) may be calculated as shown in Equation (2).

$$T_{std} = \frac{128}{f_{TDAC}} \times 128 = 16384 \times t_0 \quad (2)$$

15.2.2 Coarse adjustment

An active HIGH pulse is generated in every subperiod (except the first one); the pulse duration being determined by the contents of VSTH. The coarse pulses are generated at the OUT1 output. The coarse pulse output is LOW at the start of each subperiod and will remain LOW until the time $[(128 - VSTH) \times t_0]$ has elapsed. The output will then go HIGH and remain HIGH until the start of the next subperiod. The coarse pulse duration is $(VSTH \times t_0)$. The trailing edge of each coarse pulse coincides with the end of each T_{sub} period. If VSTH = 0000000, then the coarse output is LOW for the complete period. If the contents of VSTH = 1111111, then the coarse output is LOW for the first t_0 period but will go HIGH for the remaining $127 \times t_0$ periods of Tsub.

15.2.3 Fine adjustment

Fine adjustment is achieved by generating an additional pulse in specific subperiods. These additional pulses appear at the OUT2 output. The pulse is added at the start of the selected subperiod and has a pulse width of t_0. The value held in VSTL determines the subperiod in which an additional pulse is generated and also determines the number of additional pulses that will be added during one T_{std} period. Table 39 shows the relationship between the value held in VSTL, the subperiod during which an additional pulse OUT2 is generated and the total number of additional OUT2 pulses generated.

For example, if the contents of VSTL = 000 0000, no additional pulses are generated; if the contents of VSTL = 111 1111, the number of additional pulses that are generated is 127. Therefore, up to 127 additional pulses can be added during a T_{std} period. Additional pulses must be distributed equally in one T_{std} period (pulse distribution procedure).

Figure 25 shows some examples of OUT2.

15.2.4 THE TPWM OUTPUT

If the contents of VSTH = 001 1101, and the contents of VSTL = 000 0010, then the TPWM output is as shown in Fig.26. The additional OUT2 pulses are generated in subperiods 32 and 96.

Two extreme cases are worthy of further analysis:

- VSTH = 000 0000, and VSTL = 000 0000. No coarse pulses will be generated and OUT1 is LOW for the whole T_{std} period. No fine pulses will be generated and consequently TPWM is LOW for the whole T_{std} period.
- VSTH = 111 1111 and VSTL = 111 1111. This value of VSTH results in OUT1 being LOW for the first t_0 period but will go HIGH for the remaining $127 \times t_0$ periods in the T_{sub} cycle. This value of VSTL will generate 127 additional fine pulses (in every T_{sub} cycle except in T_{sub0}). These additional fine pulses fill the gaps in the OUT1 output (except in T_{sub0}). Consequently, the TPWM output will be LOW for the first t_0 period (T_{sub0}) but will be HIGH for the remainder of the T_{std} period.

Table 39 Additional pulse distribution

VSTL CONTENTS	ADDITIONAL PULSE GENERATED IN SUBPERIOD T_{subn}	BINARY POSITION	TOTAL NUMBER OF ADDITIONAL OUT2 PULSES
000 0000	–	–	0
000 0001	64	100 0000	1
000 0010	32, 96	010 0000	2
000 0011	32, 64, 96	100 0000 010 0000	3
000 0100	16, 48, 80, 112	001 0000	4
000 0101	16, 48, 64, 80, 112	100 0000 001 0000	5
000 1000	8, 24, 40, 56, 72, 88, 104, 120	000 1000	8
001 0000	4, 12, 20, 28, 36, 44, 52, 60, ...116, 124	000 0100	16
010 0000	2, 6, 10, 14, 18, 22, 26, 30, ...122, 126	000 0010	32
100 0000	1, 3, 5, 7, 9, 11, 13, 15, ...125, 127	000 0001	64
111 1110	1, 2, 3, 4, ...62, 63, 65, 66, ...125, 126, 127	010 0000 001 0000 000 1000 000 0100 000 0010 000 0001	126
111 1111	1, 2, 3, 4, 5, 6, 7, ...125, 126, 127	100 0000 010 0000 001 0000 000 1000 000 0100 000 0010 000 0001	127

15.2.5 Special Function Register TDACH

Table 40 SFR TDACH (SFR address D3H)

7	6	5	4	3	2	1	0
TPWME	–	TD13	TD12	TD11	TD10	TD9	TD8

Table 41 Description of TDACH bits

BIT	SYMBOL	DESCRIPTION
7	TPWME	**TPWM enable.** When TPWME = 1, pin 1 is the TPWM output. When TPWME = 0, pin 1 is general I/O line P5.0.
6	–	This bit is not used.
5 to 0	TD13 to TD8	These 6 bits are loaded into TDACREG and form the 6 MSBs (TDACREG<13-8>).

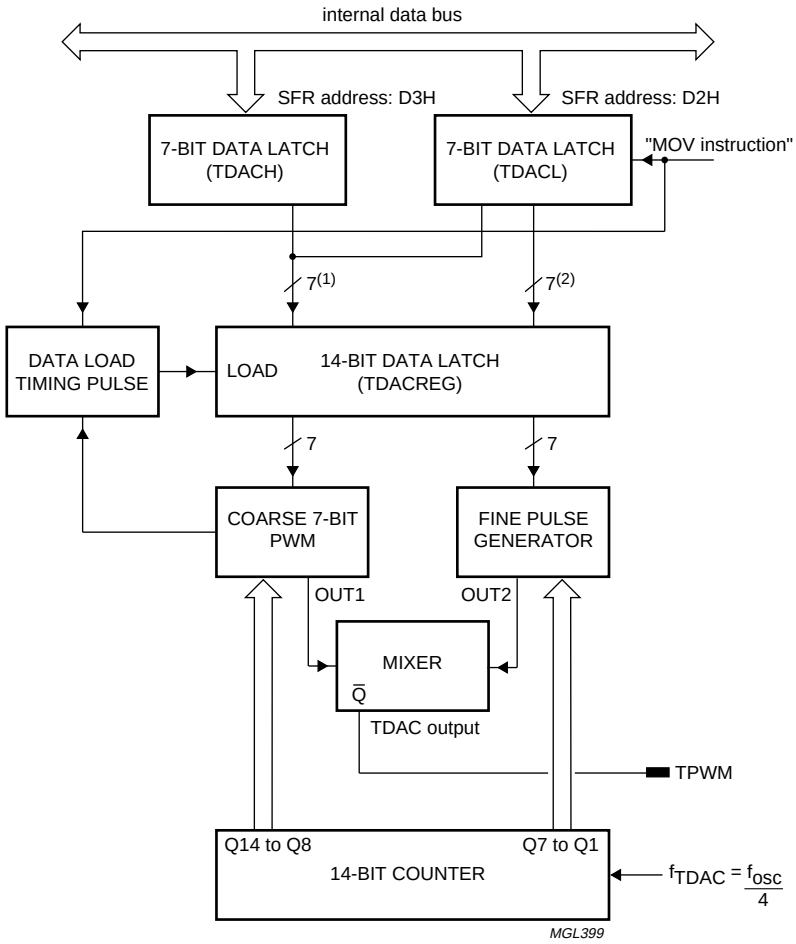
15.2.6 Special Function Register TDACL

Table 42 SFR TDACL (SFR address D2H)

7	6	5	4	3	2	1	0
TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0

Table 43 Description of TDACL bits

BIT	SYMBOL	DESCRIPTION
7	TD7	This bit is loaded into TDACREG and becomes bit 7 (TDACREG.7).
6 to 0	TD6 to TD0	These 7 bits are loaded into TDACREG and form the 7 LSBs (TDACREG<6-0>).



(1) These are the upper 7 bits of TDACREG and are called VSTH.
(2) These are the lower 7 bits of TDACREG and are called VSTL.

Fig.22 Block diagram of the 14-bit PWM circuit.

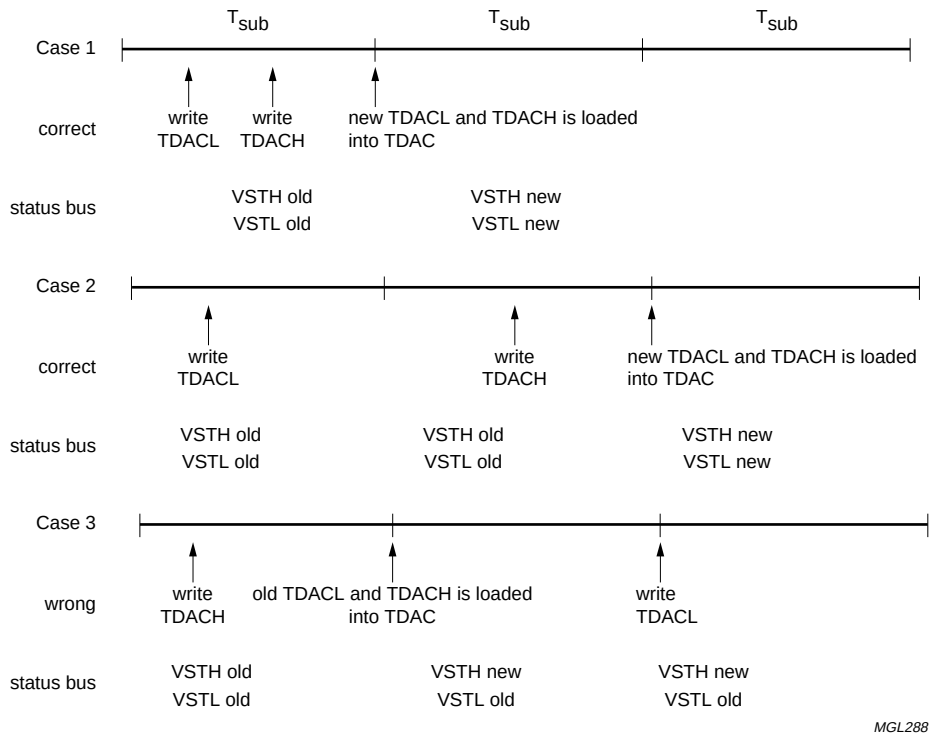


Fig.23 Loading VSTL and VSTH into VSTREG.

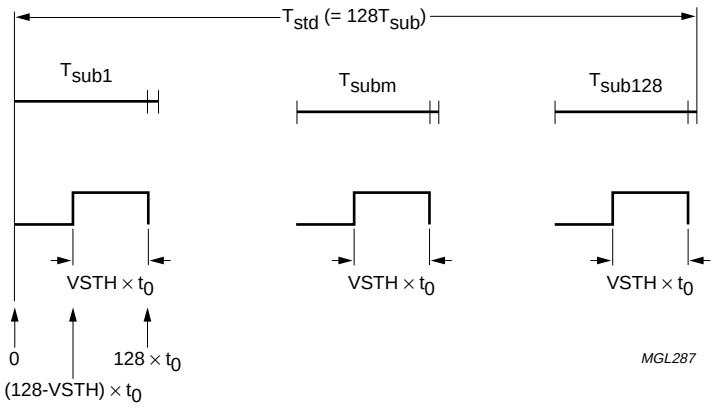


Fig.24 Coarse adjustment output (OUT1).

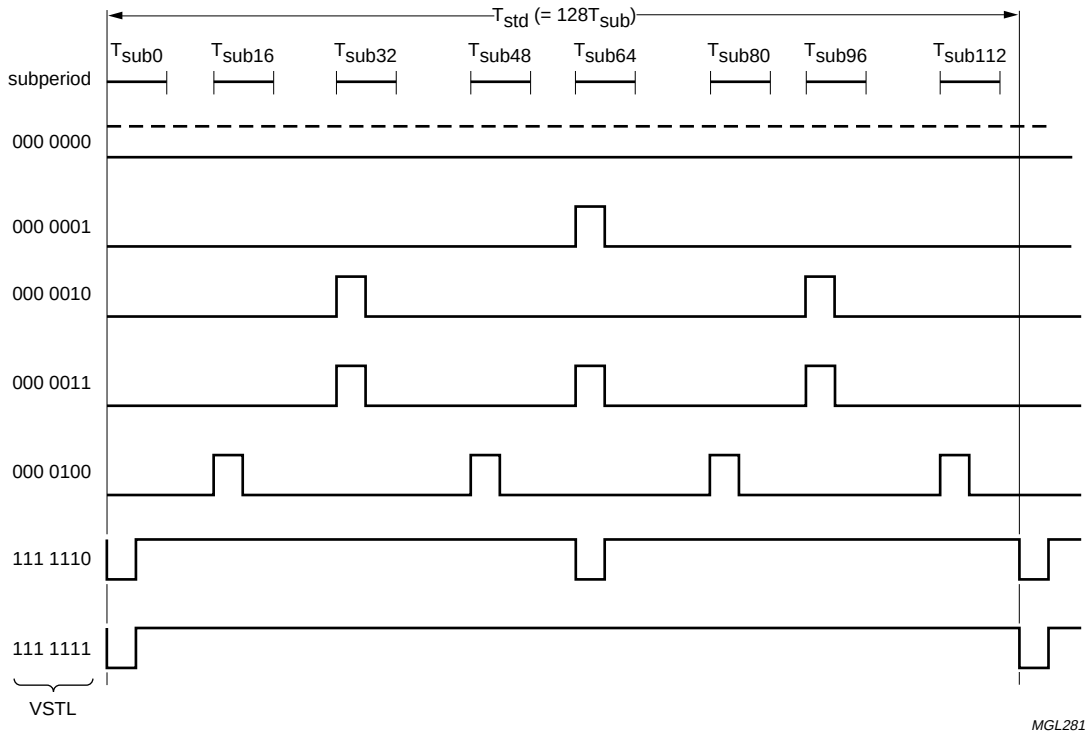


Fig.25 Fine adjustment output (OUT2).

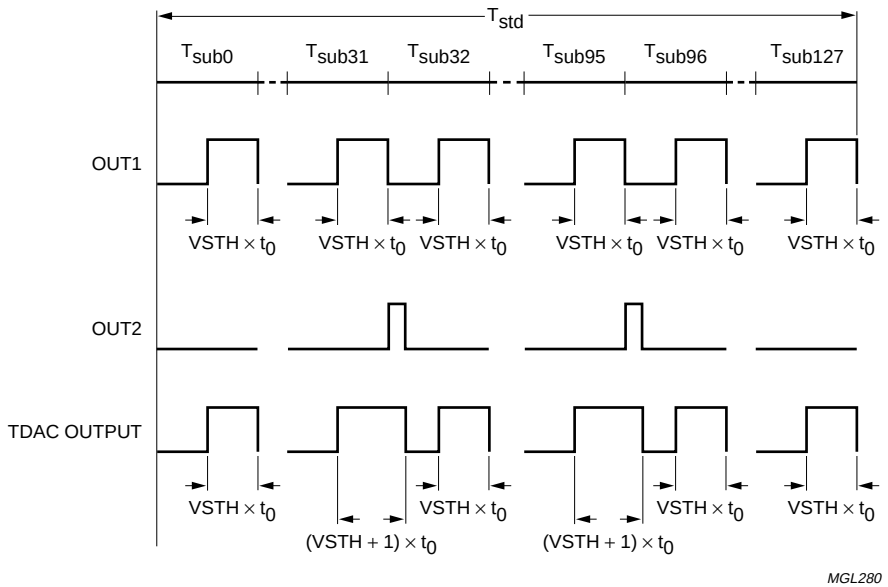


Fig.26 An example of TPWM output (VSTH = 001 1101 and VSTL = 000 0010).

16 ANALOG-TO-DIGITAL CONVERTERS (ADC)

The 3 channel ADC consists of a 4-bit Digital-to-Analog Converter (DAC), a comparator, an analog channel selector and control circuitry. The block diagram of the ADC circuit is shown in Fig.27.

One of these channels can be used to measure the level of the Automatic Frequency Control signal. This is achieved by comparing the ADC signal with the output of a 4 bit DAC using the comparator (accuracy $\pm\frac{1}{2}$ LSB).

The ADC inputs ADC0, ADC1 and ADC2 share the same pins as general I/O port lines P3.0, P3.1 and P3.2, respectively. Selection of the pin function as either an ADC input or a general I/O port line is achieved using bits ADCE0, ADCE1 and ADCE2 in SFR SAD2 (see Section 16.2).

The conversion time of the ADC is equal to 8 machine cycles (8 µs at 12 MHz). Some NOP instructions should be added in between the instruction which changes the reference voltage or the channel selection and the instruction which reads the VHI register bit. The ST bit must be set to a logic 1 at the same time as the reference voltage or channel selection change, otherwise the VHI state of the previous comparison will be read out.
The recommended procedure is as follows:

1. Write SFR SAD (X, CH<1:0>, ST = 1, SAD<3:0>)
2. Wait 8 machine cycles (for example 8 NOPs)
3. Read SFR SAD for VHI value.

ST is reset by hardware when it is set to a logic 1 by a written instruction. When ST is read, the value is always a logic 0.

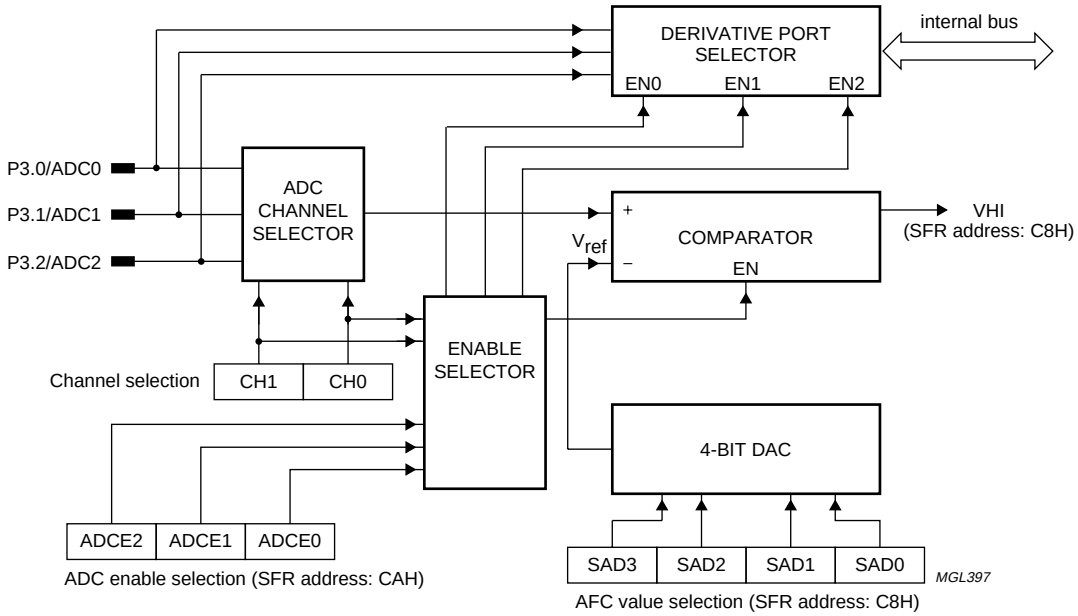


Fig.27 ADC block diagram.

16.1 ADC Control Register 1 (SAD)

Table 44 ADC Control Register 1 (SFR address C8H)

7	6	5	4	3	2	1	0
VHI	CH1	CH0	ST	SAD3	SAD2	SAD1	SAD0

Table 45 Description of SAD bits

BIT	SYMBOL	DESCRIPTION
7	VHI	**Compare result.** If VHI = 0, then the ADC input voltage is lower than the reference voltage. If VHI = 1, then the ADC input voltage is higher than the reference voltage.
6	CH1	**ADC input channel selection.** These 2 bits select the ADC channel, see Table 46.
5	CH0	
4	ST	**Start voltage comparison.** If ST = 0, voltage comparison is disabled. If ST = 1, a voltage comparison is started.
3	SAD3	**Reference voltage level selection.** These 4 bits are used to select the analog output voltage (V_{ref}) of the 4-bit DAC. V_{ref} is calculated as shown below. $V_{ref} = \frac{V_{DD}}{16} \times (\text{SAD value} + 1)$
2	SAD2	
1	SAD1	
0	SAD0	

Table 46 ADC input channel selection

CH1	CH0	CHANNEL SELECTED
0	0	Reserved.
0	1	Input channel ADC0 selected.
1	0	Input channel ADC1 selected.
1	1	Input channel ADC2 selected.

16.2 ADC Control Register 2 (SAD2)

Table 47 ADC Control Register 2 (SFR address CAH)

7	6	5	4	3	2	1	0
–	–	–	–	–	ADCE2	ADCE1	ADCE0

Table 48 Description of SAD2 bits

BIT	SYMBOL	DESCRIPTION
7 to 3	–	These 5 bits are not used.
2	ADCE2	**ADC2 input select.** If ADC2 = 1, then pin 11 is selected as the ADC2 input. If ADC2 = 0, then pin 11 is selected as the open-drain bidirectional port line P3.2.
1	ADCE1	**ADC1 input select.** If ADC1 = 1, then pin 10 is selected as the ADC1 input. If ADC2 = 0, then pin 10 is selected as the open-drain bidirectional port line P3.1.
0	ADCE0	**ADC0 input select.** If ADC0 = 1, then pin 9 is selected as the ADC0 input. If ADC0 = 0, then pin 9 is selected as the open-drain bidirectional port line P3.0.

17 ON-SCREEN DISPLAY (OSD)

17.1 Features

- Programmable active level polarity of VSYNC, HSYNC and digital RGB with polarity selection
- Display RAM: 192 × 12 bits
- Display character fonts: 128 (126 customer fonts plus 2 reserved codes)
- One programmable vertical starting position counter giving 63 different vertical starting positions
- One programmable horizontal starting position counter giving 110 different horizontal starting positions
- Character size: 4 character sizes on a line-by-line basis
- Character matrix: 12 × 18 with no spacing between characters
- Foreground colours: 8 on a character-by-character basis
- Background/shadowing modes: Two primary modes: TV mode and Frame mode on a frame basis. Each primary mode has four sub-modes on a character row basis:
  - Sub-mode 1: Superimpose (no background)
  - Sub-mode 2: North-West shadowing
  - Sub-mode 3: Box background
  - Sub-mode 4: Border shadowing.
- Background colours: 8 on a word-by-word basis. Available when background is either in North-West shadowing, Box background, Border shadowing and Frame shadowing sub-modes.
- Display RAM starting address is programmable. Fast switching between banks of display characters is possible through software control.
- HSYNC driven PLL (frequency determined by SFR OSPLL)
- Character blinking ratio: 1 : 1
- Character blinking frequency: programmable using f_{VSYNC} divisors of 32 and 64, on a character basis
- Display format: Flexible display format by using CR (carriage return) and SP1, SP2 (space) and split space code
- Display RAM address post increment each time new data is written
- Vertical jitter cancelling circuit to avoid unstable VSYNC leading edge mismatch with HSYNC signal
- OSD clock operating frequency: 4 to 12 MHz
- Meshing function.

17.2 Flexible display format

Figures 28 and 29 show typical examples of on-screen displays generated by the P8xCx66.

There are 128 different fonts available two of which, the Carriage Return (CR) code and the Space (SP) code, are reserved for special functions. The CR code performs the same function as the return key on a conventional keyboard, the display will start on the next line. The SP code enables the background colour of the space itself and that of the following characters to be changed.

There are 192 display RAM locations (00H to BFH) and these are considered as a linear addressed RAM. The first character fetched is from the display RAM address pointed to by the contents of the Special Function Register OSSTART (see Section 17.3.5).

The OSD starting position is programmable, this is described in detail in Section 17.2.1.

Two other registers are used to program the OSD: OSCON and OSCON2. These registers are described in Sections 17.3.2 and 17.3.6.

17.2.1 OSD STARTING POSITION

The horizontal and vertical starting position of the display is controlled by two counters: SFRs OSORGH and OSORGV.

OSORGH controls the horizontal starting position. This counter is incremented every OSD clock cycle after the falling edge of HSYNCP (after the polarity selection). HSYNCP is always active HIGH. OSORGH is described in Section 17.3.4.

OSORGV controls the vertical starting position. This counter is incremented every HSYNC cycle and is reset by the VSYNC signal. OSORGV is described in Section 17.3.3.

The OSD starting position reference points are shown in Fig.32.

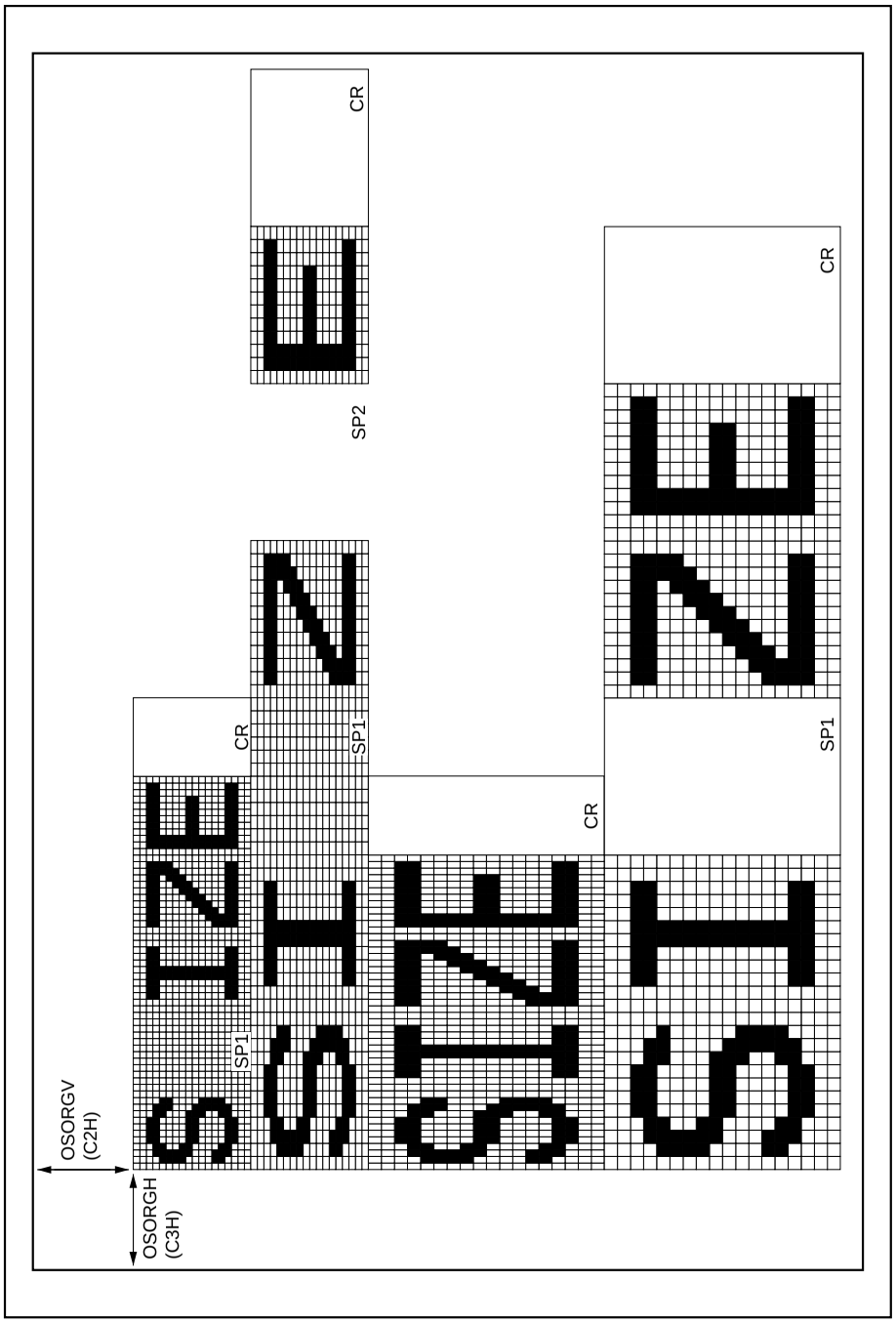


Fig.28 An example of flexible display format (Split space off).

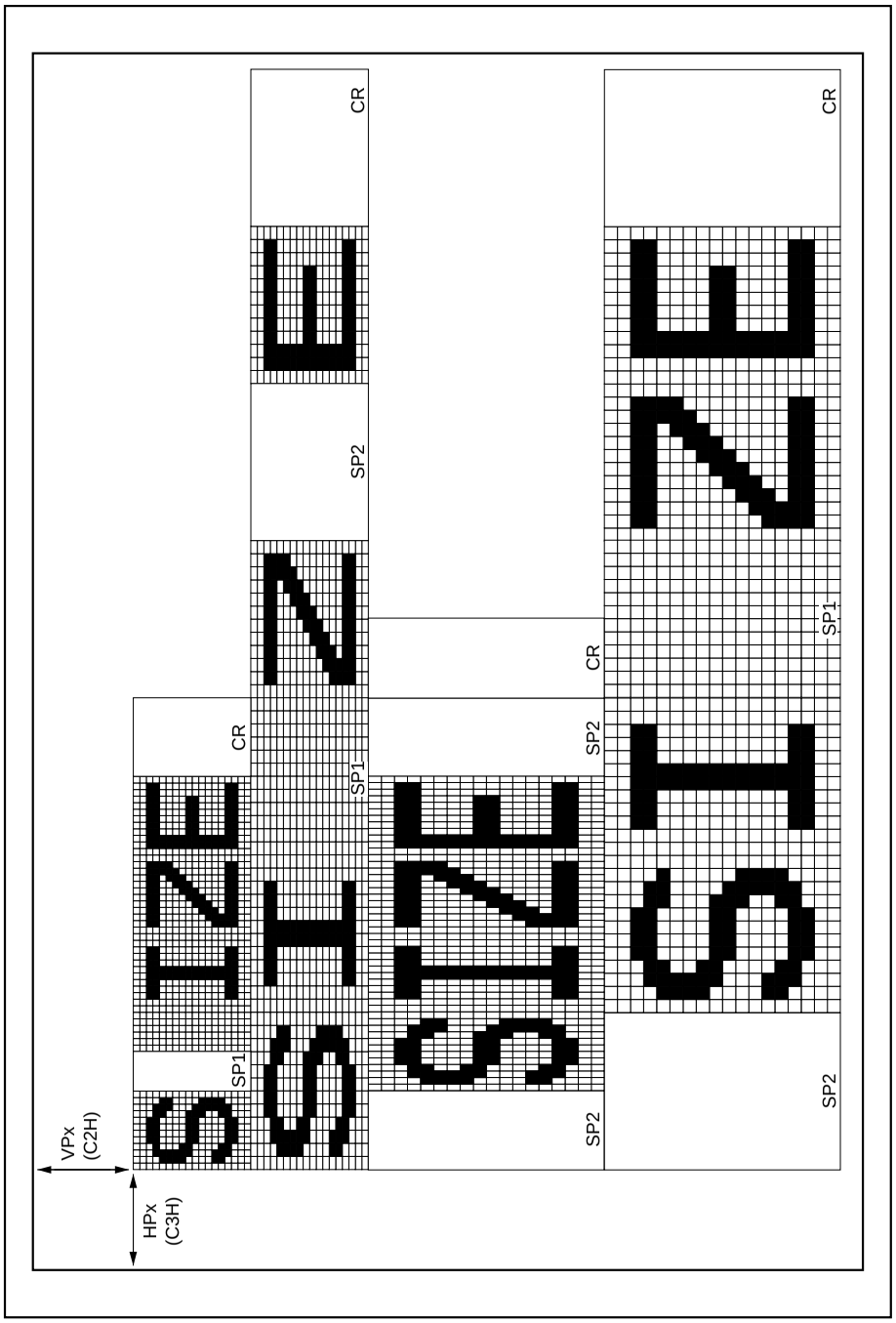


Fig.29 An example of flexible display format (Split space on).

17.3 OSD registers

17.3.1 OSD DEFAULT REGISTER (OSDDEF)

This register is used to set the default values for background colour, character size and sub-mode after each VSYNC pulse. After a system reset OSDDEF holds 22H. These values can be changed by writing new data to OSDDEF or by starting the screen with a space code (SP1 or SP2) and a CR code.

Table 49 OSD Default Register (SFR address 9CH)

7	6	5	4	3	2	1	0
R	G	B	–	SV	SH	M1	M0

Table 50 Description of OSDEF bits

BIT	SYMBOL	DESCRIPTION
7	R	**Default background colour.** These 3 bits select the default background colour.
6	G	
5	B	
4	–	This bit is reserved for future use (intensity output).
3	SV	**Default character size.** If SV = 0, then the vertical dot size is equal to one horizontal line. If SV = 1, then the vertical dot size is equal to two horizontal lines.
2	SH	**Default horizontal dot size.** If SH = 0, then the horizontal dot size is equal to one OSD clock. If SH = 1, then the horizontal dot size is equal to two OSD clocks.
1	M1	**Default sub-mode selection.** These 2 bits select the default sub-mode; see Table 51.
0	M0	

Table 51 Default sub-mode selection

M1	M0	SUB-MODE
0	0	Superimpose mode selected.
0	1	North-West shadowing mode selected.
1	0	Box background mode selected.
1	1	Border shadowing mode selected.

The default value of OSDDEF gives the following initial settings:

- Character size = 1 horizontal line/1 DOSC (Fig.31)
- Background colour = blue (R = G = 0, B = 1)
- Sub-mode = Box background mode.

17.3.2 OSD CONTROL REGISTER 1 (OSCON)

Table 52 OSD Control Register 1 (SFR address C1H)

7	6	5	4	3	2	1	0
Split	Mesh	Mode	Hp	Vp	Bp	BF	OSDE

Table 53 Description of OSCON bits

BIT	SYMBOL	DESCRIPTION
7	Split	**Split space control.** If Split = 0, then split space is disabled. If Spilt = 1, then split space is enabled on frame-by-frame basis. Split space only effects Space 1 (SP1) because Space 2 (SP2) is displayed transparent.
6	Mesh	**OSD meshing mode.** If Mesh = 0, then the OSD meshing mode is disabled. If Mesh = 1, the OSD meshing mode is enabled.
5	Mode	**Background mode selection.** If Mode = 0, then TV mode is selected (FB only active when there are characters displayed). If Mode = 1, then Frame mode is selected (FB is active in every single active scan line; FB is inactive during horizontal and vertical retrace period).
4	Hp	**HSYNC active polarity selection.** If Hp = 0, then HSYNC is an active LOW input. If Hp = 1, then HSYNC is an active HIGH input. See Fig.30.
3	Vp	**VSYNC active polarity selection.** If Vp = 0, then VSYNC is an active LOW input. If Vp = 1, then VSYNC is an active HIGH input. See Fig.30.
2	Bp	**Active R, G, B and FB output polarity selection.** If Bp = 0, then these signals are all active LOW. If Bp = 1, then these signals are all active HIGH. See Fig.31.
1	BF	**Character blinking frequency control.** If BF = 0, the blinking frequency is $\frac{1}{32}f_{VSYNC}$. If BF = 1, the blinking frequency is $\frac{1}{64}f_{VSYNC}$. The duty cycle of the blinking frequency is fixed at 1 : 1.
0	OSDE	**OSD circuit general enable/disable.** If OSDE = 0, the OSD is disabled and the R, G, B and FB signals stay in the inactive status (inverse of the Bp bit in SFR OSCON). If OSDE = 1, the OSD is enabled.

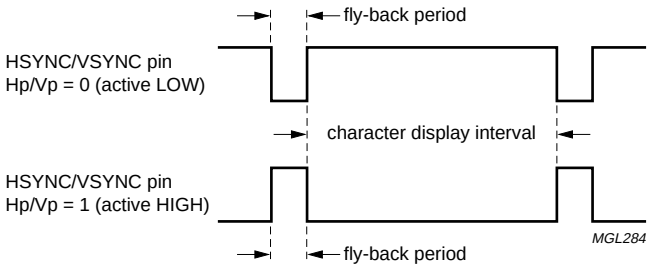


Fig.30 HSYNC and VSYNC active level selection.

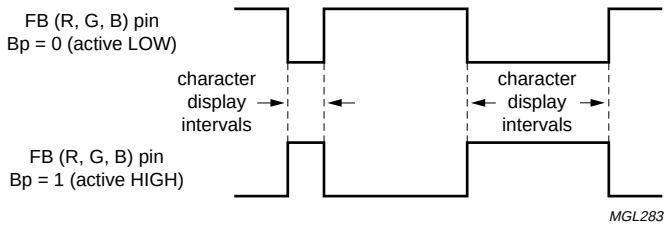


Fig.31 Active R, G, B and FB polarity control.

17.3.3 OSD VERTICAL START REGISTER (OSORGV)

Table 54 OSD Vertical Start Register (SFR address C2H)

7	6	5	4	3	2	1	0
–	–	VP5	VP4	VP3	VP2	VP1	VP0

Table 55 Description of OSORGV bits

BIT	SYMBOL	DESCRIPTION
7	–	These 2 bits are not used.
6	–	
5	VP5	**Vertical starting position selection.** These 6 bits select the vertical starting position of the OSD. 1 of 63 starting positions may be selected. The reference point of the vertical starting position is the leading edges of VSYNCP and HSYNCP. The vertical starting position (VP) is calculated as follows: $VP = 4 \times (VP5 \rightarrow VP0) \times$ horizontal scan lines Where (VP5 $\rightarrow$ VP0) is the decimal value of the contents of OSORGV and (VP5 $\rightarrow$ VP0) ≥ 1.
4	VP4	
3	VP3	
2	VP2	
1	VP1	
0	VP0	

17.3.4 OSD HORIZONTAL START REGISTER (OSORGH)

Table 56 OSD Horizontal Start Register (SFR address C3H)

7	6	5	4	3	2	1	0
–	HP6	HP5	HP4	HP3	HP2	HP1	HP0

Table 57 Description of OSORGH bits

BIT	SYMBOL	DESCRIPTION
7	–	This bit is not used.
6	HP6	**Horizontal starting position selection.** These 7 bits select the horizontal starting position of the OSD. 1 from 110 starting positions may be selected.The reference point of the horizontal starting position is the leading edge of HSYNC. The horizontal starting position (HP) is calculated as follows: $HP = 2 \times (HP6 \rightarrow HP0) \times OSD\ clock$ Where (HP6 → HP0) is the decimal value of the contents of OSORGH and (HP6 → HP0) ≥ 12H. Note that the period of the horizontal starting position plus characters display cannot be more than one HSYNC period (for example 64 μs).
5	HP5	
4	HP4	
3	HP3	
2	HP2	
1	HP1	
0	HP0	

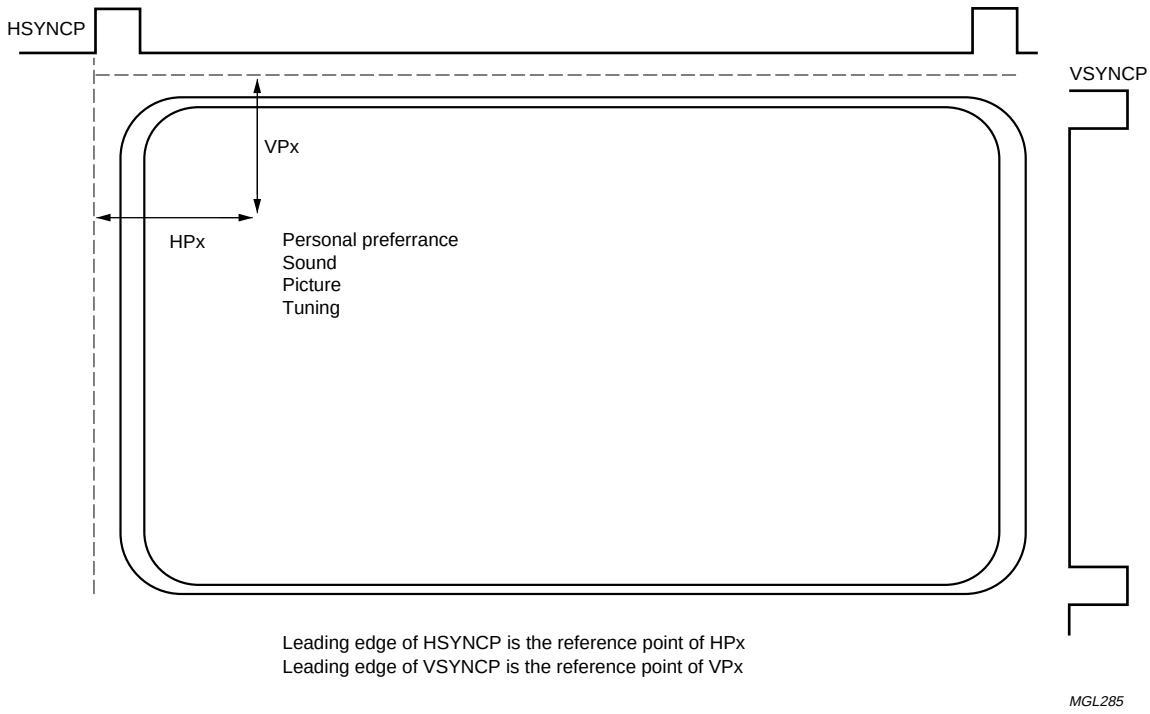


Fig.32 OSD starting position reference points.

17.3.5 OSD START REGISTER (OSSTART)

Table 58 OSD Start Register (SFR address C5H)

7	6	5	4	3	2	1	0
START7	START6	START5	START4	START3	START2	START1	START0

Table 59 Description of OSSTART bits

BIT	SYMBOL	DESCRIPTION
7	START7	**RAM start address.** These 7 bits specify the display RAM address from which the first character will be fetched. The display RAM address is from 0 to 191 decimal, or 00 to BF hexadecimal.
6	START6	
5	START5	
4	START4	
3	START3	
2	START2	
1	START1	
0	START0	

17.3.6 OSD CONTROL REGISTER 2 (OSCON2)

Table 60 OS Control Register 2 (SFR address CFH)

7	6	5	4	3	2	1	0
–	–	–	TCEN	R	G	B	–

Table 61 Description of OSCON2 bits

BIT	SYMBOL	DESCRIPTION
7	–	These 3 bits are reserved.
6	–	
5	–	
4	TCEN	**Test Code Enable.** When TCEN = 1, the content of the space from character ROM is displayed. This is valid for Space 1 and Space 2. The default value of TCEN is a logic 0. This feature is for testing purposes only.
3	R	**Background colour selection.** These 3 bits select the background colour of the TV screen in the Frame mode. The default background colour is blue.
2	G	
1	B	
0	–	This bit is reserved.

17.4 OSD clock generator

The clock generator comprises Phase-Locked-Loop circuitry. The frequency of the OSD clock is programmable and is determined by the decimal value of the contents of the 8-bit OSPLL register. OSD clock frequencies within the range 4 to 12 MHz can be selected in increments of 31.25 kHz. The OSD frequency (f_{OSD}) is calculated as shown below:

$$f_{OSD} = 2 \times f_{HSYNCP} \times (129 + \text{OSPLL value})$$

Where f_{HSYNCP} is the horizontal sync frequency after the polarity selection circuit.

17.4.1 OSD PLL Register (OSPLL)

The reset value of OSPLL is 00H.

Table 62 OSD PLL Register (SFR address C4H)

7	6	5	4	3	2	1	0
PLL7	PLL6	PLL5	PLL4	PLL3	PLL2	PLL1	PLL0

Table 63 Description of OSPLL bits

BIT	SYMBOL	DESCRIPTION
7 to 0	PLL7 to PLL0	These 8 bits are used to select the OSD clock frequency. Examples of OSD clock selection are shown in Table 64.

Table 64 Selection of OSD clock frequency

OSPLL VALUE	OSD FREQUENCY (MHz)
00H	4.00
3FH	6.00
7FH	8.00
BFH	10.00
FFH	12.00

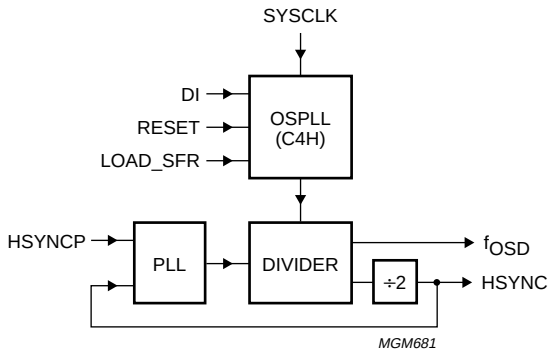


Fig.33 OSD PLL.

17.5 Display RAM organization

The display character RAM is organized as 192 × 12 bits. The general format of each RAM location is as follows. Bits <11-5> hold character data: 1 out of 128 different character fonts may be specified (126 customized fonts plus 2 reserved codes). Bits <4-0> hold attribute data of the character font, for example, colour, character size etc.

17.5.1 Display RAM formats

There are four different formats to be considered:

1. Customer character code.
2. Carriage Return code
3. Space code 1 and Space code 2.

These formats are shown in Tables 70 to 72.

17.5.1.1 Customer character code

If bits <11-5> are in the range 00H to 7CH then this is a customized character code.

Bits <4-2> select the character colour, a choice of 8 colours are available.

Bit <0> determines whether the character blinks or not. The actual blinking frequency is determined by the BF bit in SFR OSCON.

17.5.1.2 Carriage Return code

If bits <11-5> hold 7EH then this is the Carriage Return code. A transparent pattern will be displayed on the screen, the current display row will be terminated and the character stored in the display RAM next to this code will be displayed at the beginning of the next row.

Bits <4-3> select the size of the characters to be displayed in the next row. The character size is independently controlled in both the vertical and the horizontal direction. Bit <4> controls the vertical size as shown in Table 65 and bit <3> controls the horizontal size as shown in Table 66. Figure 34 shows the four different character sizes available.

Bits <2-1> select the display sub-mode of the next row. Four sub-modes can be selected (see Table 67) in either the Frame mode or the TV mode. Therefore a total of 8 different modes are available, these are illustrated in Figs 35 and 36.

Bit <0> is the end of display control bit and stops the display function before the last display RAM address (191 decimal). By combining the ‘end of display’ feature with the start RAM address (controlled by SFR OSSTART) the display RAM can be configured into several banks for fast display data switching. The states of the end of display control bit are defined in Table 68.

Table 65 Selection of vertical size

BIT 4	VERTICAL SIZE
0	One vertical dot is equal to one horizontal scan-line width.
1	One vertical dot is equal to two horizontal scan-line widths.

Table 66 Selection of horizontal size

BIT 3	HORIZONTAL SIZE
0	One horizontal dot is equal to one OSD clock width.
1	One horizontal dot is equal to two OSD clock widths.

Table 67 Selection of sub-modes

BIT 2	BIT 1	SUB-MODE
0	0	Superimpose
0	1	North-West shadowing
1	0	Box shadowing
1	1	Border shadowing

Table 68 End of display control

BIT 0	OPERATION
0	Continue to display in next row.
1	Stop the display and wait for the next display field. As soon as the horizontal and vertical starting position has been reached, continue to display.

17.5.1.3 Space code 1 and Space code 2

If bits <11-5> hold 7FH, then this is a space code. One of two space codes can be selected: Space code 1 and Space code 2.

Space code 2 always displays a transparent pattern, equal to one character width, on the screen regardless of which primary mode and sub-mode is selected. Space code 1 only differs from Space code 2 when in the Box shadowing sub-mode. In this mode SP1 displays a 12 × 18 dot matrix pattern filled with the background colour whilst SP2 displays a transparent pattern. See Figs 37 and 38.

Selection of a specific space code is determined by the state of bit 0 as detailed in Table 69.

Table 69 Selection of Space code

BIT 0	SPACE CODE
0	Space code 1 is selected.
1	Space code 2 is selected.

Bits <4-1> determine the background colour of the characters that follow the space code dependent upon the sub-mode selected, see Figs 35 and 36.

- In North-West shadowing sub-mode the background colour is the colour of the bit pattern shadow
- In Box shadowing sub-mode the background colour is the colour within the character 12 × 18 dot matrix where no foreground character bits are present
- In the Superimpose sub-mode there is no background colour
- In the Border shadowing sub-mode the background colour is the colour of the border bit pattern.

17.5.1.4 Summary of CR, SP1 and SP2 functions

- Carriage Return code:
  - Ends the current display row and uses the character in the display RAM next to this CR code as the first character of next display row
  - Selects the character size of next display row
  - Selects the character sub-mode of next display row
  - Indicates the end of display for present screen.
- Space code 1 and Space code 2:
  - Inserts transparent pattern in a row of characters
  - Selects the background colour of the characters following this space code.

Table 70 Format of Character font code

11	10	9	8	7	6	5	4	3	2	1	0
Character Font code (00H to 7CH)							Foreground colour				Blink
C6	C5	C4	C3	C2	C1	C0	T4	T3	T2	T1	T0

Table 71 Format of Carriage Return code

11	10	9	8	7	6	5	4	3	2	1	0
Carriage Return code (7EH)							Character size		Mode		End
C6	C5	C4	C3	C2	C1	C0	T4	T3	T2	T1	T1

Table 72 Format of Space code

11	10	9	8	7	6	5	4	3	2	1	0
Space code 1 and Space code 2 (7FH)							Background colour			0	SP1 SP2
C6	C5	C4	C3	C2	C1	C0	T4	T3	T2	T1	T0

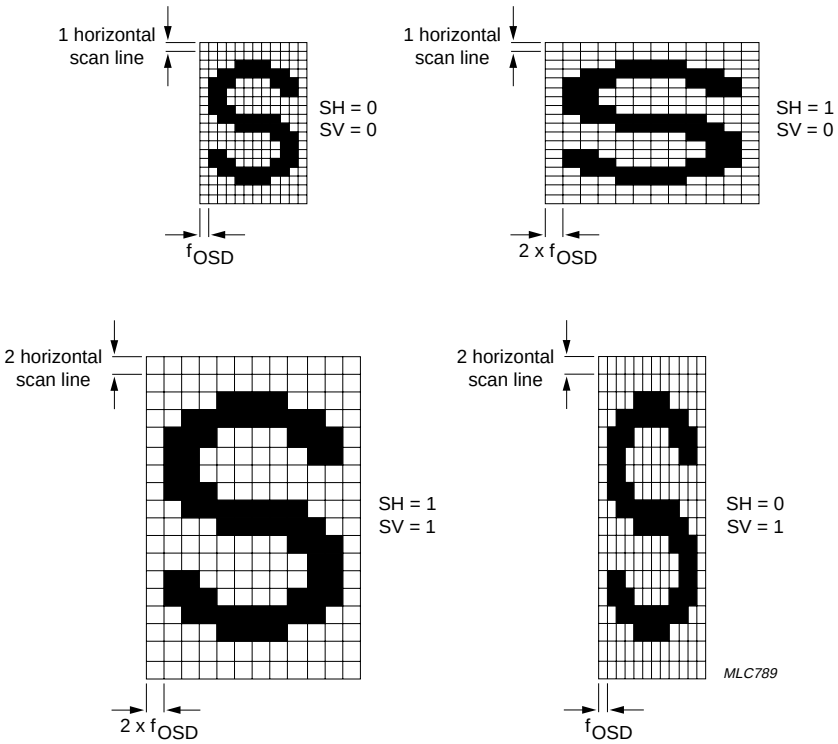


Fig.34 Four different character size combinations.

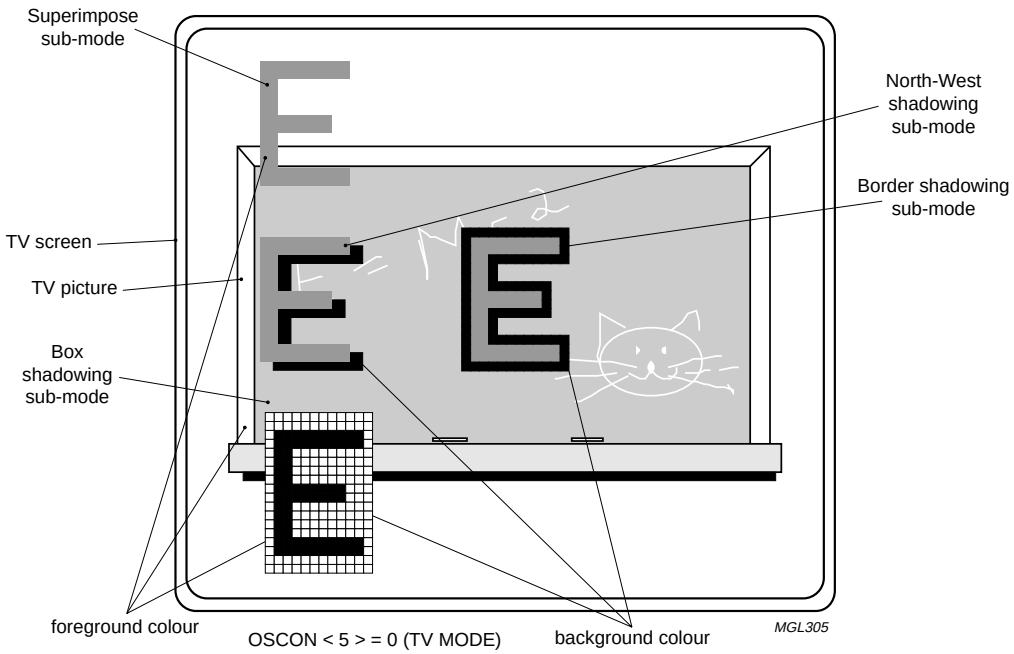


Fig.35 Four different sub-modes in TV mode.

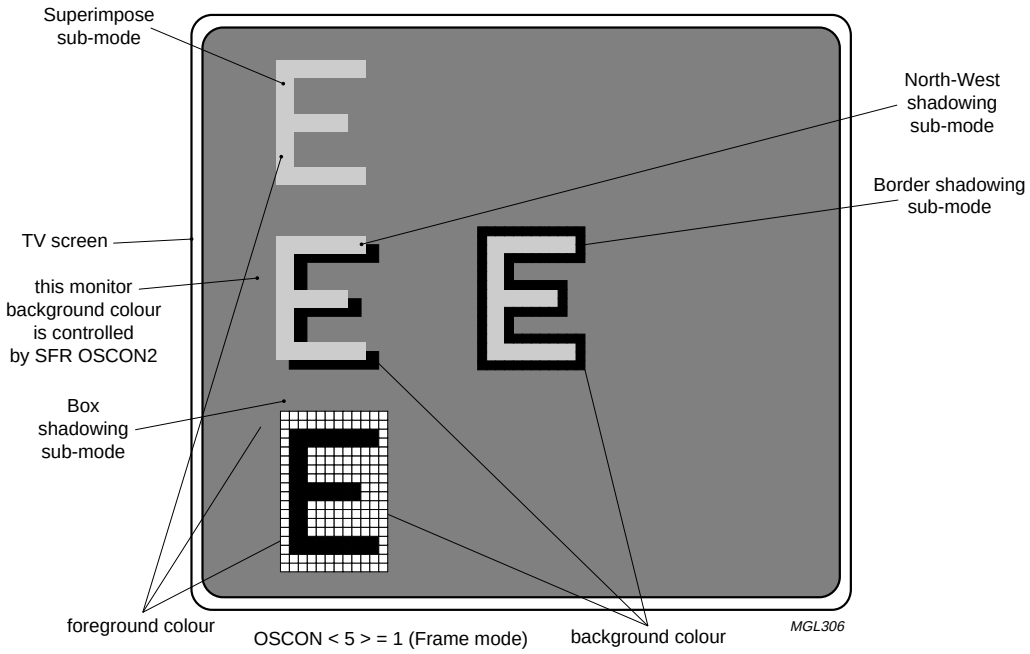


Fig.36 Four different sub-modes in Frame mode.

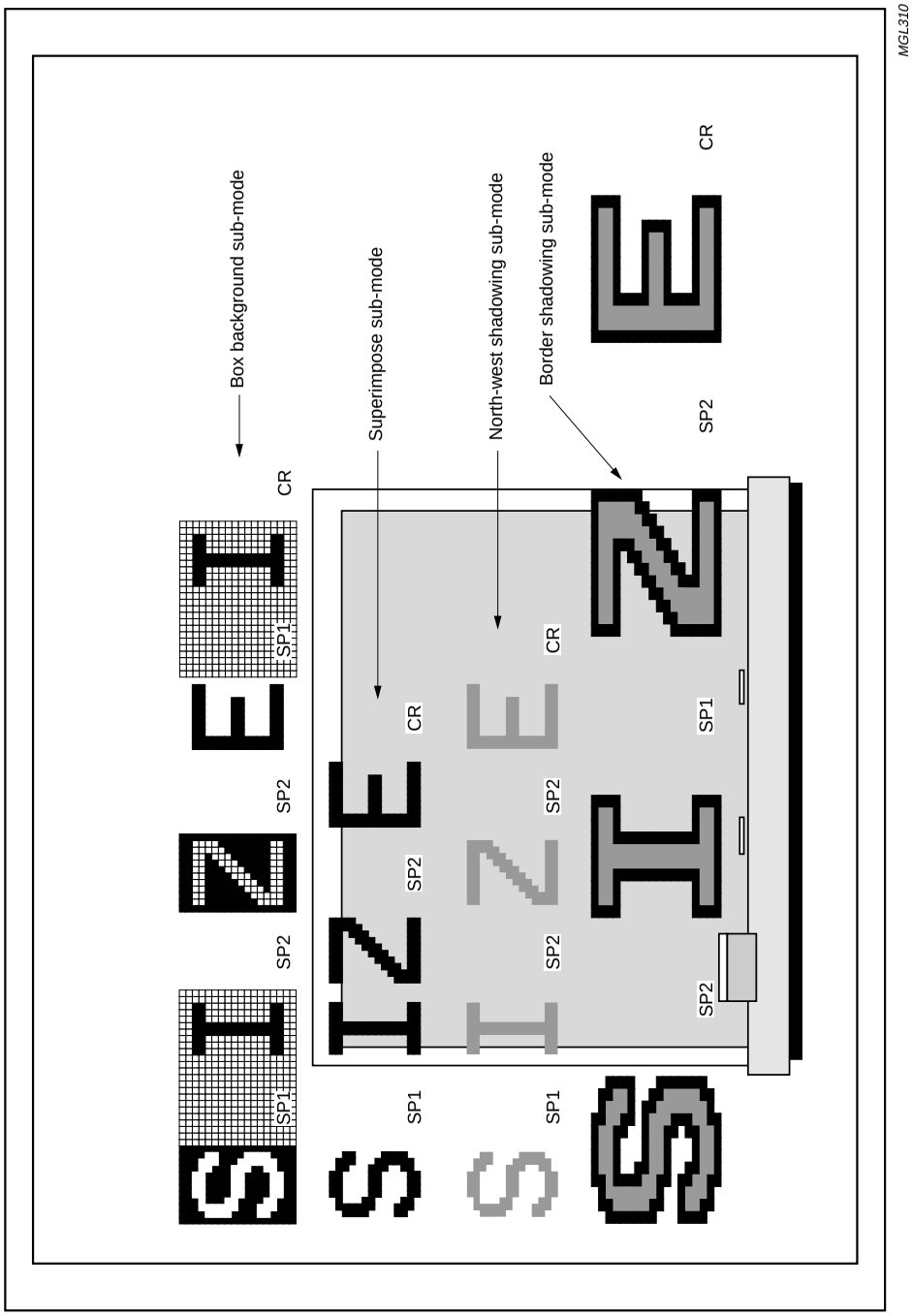


Fig.37 SP1 and SP2 codes in the 4 sub-modes of TV mode.

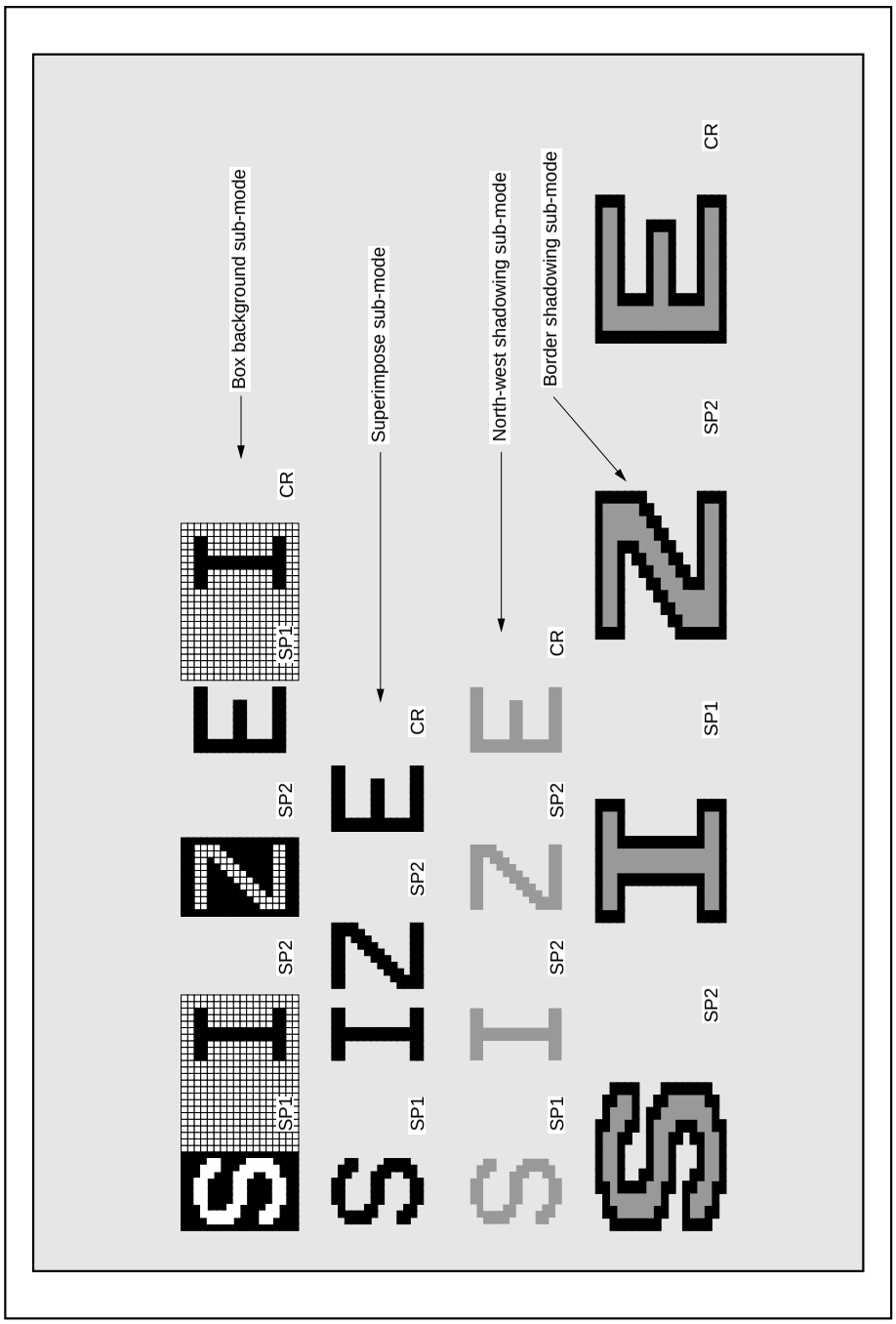


Fig.38 SP1 and SP2 codes in the 4 sub-modes of Frame mode.

17.6 Loading character data into display RAM

Three registers are used to address and load data into the display RAM: OSAD, OSDT and OSAT. These registers are described in Sections 17.6.1 to 17.6.3.

17.6.1 OSD Address Register (OSAD)

This register holds the address of the location in display RAM, into which character data is to be written.

Table 73 OSD Address Register (address 9BH)

7	6	5	4	3	2	1	0
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

17.6.2 OSD Data Register (OSDT)

This register holds the character font data that will be loaded into bits <11-5> of the location in RAM addressed by the contents of OSAD.

Table 74 OSD Data Register (address 9AH)

7	6	5	4	3	2	1	0
–	C6	C5	C4	C3	C2	C1	C0

17.6.3 OSD Attribute Register (OSAT)

This register is loaded with character attribute data. The data will be loaded into bits <4-0> of the location in RAM addressed by the contents of OSAD. The actual attribute is dependent upon whether the Character Font Code, Carriage Return Code, Space Code 1 or Space Code 2 has been selected.; this is explained in Section 17.5.1. Bits 7 to 5 are not used and are reserved.

Table 75 OSD Attribute Register (address 99H)

7	6	5	4	3	2	1	0
–	–	0	T4	T3	T2	–	T0

17.7 Writing character data into the display RAM

The procedure for writing character data into the display RAM is as follows:

1. Initialize the starting address of the display RAM by writing data into OSAD.
2. Write the character attributes to OSAT. If the attributes of a series of displayed characters are the same, the contents of this register need not be changed; only OSDT need be updated.
3. Write the character font code to be displayed to OSDT. When the write to OSDT operation is finished an automatic transfer occurs that loads the data stored in OSAT and OSDT into the display RAM location addressed by OSAD. The address held in OSAD is then incremented by ‘1’.
4. Post increment operation is executed in OSAD (OSAD ← OSAD + 1) making it point to the next RAM location. On overflow OSAD is cleared. Figure 39 shows the post-increment operation.

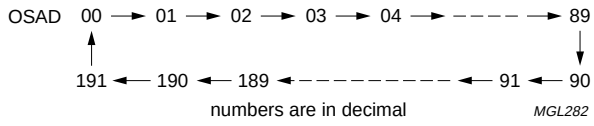


Fig.39 OSAD post-increment operation.

17.8 Character ROM

128 character fonts may be stored in ROM: 126 customer selected character fonts plus two reserved codes (the Carriage Return code and the Space code).

Each character font is stored in a 12×19 dot matrix in character ROM. However, only elements in rows 1 to 18 can be selected as visible dots on the TV screen. Row 0 is used only in the North-West shadowing sub-mode and the Border shadowing sub-mode when two character cells are to be combined in a vertical direction to formulate a new pattern. If combination of character fonts is not required then row 0 should be filled with zeros. An example of a bit pattern stored in ROM is shown in Fig.40.

A software package that helps the customer design the character fonts on the screen and that also generates the bit pattern HEX files automatically, is available on request, from local Philips sales organisations. The package is run under the MS-DOS environment for IBM compatible PCs.

17.9 Character ROM organization

ROM is divided into two parts: OSDL and OSDH.
The address of OSDL is from 0000H to 0FFFH and the address of OSDH is from 1000H to 1FFFH.

The organisation of the bit patterns stored in ROM and the file format to submit to Philips for customized character sets is shown in Fig.40. Regarding Fig.40 the following points should be noted.

1. Each character is structured using 38 bytes.
2. Row 0 of each font is reserved for vertical combination of two fonts. In vertical mergence row 0 holds the same code as row 18 of the previous font.
3. Binary 1 denotes visual dots.
4. ROM data files are in Intel HEX format on a byte basis. Each byte is structured high nibble followed by low nibble.
5. The unused bytes in ROM must be filled with FFH.

17.10 Combination of two or more font cells

Two (or more) character font cells may be combined in a vertical or horizontal direction to create a new higher resolution pattern.

The combination of two cells in a horizontal direction is straight forward and presents no problems to the user. All 4 background/shadowing sub-modes can be used.

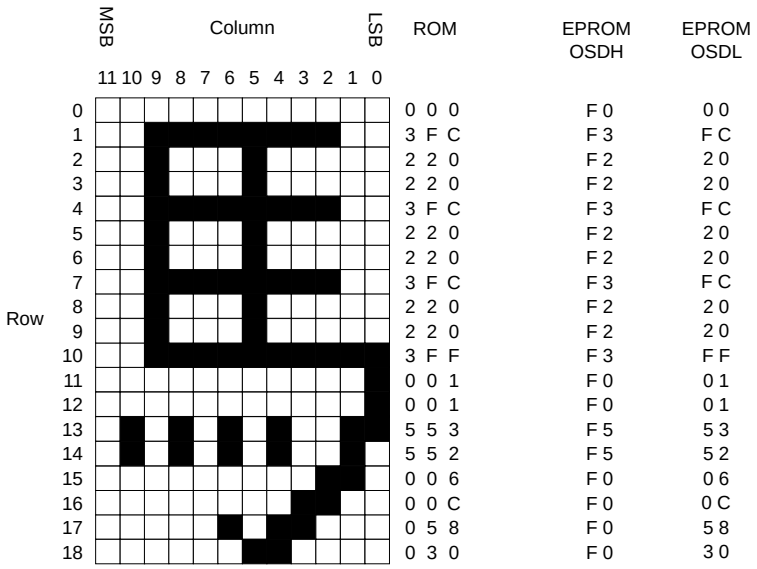
However, the combination of two character font cells in a vertical direction is more difficult and care must be taken otherwise the new pattern may be created with gaps in its shadowing.

- Row 0 in the character ROM is for use in the North-West shadowing and Border shadowing sub-modes. If either of these sub-modes is selected when combining two character cells in a vertical direction then row 0 must contain the bit pattern of row 18 of the font above it otherwise a broken dot in the shadow may occur.

17.11 More about North-West shadowing and Border shadowing sub-modes

Some special care must be taken when designing the character bit pattern if the character is intended to be used in the North-West shadowing or Border shadowing sub-mode.

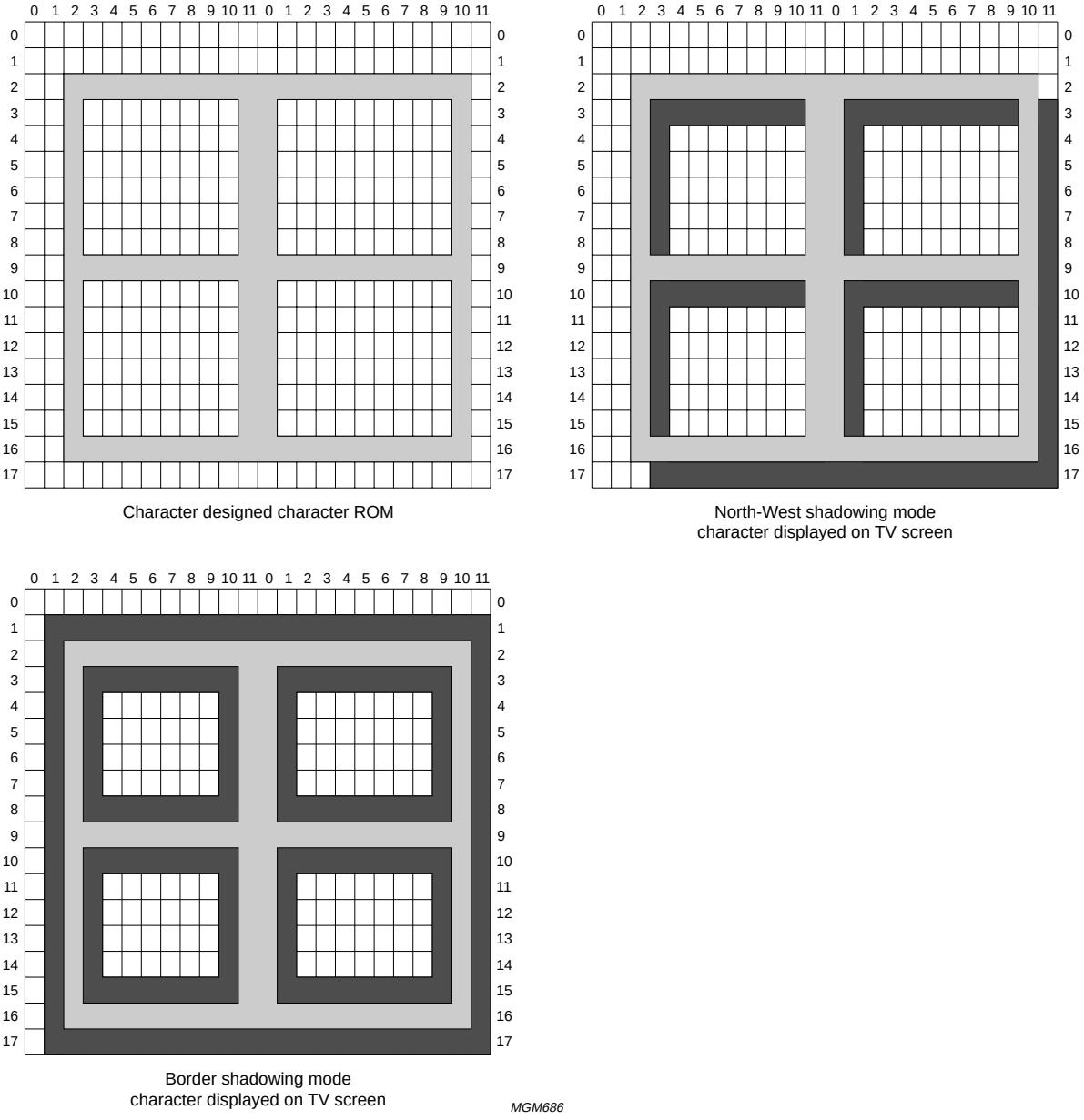
- North-West shadowing and Border shadowing sub-modes are limited in the 18 display scan lines box only in the vertical direction if the character in the next row is not in North-West shadowing sub-mode (otherwise as described in Section 17.10) if the shadow of the last foreground bit pattern line is intended to be seen as well. To get correct shadowing following the character font then in:
  - North-West shadowing: row 18 must be blank
  - Border shadowing: row 1 and 18 must be blank.
- North-West shadowing and Border shadowing sub-modes are not limited to the 12 horizontal OSD dots. Shadows of the previous font cell may cross over the 12 dot boundary and appear in the next font cell.



Intel Hex Format	Byte#	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
10 0000 00		00	FC	20	20	FC	20	20	FC	20	20	FF	01	01	53	52	06
10 0010 00		0C	58	30	←	---	---	Data for font 2 OSDL									
10 0020 00					---	---	→	←	Data for font 3 OSDL								
10 0030 00								---	---	→	←	Data for font 4					
10 0040 00		OSDL									---	---	→				
.....					....	....	....	....	....	....	....	....					
10 0FE0 00		FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
10 0FF0 00		FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
10 1000 00		F0	F3	F2	F2	F3	F2	F2	F3	F2	F2	F3	F0	F0	F5	F5	F0
10 1010 00		F0	F0	F0	←	---	---	Data for font 2 OSDH									
10 1020 00					---	---	→	←	Data for font 3 OSDH								
10 1030 00								---	---	→	←	Data for font 4					
10 1040 00		OSDH									---	---	→				
.....					....	....	....	....	....	....	....	....					
10 1FE0 00		FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
10 1FF0 00		FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF

MGL312

Fig.40 Character bit pattern stored in on-chip ROM.



The minimum dot size is 1. Take 1 horizontal line × as an example of the character displayed on the TV screen, in both the North-West and Border shadowing submodes.

Fig.41 Combination of two font cells in a horizontal direction.

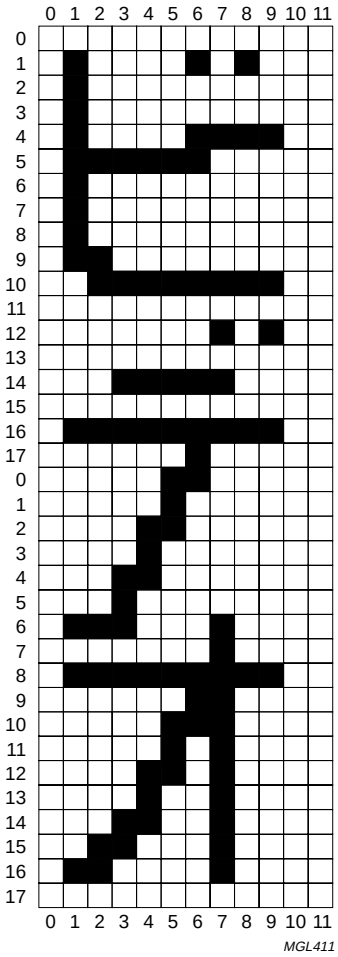


Fig.42 Combination of two font cells in a vertical direction.

17.12 Maximum number of characters per row

The number of characters per row is a function of the OSD clock frequency and the TV standard used.

The active video signal period of a horizontal line is 53.5 μs. However, in order to reduce jittering at the screen edge, overscan is normally applied by the TV manufacturer and this reduces the visible video signal period to 48.15 μs.

The examples given below show how the number of characters per row and the character width may be obtained for the NTSC 525LPF/60 Hz TV standard using different OSD clock frequencies.

17.12.1 NTSC 525LPF/60 Hz; f_{OSD} = 6 MHz

- As f_{OSD} = 6 MHz; T_{OSD} = 0.1666 μs
- The number of visible dots on one horizontal line is 290 (48.15 μs/0.1666 μs)
- Each character is composed of a 12 x 18 dot matrix; therefore the maximum number of characters on one line is 24 (290/12)
- If a 19 inch TV screen is used, the width of a horizontal line is approximately 370 mm and this gives a character width of 15.4 mm (370/24).

17.12.2 NTSC 525LPF/60 Hz; f_{OSD} = 10 MHz

- As f_{OSD} = 10 MHz; T_{OSD} = 0.1 μs
- The number of visible dots on one horizontal line is 481 (48.15 μs/0.1 μs)
- Each character is composed of a 12 x 18 dot matrix; therefore the maximum number of characters on one line is 40
- If a 19 inch TV screen is used, the width of a horizontal line is approximately 370 mm and this gives a character width of 9.25 mm.

17.13 Maximum number of rows per frame

The number of rows per frame is a function of the number of active lines per display field and the number of vertical dots in the character matrix (which is 18). The number of rows per frame (N) is calculated as shown below.

$$N = \frac{\text{number of active lines per field}}{18}$$

The two examples shown below illustrate how the maximum number of rows per frame is obtained for different TV scanning standards.

17.13.1 NTSC 525LPF/60 Hz

The number of active lines per field for this standard is between 241.5 and 249 H. If the value of 241 is used then the maximum number of rows per frame is 13.

17.13.2 PAL 625LPF/50 Hz

The number of active lines per field for this standard is 280. Therefore, the maximum number of rows per frame is 15.

17.14 OSD vertical debouncing circuit

The HSYNC and VSYNC signals entering the OSD circuit are usually extracted from the horizontal and vertical deflection units of a television set. The shaping and timing of these signals is therefore related to several external conditions that all have certain tolerances. The trigger levels of the input circuitry also influence the internal timing of HSYNC and VSYNC. In the odd field the leading edge of both signals is very close, so jitter on one or both of them may result in occasionally miscounting the number of lines in a field causing a displayed character to bounce up and down on a line. To avoid this situation the HSYNC signal is delayed by a number of dot clocks. Because the relationship between HSYNC and VSYNC is not fully known there are 16 user selectable delays available. The period of the horizontal starting position plus the HDEL delay cannot exceed the HSYNC period.

17.14.1 Horizontal Delay Register (HDEL)

Table 76 Horizontal Delay Register (SFR address C6H)

7	6	5	4	3	2	1	0
–	–	–	–	HDEL3	HDEL2	HDEL1	HDEL0

Table 77 Description of HDEL bits

BIT	SYMBOL	DESCRIPTION
7 to 4	–	These 4 bits are reserved.
3	HDEL3	**HSYNC delay.** The state of these 4 bits determines the delay time applied to the HSYNC signal, see Table 78.
2	HDEL2	
1	HDEL1	
0	HDEL0	

Table 78 Selection of HSYNC delay

HDEL3	HDEL2	HDEL1	HDEL0	NO. OF DOT CLOCKS	DELAY TIME AT 5 MHz (μs)	DELAY TIME AT 10 MHz (μs)
0	0	0	0	0	0	0
0	0	0	1	32	6.4	3.2
0	0	1	0	64	12.8	6.4
0	0	1	1	96	19.2	9.6
0	1	0	0	128	25.6	12.8
0	1	0	1	160	32	16
0	1	1	0	192	38.4	19.2
0	1	1	1	224	44.8	22.4
1	0	0	0	256	51.2	25.6
1	0	0	1	288	57.6	28.8
1	0	1	0	320	64	32
1	0	1	1	352	70.4	35.2
1	1	0	0	384	76.8	38.4
1	1	0	1	416	83.2	41.6
1	1	1	0	448	89.6	44.8
1	1	1	1	480	96	48

17.15 OSD meshing

Meshing results is a contrast reduction of a selected video area. This reduced contrast enhances the reliability of the OSD character displayed in that area without the loss of the video information in that area in case of a normal solid background. This feature is implemented by replacing the normal character solid background by a checker-board pattern background and inverts this pattern every new frame. The checker-board pattern itself is generated by switching FB on and off with a pixel frequency in the first frame and off and on in the next frame only for those OSD characters that have background switched on.

- The OSD character itself or its contrast is not affected by the meshing feature
- The meshing function is frame based
- Normal background is replaced by an alternating meshing pattern
- For meshing the meshing bit and the background mode must be set
- Meshing can only be activated in TV mode, e.g mode bit (bit 5 in SFR OSCON) must be a logic 0.

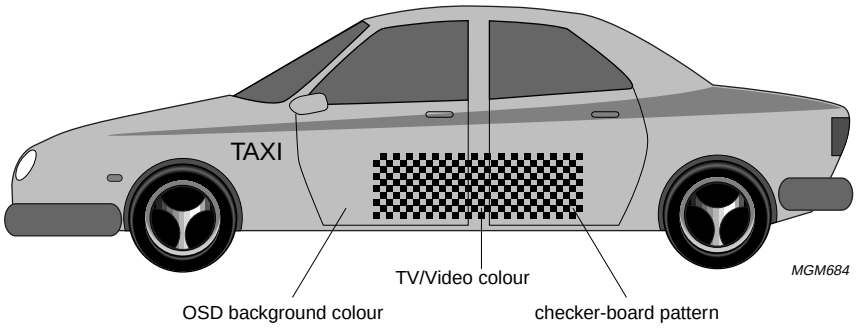


Fig.43 TV/video signal superimposed with checker-board pattern.

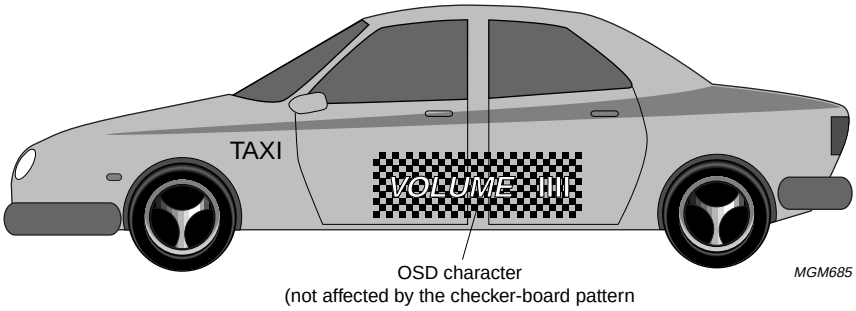


Fig.44 Complete meshing feature.

17.16 FB to RGB delay compensation

The P8xCx66 is connected to an analog video mixer. In the past analog mixers had different delays between FB and RGB. To compensate for these differences, FB to RGB delay compensation is implemented on-chip. The delay time is selected using the OSFBD register.

The delay compensation can be done with a resolution of $\frac{1}{2}f_{OSC}$. The OSC clock runs at 4 times the OSD clock frequency for OSD frequencies from 4 up to 6.75 MHz, and at 2 times the OSD clock frequency from OSD frequencies from 6.75 MHz up to 12 MHz. At 4 MHz the delay unit is 33 ns, at 6.5 MHz the delay unit is 19 ns, at 8 MHz the delay unit is 33 ns, at 10 MHz the delay unit is 25 ns and at 12 MHz the delay unit is 21 ns.

17.16.1 OSD FB Delay Register (OSFBD)

Table 79 OSD FB Delay Register (SFR address C7H)

7	6	5	4	3	2	1	0
–	–	–	0	FBD3	FBD2	FBD1	FBD0

Table 80 Description of OSFBD bits

BIT	SYMBOL	DESCRIPTION
7 to 5	–	These 3 bits are not used.
4	–	This bit must be set to a logic 0. If set to a logic 1, the character font will come from internal logic instead of character ROM.
3 to 0	FBD3 to FB D0	**FB to RGB delay select.** These 4 bits select the delay unit multiple that will determine the delay time between FB and RGB; see Table 81.

Table 81 Selection of FB to RGB delay

FBD3	FBD2	FBD1	FBD0	DECIMAL VALUE	FB to RGB DELAY
1	1	1	1	–7	Delay RGB with 7 units in relation to FB.
1	1	1	0	–6	Delay RGB with 6 units in relation to FB.
1	1	0	1	–5	Delay RGB with 5 units in relation to FB.
1	1	0	0	–4	Delay RGB with 4 units in relation to FB.
1	0	1	1	–3	Delay RGB with 3 units in relation to FB.
1	0	1	0	–2	Delay RGB with 2 units in relation to FB.
1	0	0	1	–1	Delay RGB with 1 units in relation to FB.
1	0	0	0	0	Delay RGB with 0 unit in relation to FB.
0	0	0	0	+0	Delay FB with 0 unit in relation to RGB.
0	0	0	1	+1	Delay FB with 1 unit in relation to RGB.
0	0	1	0	+2	Delay FB with 2 units in relation to RGB.
0	0	1	1	+3	Delay FB with 3 units in relation to RGB.
0	1	0	0	+4	Delay FB with 4 units in relation to RGB.
0	1	0	1	+5	Delay FB with 5 units in relation to RGB.
0	1	1	0	+6	Delay FB with 6 units in relation to RGB.
0	1	1	1	+7	Delay FB with 7 units in relation to RGB.

18 EPROM PROGRAMMER

18.1 Interface to the on-chip EPROMs

The P87C766 contains two EPROMs: the program EPROM and the OSD EPROM. The EPROM memory map is shown in Fig.46.

The 64K × 8-bit program EPROM is subdivided into four EPROM modules: Modules 1 to 4, each of 16 kbytes.

The 8K × 8-bit OSD EPROM is subdivided into two modules: OSDL and OSDH, each of 4 kbytes. The OSDL module provides the 8 LSBs of the 12-bit character word and the OSDH module provides the 4 MSBs of the 12-bit character word. The 4 MSBs of OSDH are not used and should be programmed to logic 1s.

To ensure greater reliability and to reduce power consumption, all unused EPROM cells should be programmed to logic 1s.

To program the EPROM modules, several functions of the EPROMs must be mapped to the pins of the package.

- The program EPROM uses 16 address lines: A0 to A15
  - A0 to A13 are used for the EPROM address
  - A14 and A15 are used to select one of the 4 program EPROM modules; see Table 82.
- The OSD EPROM uses 13 address lines A0 to A12
  - A0 to A11 are used for the EPROM address
  - A12 is used to select one of the 2 OSD EPROM modules; see Table 83.
- Data I/O: D0 to D7 are used for all EPROM modules
- Write Enable ($\overline{WE}$): active LOW programming pulse
- Output Enable ($\overline{OE}$): active LOW data output enable, when in EPROM verify mode, $\overline{OE}$ must be LOW
- Programming voltage: the programming and verification voltage (V_{PP}) is typically 12.75 V; when programming and verify operations have been completed V_{PP} should be reduced to 0 V.

All other signals to be connected to the EPROM module in the programming/verification mode are generated internally. Table 84 gives an overview of the functions mapped to the pins.

Programming and verification waveform characteristics are specified in Chapter 21.

Table 82 Selection of Program EPROM modules

A15	A14	PROGRAM EPROM MODULE
0	0	Module 1
0	1	Module 2
1	0	Module 3
1	1	Module 4

Table 83 Selection of OSD EPROM modules

A12	OSD EPROM MODULE
0	OSDL module
1	OSDH module

Table 84 Truth table for EPROM modules

OPERATION MODE	$\overline{WE}$	$\overline{OE}$	V_{PP}	I/O	ADDRESS LINES
Programming Program EPROM	0	1	12.75	data in	A0 to A15
Verification Program EPROM	1	0	12.75	data out	A0 to A15
Programming OSD EPROM	0	1	12.75	data in	A0 to A12
Verification OSD EPROM	1	0	12.75	data out	A0 to A12

18.2 EPROM Programming mode

In the EPROM programming mode the selected EPROM is under the direct control of the external pins. For entering the programming mode the RESET pin serves as the data input and the XTALIN pin serves as the clock input. There is no need to synchronise the addresses, data, read and write signals with the CPU.

To enter the programming mode, the microcontroller must first be reset in accordance to the normal reset procedure to avoid the Idle mode. The programming code is then shifted in serially via the RESET pin and stored in a register. After decoding, the required control signals are generated.

18.2.1 Serial programming codes

Once the device has been reset the programming code can be shifted in via the RESET pin. The 10-bit programming code is shown in Fig.45 and defined in Table 85.

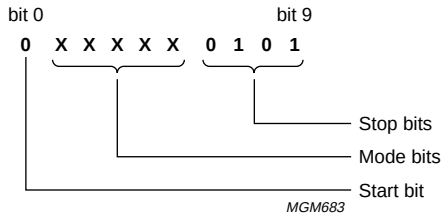


Fig.45 Serial programming code.

Table 85 Programming code format

BIT	FUNCTION
9 to 6	**Stop bits.** These are the last 4 bits to be shifted in and always take the value ‘0101’, indicating the end of the test mode code.
5 to 1	**Mode bits.** These 5 bits follow the start bit and select the test mode; see Table 86.
0	**Start bit.** This is the first bit to be shifted in and is always a logic 0, indicating that the following 5 bits are test mode code.

Table 86 Test mode selection.

MODE BITS					TEST MODE
5	4	3	2	1	
0	0	1	0	0	Program EPROM
0	0	1	1	0	OSD EPROM

18.2.2 Entering the Programming mode

The procedure for entering the Programming mode is detailed below and illustrated in Fig.47

1. The normal reset should be active for at least 24 XTALIN clocks:
   a) The first 10 XTALIN clocks cancel any special modes
   b) The 24 XTALIN clocks (2 machine cycles) ensure that the CPU core is reset.
2. Shift in the programming code via the RESET pin
3. Wait at least 2 XTALIN clocks until the control signals are ready, then the EPROM address, data and control signals can be applied. The RESET pin should be released within 10 XTALIN clocks to prevent the circuit escaping from EPROM programming mode.

18.2.3 Leaving the Programming mode

The device will exit the Programming mode when the RESET pin is driven HIGH for at least 10 XTALIN clock cycles.

18.3 Programming and verification

It is not recommended to carry out programming/verify operations on a byte basis. It is far better to program all program EPROM (or OSD EPROM) and then verify the contents.

18.4 OSD EPROM bit map and the sequence of programming OSDL and OSDH

Each character bit pattern is stored in the on-chip ROM/EPROM. The character displayed on the screen is in a 12×18 dot matrix format, however it is stored in the on-chip character ROM in a 12×19 format. For the OSD EPROM character the dot matrix is 16×19, but only 12×19 is used, therefore the high nibble of OSDH must be filled with FH.

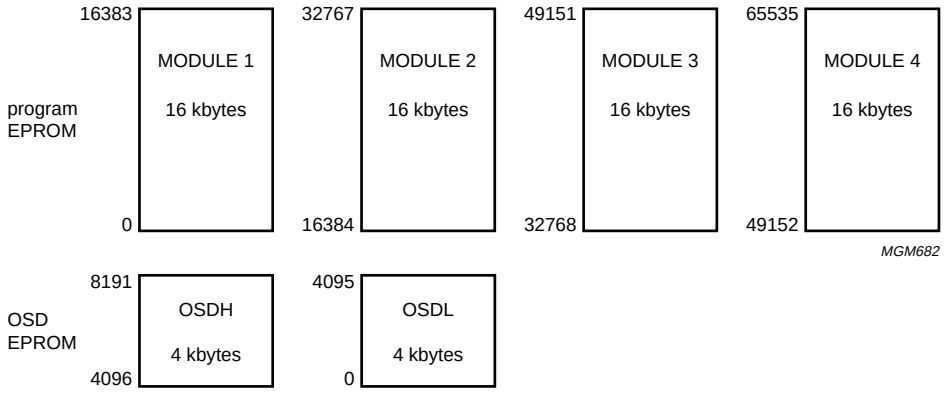


Fig.46 On-chip EPROM structure for the P87C766.

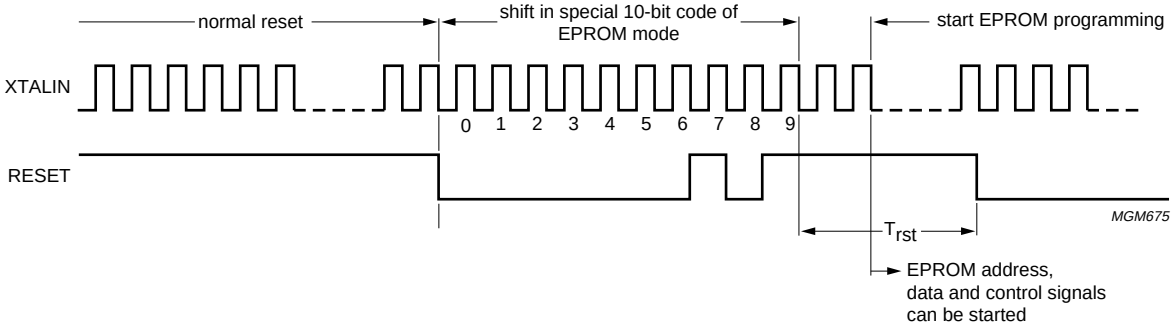


Fig.47 Sequence to enter EPROM programming mode.

18.5 Summary of the Programming mode configuration

Table 87 Pin connections in Programming mode.

SYMBOL	PIN	EPROM CONNECTION	
		PROGRAM	OSD
P3.3/PWM7	12	A15	–
P5.7/PWM6	8	A14	–
P5.6/PWM5	7	A13	–
P5.5/PWM4	6	A12	A12
P5.4/PWM3	5	A11	A11
P5.3/PWM2	4	A10	A10
P5.2/PWM1	3	A9	A9
P5.1/PWM0	2	A8	A8
P1.4/T1	38	A7	A7
P1.3/INT0	37	A6	A6
P1.2/T0	36	A5	A5
P1.1/INT1	35	A4	A4
VSYNC	27	A3	A3
HSYNC	26	A2	A2
FB	25	A1	A1
R	24	A0	A0
G	23	$\overline{OE}$	$\overline{OE}$
B	22	$\overline{WE}$	$\overline{WE}$
P0.7	20	data I/O, bit 7	data I/O, bit 7
P0.6	19	data I/O, bit 6	data I/O, bit 6
P0.5	18	data I/O, bit 5	data I/O, bit 5
P0.4	17	data I/O, bit 4	data I/O, bit 4
P0.3	16	data I/O, bit 3	data I/O, bit 3
P0.2	15	data I/O, bit 2	data I/O, bit 2
P0.1	14	data I/O, bit 1	data I/O, bit 1
P0.0	13	data I/O, bit 0	data I/O, bit 0
V_{PP}	30	V_{PP}	V_{PP}

Table 88 EPROM module selection.

MEMORY SIZE	ADDRESS LINES	DATA LINES
Program EPROM: Module 1		
16K × 8	14-bit address: A0 to A13; Module 1 select: A14 = 0, A15 = 0	8-bit data byte: D0 to D7
Program EPROM: Module 2		
16K × 8	14-bit address: A0 to A13; Module 2 select: A14 = 1, A15 = 0	8-bit data byte: D0 to D7
Program EPROM: Module 3		
16K × 8	14-bit address: A0 to A13; Module 3 select: A14 = 0, A15 = 1	8-bit data byte: D0 to D7
Program EPROM: Module 4		
16K × 8	14-bit address: A0 to A13; Module 4 select: A14 = 1, A15 = 1	8-bit data byte: D0 to D7
OSD EPROM (OSDL) – LSBs		
128 × 19 × 8	12-bit address: A0 to A11; OSDL select: A12 = 0	8-bit data byte: D0 to D7
OSD EPROM (OSDH) – MSBs		
128 × 19 × 8	12-bit address: A0 to A11; OSDH select: A12 = 1	8-bit data byte: D0 to D7

19 SPECIAL FUNCTION REGISTERS ADDRESS MAP

The SFRs are presented in ascending address order in Table 89 to aid designer/programmers quick reference.

Table 89 SFRs address map

ADDRESS	NAME	7	6	5	4	3	2	1	0
80H(1)	P0 latch	P07	P06	P05	P04	P03	P02	P01	P00
81H(1)	Stack Pointer (SP)	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
82H(1)	Data Pointer Low (DPL)	DPL7	DPL6	DPL5	DPL4	DPL3	DPL2	DPL1	DPL0
83H(1)	Data Pointer High (DPH)	DPH7	DPH6	DPH5	DPH4	DPH3	DPH2	DPH1	DPH0
86H	I^2C-bus Port Control Register (I^2CCON)	–	–	–	–	–	I^2CE	–	–
87H(1)	Power Control Register (PCON)	–	–	–	WLE	GF1	GF0	0	IDL
88H(1)	Timer/Counter Control Register (TCON)	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
89H(1)	Timer/Counter Mode Control Register (TMOD)	Gate	C/T	M1	M0	Gate	C/T	M1	M0
8AH(1)	Timer 0 Low byte (TL0)	TL07	TL06	TL05	TL04	TL03	TL02	TL01	TL00
8BH(1)	Timer 1 Low byte (TL1)	TL17	TL16	TL15	TL14	TL13	TL12	TL11	TL10
8CH(1)	Timer 0 High byte (TH0)	TH07	TH06	TH05	TH04	TH03	TH02	TH01	TH00
8DH(1)	Timer 1 High byte (TH1)	TH17	TH16	TH15	TH14	TH13	TH12	TH11	TH10
90H(1)	P1 latch	P17	P16	P15	P14	P13	P12	P11	P10
98H	P5 latch	P57	P56	P55	P54	P53	P52	P51	P50
99H	OSD Attribute Register (OSAT)	–	–	–	T4	T3	T2	–	T0
9AH	OSD Character Data Register (OSDT)	C7	C6	C5	C4	C3	C2	C1	C0
9BH	OSD Address Register (OSAD)	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
9CH	OSD Default Register (OSDDEF)	R	G	B	–	SV	SH	M1	M0
A0H(1)	P2 latch	P27	P26	P25	P24	P23	P22	P21	P20
A8H(1)	Interrupt Enable Register 0 (IEN0)	EA	–	ES1	–	ET1	EX1	ET0	EX0
B0H(1)	P3 latch	–	–	–	–	P33	P32	P31	P30
B8H(1)	Interrupt Priority Register 0 (IP0)	–	–	PS1	–	PT1	PX1	PT0	PX0
C0H	Interrupt Request Register 1 (IRQ1)	IQ9	–	IQ7	IQ6	IQ5	IQ4	IQ3	IQ2
C1H	OSD Control Register 1 (OSCON)	Split	Mesh	Mode	Hp	Vp	Bp	BF	OSDE
C2H	OSD Vertical Start Register (OSORGV)	–	–	VP5	VP4	VP3	VP2	VP1	VP0
C3H	OSD Horizontal Start Register (OSORGH)	–	HP6	HP5	HP4	HP3	HP2	HP1	HP0
C4H	OSD PLL Register (OSPLL)	PLL7	PLL6	PLL5	PLL4	PLL3	PLL2	PLL1	PLL0
C5H	OSD Start Register (OSSTART)	START7	START6	START5	START4	START3	START2	START1	START0

ADDRESS	NAME	7	6	5	4	3	2	1	0
C6H	Horizontal Delay Register (HDEL)	–	–	–	–	HDEL3	HDEL2	HDEL1	HDEL0
C7H	OSD FB Delay Register (OSFBD)	–			0	FBD3	FBD2	FBD1	FBD0
C8H	ADC Control Register (SAD)	#VHI	CH1	CH0	ST	SAD3	SAD2	SAD1	SAD0
C9H(1)	VSYNC Interrupt Register (VINT)	–	–	–	–	–	–	–	VLVL
CAH	ADC Control Register 2 (SAD2)	–	–	–	–	–	ADCE2	ADCE1	ADCE0
CFH	OSD Control Register 2 (OSCON2)	–	–	–	0	R	G	B	–
D0H(1)	Program Status Word (PSW)	#CY	#AC	#F0	RS1	RS0	#OV	–	#P
D2H	TDACL	TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0
D3H	TDACH	TPWME	–	TD13	TD12	TD11	TD10	TD9	TD8
D8H	Serial Control Register (S1CON)	CR2	ENS1	STA	STO	SI	AA	CR1	CR0
D9H(2)	Status Register (S1STA)	SC4	SC3	SC2	SC1	SC0	0	0	0
DAH	Data Shift Register (S1DAT)	D7	D6	D5	D4	D3	D2	D1	D0
DBH	Slave Address Register (S1ADR)	SLA6	SLA5	SLA4	SLA3	SLA2	SLA1	SLA0	GC
DCH(2)	Internal Status Register (S1IST)	MST4	TX	BB	FB	ARL	SEL	AD0	SHRA
E0H(1)	Accumulator (ACC)	ACC7	ACC6	ACC5	ACC4	ACC3	ACC2	ACC1	ACC0
E4H	PWM0 (7-bit PWM)	PWM0E	data6	data5	data4	data3	data2	data1	data0
E5H	PWM1 (7-bit PWM)	PWM1E	data6	data5	data4	data3	data2	data1	data0
E6H	PWM2 (7-bit PWM)	PWM2E	data6	data5	data4	data3	data2	data1	data0
E7H	PWM3 (7-bit PWM)	PWM3E	data6	data5	data4	data3	data2	data1	data0
E8H(1)	Interrupt Enable Register 1 (IEN1)	EX9	–	EX7	EX6	EX5	EX4	EX3	EX2
E9H(1)	Interrupt Polarity Register (IX1)	IL9	IL8	IL7	IL6	IL5	IL4	IL3	IL2
ECH	PWM4 (7-bit PWM)	PWM4E	data6	data5	data4	data3	data2	data1	data0
EDH	PWM5 (7-bit PWM)	PWM5E	data6	data5	data4	data3	data2	data1	data0
EEH	PWM6 (7-bit PWM)	PWM6E	data6	data5	data4	data3	data2	data1	data0
EFH	PWM7 (7-bit PWM)	PWM7E	data6	data5	data4	data3	data2	data1	data0
F0H(1)	B Register (B)	B7	B6	B5	B4	B3	B2	B1	B0
F8H	Interrupt Priority Register 1 (IP1)	PX9	–	PX7	PX6	PX5	PX4	PX3	PX2
FFH	Watchdog timer Register (WDT)	T37	T36	T35	T34	T33	T32	T31	T30

Notes

1. Standard 80C51 register.
2. Read only register.

20 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDX}	any supply voltage	4.5	–	5.5	V
V_I	input voltage (all inputs)	–0.5	–	V_{DD} + 0.5	V
P_{tot}	total power dissipation	–	–	170	mW
T_{stg}	storage temperature	–55	–	+125	°C
T_{amb}	operating ambient temperature	–20	–	70	°C

21 CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = –20 to 70 °C; all voltages with respect to V_{SS} unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
I_{DDD}	digital supply current	f_{CLK} = 12 MHz	–	–	32	mA
I_{DDA}	analog supply current	f_{CLK} = 12 MHz	–	–	5.0	mA
V_{PP}	programming voltage		12.5	12.75	13	V
I_{PP}	programming current		–	–	10	mA
CMOS inputs						
V_{IL}	LOW-level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	–	V
I_{LI}	input leakage current	$V_{SS} < V_I < V_{DD}$	–10	–	+10	µA
CMOS inputs (Schmitt trigger)						
V_{IL}	LOW-level input voltage		$0.2V_{DD}$	–	–	V
V_{IH}	HIGH-level input voltage		–	–	$0.8V_{DD}$	V
TTL inputs						
V_{IL}	LOW-level input voltage		–	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	–	V
TTL inputs (Schmitt trigger)						
V_{IL}	LOW-level input voltage		0.6	–	–	V
V_{IH}	HIGH-level input voltage		–	–	2.4	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog inputs: ADC0 to ADC2						
V_I	input voltage		V_{SS}	–	V_{DD}	V
Push-pull outputs: R, G, B and FB						
I_{OL}	LOW-level output current		–	–	1.6	mA
I_{OH}	HIGH-level output current		–	–	–1.6	mA
Open-drain outputs						
$t_{t(L-H)}$	transition time LOW to HIGH	determined by external RC network	25	–	100	ns
$t_{t(H-L)}$	transition time HIGH to LOW	load independent slope control for a capacitance load up to 50 pF	25	–	100	ns
$I_{O(sink)}$	output sink current logic 0	V_{OL} = 0.4	–	–	1.6	mA
		V_{OL} = 1.0	–	–	10	mA
System clock						
f_{CLK}	system clock frequency		4	–	12	MHz
OSD clock						
f_{OSD}	OSD clock frequency		4	–	12	MHz

21.1 DC parameters of EPROM

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
T_{oper}	operating temperature (programming/verification)	–	25	–	°C
I_{PP}	programming current	–	–	10.0	mA
V_{PP}	programming voltage	12.50	12.75	13.0	V

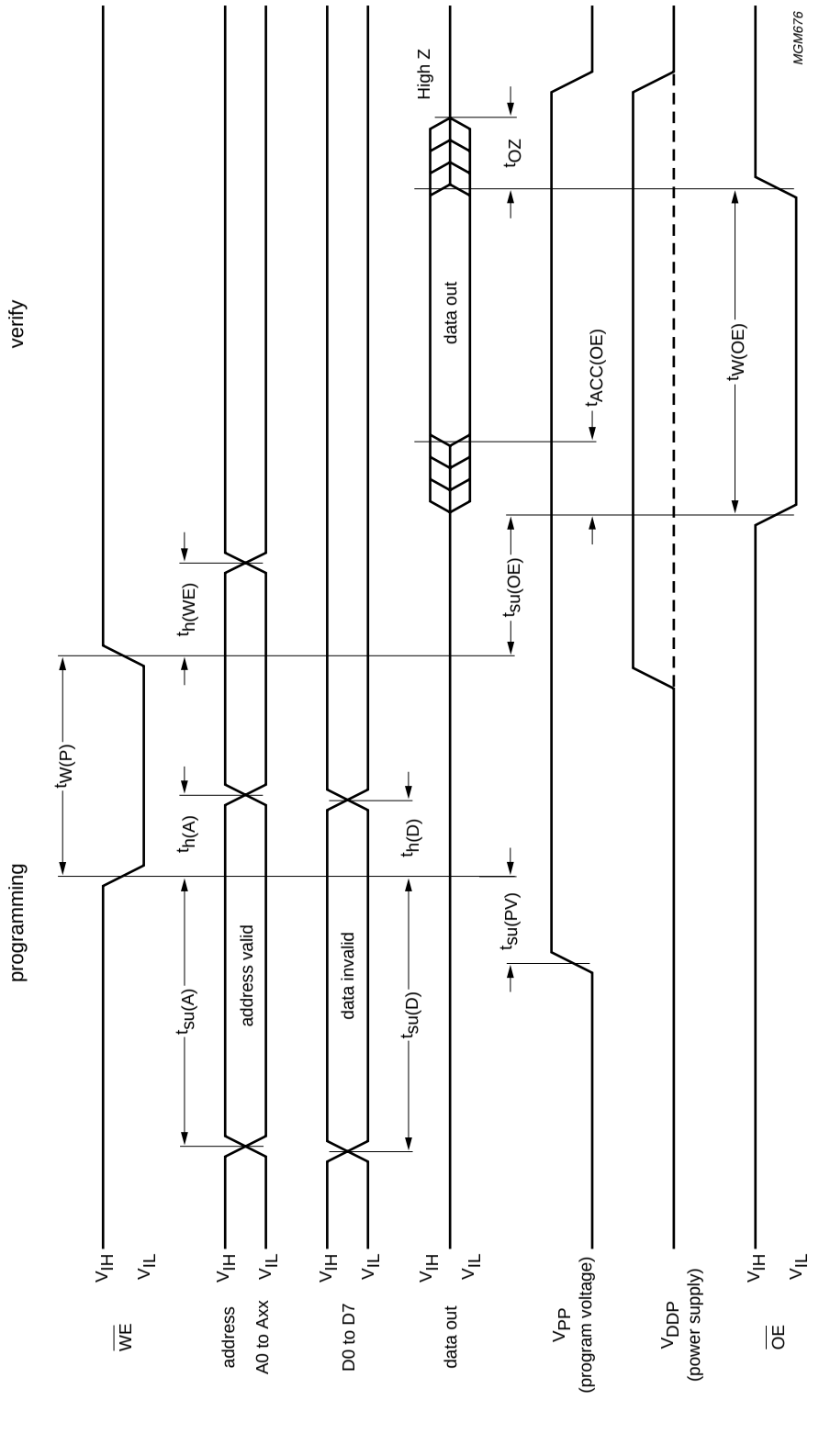
21.2 Programming specification for programmer

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
T_{oper}	operating temperature (programming/verification)	–	25	–	°C
V_{DD}	supply voltage (reading)	4.5	5.0	5.5	V
V_{DDP}	supply voltage (programming)	–	5.0	–	V
V_{DDP}	supply voltage (verify)	–	5.8	–	V
$t_{W(P)}$	programming pulse width per time	90	100	110	µs
Nprog	number of pulses for programming	–	5	–	–
$t_{acc(byte)}$	accumulated programming time per byte	450	500	550	µs
V_{PP}	programming voltage	12.50	12.75	13.00	V

21.3 AC characteristics of Programming mode

Table 90 Timing for programming Program EPROM and OSD EPROM; see Fig.48

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$t_{su(A)}$	address set-up time	2	–	–	µs
$t_{h(A)}$	address hold time	20	–	–	ns
$t_{su(D)}$	data set-up time	2	–	–	ns
$t_{h(D)}$	data hold time	20	–	–	ns
$t_{su(PV)}$	programming voltage set-up time	2	–	–	µs
$t_{W(P)}$	programming pulse width	90	100	110	µs
$t_{h(WE)}$	write enable hold time	110	–	–	ns
$t_{su(OE)}$	output enable set-up time	2	–	–	µs
$t_{ACC(OE)}$	output enable access verify	–	–	20	ns
$t_{su(CE)}$	chip enable set-up time	2	–	–	µs
t_{OZ}	output to high impedance verify	14	–	–	ns
$t_{W(OE)}$	output enable pulse width	300	–	–	ns



V_{IH} and V_{IL} are CMOS levels and are typically 5 V and 0 V respectively.
When $\overline{OE}$ is HIGH, P0.0 to P0.7 are used as inputs, when $\overline{OE}$ is LOW, P0.0 to P0.7 are used as outputs.
During programming the power supply must remain at 5 V. During verification the power supply must remain at 5.8 V.

Fig.48 Programming waveforms.

22 PINNING CHARACTERIZATION

This chapter describes every pin used in both the SDIP42 and PLCC68 packages.

22.1 Type of packages

SDIP42: for P8XCX66

PLCC68: for Metalink+ applications

Table 91 Explanation of symbols/terms used in Table 92

SYMBOL/TERM	MEANING
STr	Schmitt trigger
Rpu	pull-up resistor
Rpd	pull-down resistor
Z	high-impedance
original state	the outputs keep the state they had before entering the Idle mode

Table 92 Pin characteristics

PIN		SYMBOL	TYPE	INPUT LEVEL	OUTPUT TYPE	SLOPE CONTROL	OUTPUT IN IDLE MODE	OUTPUT AFTER RESET	ACTIVE STATE SW CONTROL
SDIP42	PLCC68								
–	1	V_{SS}	–	–	–	–	–	–	
–	2	INTD	I	CMOS + Rpu[1]	–	–	–	–	
1	3	P5.0	I/O	CMOS	open-drain	Yes	original state	Z[2]	
1	3	TPWM	O	–	push-pull	No	LOW	–	
2	4	P5.1	I/O	CMOS	open-drain	Yes	original state	Z[2]	
2	4	PWM0	O	–	open-drain	Yes	LOW	–	
3	5	P5.2	I/O	CMOS	open-drain	Yes	original state	Z[2]	
3	5	PWM1	O	–	open-drain	Yes	LOW	–	
4	6	P5.3	I/O	CMOS	open-drain	Yes	original state	Z[2]	
4	6	PWM2	O	–	open-drain	Yes	LOW	–	
5	7	P5.4	I/O	CMOS	open-drain	Yes	original state	Z[2]	
5	7	PWM3	O	–	open-drain	Yes	LOW	–	
6	8	P5.5	I/O	CMOS	open-drain	Yes	original state	Z[2]	
6	8	PWM4	O	–	open-drain	Yes	LOW	–	
–	9	n.c.	–	–	–	–	–	–	

PIN		SYMBOL	TYPE	INPUT LEVEL	OUTPUT TYPE	SLOPE CONTROL	OUTPUT IN IDLE MODE	OUTPUT AFTER RESET	ACTIVE STATE SW CONTROL
SDIP42	PLCC68								
–	10	n.c.	–	–	–	–	–	–	
7	11	P5.6	I/O	CMOS	open-drain	Yes	original state	Z[2]	
7	11	PWM5	O	–	open-drain	Yes	LOW	–	
8	12	P5.7	I/O	CMOS	open-drain	Yes	original state	Z[2]	
8	12	PWM6	O	–	open-drain	Yes	LOW	–	
9	13	P3.0	I/O	CMOS + Rpu[3]	open-drain	Yes	original state	Z[2]	
9	13	ADC0	I	analog	–	–	–	–	
–	14	PH1SEM	O	–	open-drain, 2 mA	note 4	–	–	
–	15	S1ESEM	O	–	open-drain, 2 mA	note 4	–	–	
10	16	P3.1	I/O	CMOS + Rpu[3]	open-drain	Yes	original state	Z[2]	
10	16	ADC1	I	analog	–	–	–	–	
–	17	P2.0	I/O	CMOS	open-drain + Rpu[5]	Yes	–	–	
11	18	P3.2	I/O	CMOS + Rpu[3]	open-drain	Yes	original state	Z[2]	
11	18	ADC2	I	analog	–	–	–	–	
–	19	P2.1	I/O	CMOS	open-drain + Rpu[5]	Yes	–	–	
12	20	P3.3	I/O	CMOS	open-drain	Yes	original state	Z[2]	
12	20	PWM7	O	–	open-drain	Yes	LOW	–	
–	21	P2.2	I/O	CMOS	open-drain + Rpu[5]	Yes	–	–	
–	22	P2.3	I/O	CMOS	open-drain + Rpu[5]	Yes	–	–	
13	23	P0.0	I/O	CMOS	open-drain	Yes	original state	Z[2]	
14	24	P0.1	I/O	CMOS	open-drain	Yes	original state	Z[2]	
15	25	P0.2	I/O	CMOS	open-drain	Yes	original state	Z[2]	
–	26	OSD_EPR_TST	–	–	–	–	–	–	
–	27	n.c.	–	–	–	–	–	–	
16	28	P0.3	I/O	CMOS	open-drain	Yes	original state	Z[2]	
17	29	P0.4	I/O	CMOS	open-drain	Yes	original state	Z[2]	
18	30	P0.5	I/O	CMOS	open-drain	Yes	original state	Z[2]	
19	31	P0.6	I/O	CMOS	open-drain	Yes	original state	Z[2]	
20	32	P0.7	I/O	CMOS	open-drain	Yes	original state	Z[2]	
–	33	V_{DDD}	–	–	–	–	–	–	
21	34	V_{SSD}	–	–	–	–	–	–	

PIN		SYMBOL	TYPE	INPUT LEVEL	OUTPUT TYPE	SLOPE CONTROL	OUTPUT IN IDLE MODE	OUTPUT AFTER RESET	ACTIVE STATE SW CONTROL
SDIP42	PLCC68								
–	35	P2.4	I/O	CMOS	open-drain + Rpu[5]	Yes	–	–	
–	36	P2.5	I/O	CMOS	open-drain + Rpu[5]	Yes	–	–	
22	37	B	O	–	push-pull, 1.6 mA	No	note 6	LOW[7]	SW con
23	38	G	O	–	push-pull, 1.6 mA	No	note 6	LOW[7]	SW con
24	39	R	O	–	push-pull, 1.6 mA	No	note 6	LOW[7]	SW con
25	40	FB	O	–	push-pull, 1.6 mA	No	note 6	LOW[7]	SW con
26	41	HSYNC	I	TTL STr	–	–	–	–	SW con
27	42	VSYNC	I	TTL STr	–	–	–	–	SW con
–	43	n.c.	–	–	–	–	–	–	
–	44	n.c.	–	–	–	–	–	–	
28	45	V_{DDA}	–	–	–	–	–	–	
29	46	V_{SS}	–	–	–	–	–	–	
–	47	P2.6	I/O	CMOS	open-drain + Rpu[5]	Yes	–	–	
30	48	V_{PP}	I	12.75 V	–	–	–	–	
–	49	V_{SS}	–	–	–	–	–	–	
31	50	XTALIN	I	CPU XTAL	–	–	–	–	
32	51	XTALOUT	O	CPU XTAL	–	–	–	–	
–	52	P2.7	I/O	CMOS	open-drain + Rpu[5]	Yes	–	–	
–	53	IDLPDEM	O	–	push-pull, 2 mA	note 4	–	–	
33	54	RESET	I	CMOS STr + Rpd[8]	–	–	–	–	
–	55	EMUPBX	O	–	push-pull, 2 mA	note 4	–	–	
–	56	V_{SS}	–	–	–	–	–	–	
34	–	V_{SS}	–	note 9	–	–	–	–	
34	57	P1.0	I/O	TTL STr	open-drain + Rpu[5]	Yes	original state	Z[2]	
34	57	V_{DD}	–	notes 9 and 10	–	–	–	–	
35	58	P1.1	I/O	TTL STr	open-drain	Yes	original state	Z[2]	
35	58	INT1	I	TTL STr	–	–	–	–	
36	59	P1.2	I/O	TTL STr	open-drain	Yes	original state	Z[2]	
36	59	T0	I	TTL STr	–	–	–	–	
–	60	n.c.	–	–	–	–	–	–	

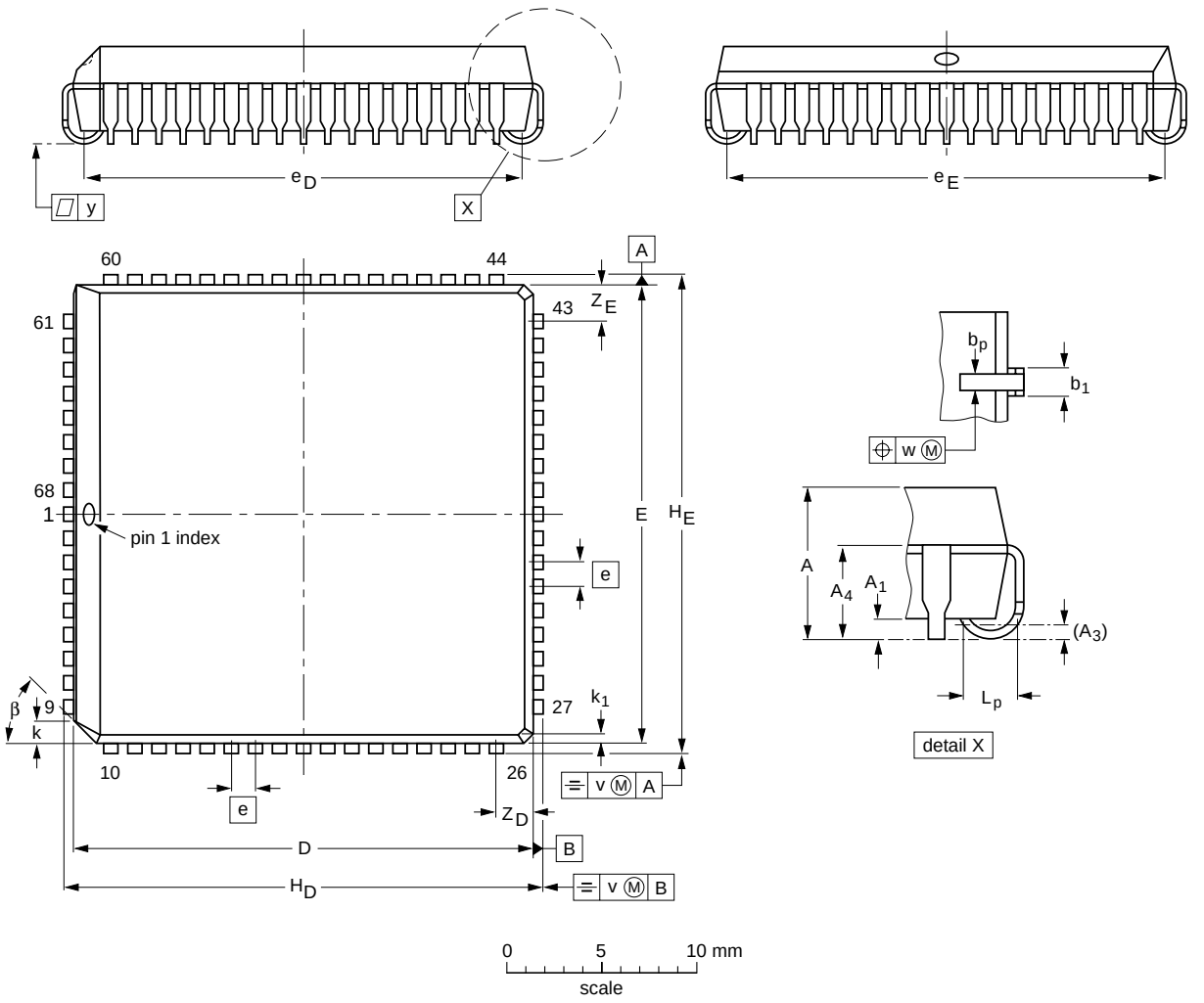
PIN		SYMBOL	TYPE	INPUT LEVEL	OUTPUT TYPE	SLOPE CONTROL	OUTPUT IN IDLE MODE	OUTPUT AFTER RESET	ACTIVE STATE SW CONTROL
SDIP42	PLCC68								
–	61	n.c.	–	–	–	–	–	–	
37	62	P1.3	I/O	TTL STr	open-drain	Yes	original state	Z(2)	
37	62	INT0	I	TTL STr	–	–	–	–	
38	63	P1.4	I/O	TTL STr	open-drain	Yes	original state	Z(2)	
38	63	T1	I	TTL STr	–	–	–	–	
39	64	P1.5	I/O	TTL STr	open-drain	Yes	original state	Z(2)	
39	64	SCL	I/O	TTL STr	open-drain	Yes	HIGH(11)	–	
40	65	P1.6	I/O	TTL STr	open-drain	Yes	original state	Z(2)	
40	65	SDA	I/O	TTL STr	open-drain	Yes	HIGH(11)	–	
41	66	P1.7	I/O	TTL STr	open-drain + Rpu(5)	Yes	original state	Z(2)	
41	–	V_{SS}	–	note 9	–	–	–	–	
–	67	V_{SS}	–	–	–	–	–	–	
42	68	V_{DD}	–	–	–	–	–	–	

Notes

1. A pull-up resistor must be present to prevent a floating input during normal/alternative mode when no external signal is applied to the pad. Pull-up = present internally.
2. All ports are in input mode after reset; that means the value at the pin is determined by the external circuitry: pull-up registers Rext (and/or external applied input).
3. A pull-up resistor must be present to prevent floating (digital) inputs if the pad is used for the analog inputs ADCO, ADCI and ADC2. This pull-up is also present if these pins are used as port function. Pull-up is internally.
4. These pins are standard I/O cells SPF20PGD (2 mA PP slew-rate controlled).
5. A pull-up resistor must be present to prevent a floating input during nominal/alternative mode when no external signal is applied to the pad. Pull-up = present internally.
6. Inverse of the Bp bit (located in OSCON).
7. After reset the Bp bit (located in OSCON) = 1, therefore output becomes LOW.
8. Its pull-down resistor is present internally (see Section 13.2).
9. For the SDIP42 package, pin P1.0 can be exchanged for a V_{SS} or V_{DD}, pin P1.7 for a V_{SS}.
10. For the PLCC68 package, pin P1.0 can be exchanged for a V_{DD} line.
11. Output is HIGH via external resistor.

23 PACKAGE OUTLINES

PLCC68: plastic leaded chip carrier; 68 leads **SOT188-2**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

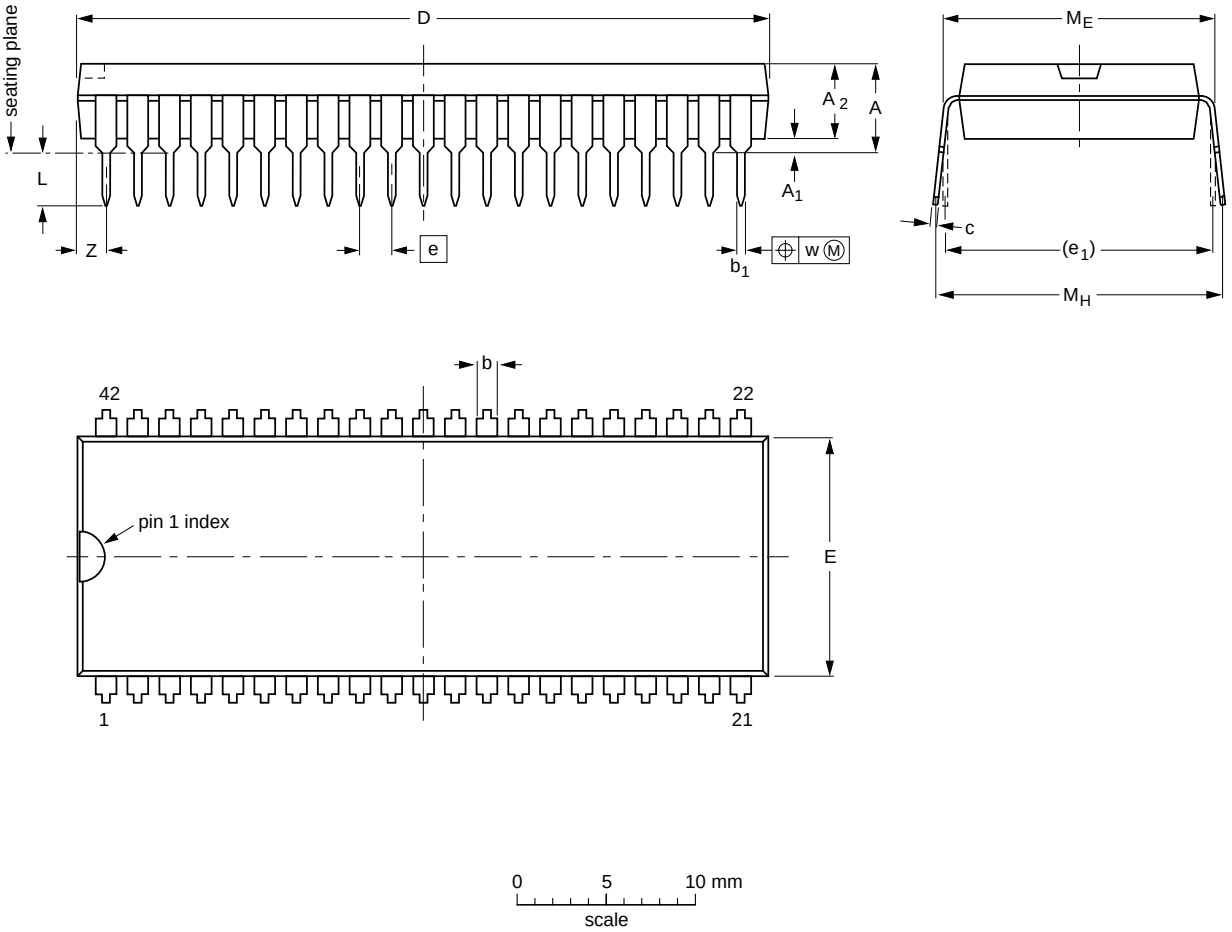
UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.30	0.53 0.33	0.81 0.66	24.33 24.13	24.33 24.13	1.27	23.62 22.61	23.62 22.61	25.27 25.02	25.27 25.02	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.13	0.021 0.013	0.032 0.026	0.958 0.950	0.958 0.950	0.05	0.930 0.890	0.930 0.890	0.995 0.985	0.995 0.985	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT188-2	112E10	MO-047AC				~~92-11-17~~ 95-03-11

SDIP42: plastic shrink dual in-line package; 42 leads (600 mil) **SOT270-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.08	0.51	4.0	1.3 0.8	0.53 0.40	0.32 0.23	38.9 38.4	14.0 13.7	1.778	15.24	3.2 2.9	15.80 15.24	17.15 15.90	0.18	1.73

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT270-1						~~90-02-13~~ 95-02-04

24 SOLDERING

24.1 Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

24.2 Through-hole mount packages

24.2.1 SOLDERING BY DIPPING OR BY SOLDER WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

24.2.2 MANUAL SOLDERING

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

24.3 Surface mount packages

24.3.1 REFLOW SOLDERING

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

24.3.2 WAVE SOLDERING

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

24.3.3 MANUAL SOLDERING

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

24.4 Suitability of IC packages for wave, reflow and dipping soldering methods

MOUNTING	PACKAGE	SOLDERING METHOD		
		WAVE	REFLOW(1)	DIPPING
Through-hole mount	DBS, DIP, HDIP, SDIP, SIL	suitable(2)	–	suitable
Surface mount	BGA, SQFP	not suitable	suitable	–
	HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable(3)	suitable	–
	PLCC(4), SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended(4)(5)	suitable	–
	SSOP, TSSOP, VSO	not recommended(6)	suitable	–

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
3. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

25 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

26 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

27 PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

NOTES

NOTES

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