DATA SHEET

P8xCL883; P8xCL884
TELX microcontrollers for CT0 handset/basestation applications

Product specification
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CONTENTS

TELX microcontrollers for CT0 handset/basestation applications

P8xCL883; P8xCL884

1 FEATURES

- Full static 80C51 CPU; enhanced 8-bit architecture with:
  - Minimum 6 cycles per instruction (twice as fast as a standard 80C51 core)
  - Non-page oriented instructions
  - Direct addressing
  - Four 8-byte RAM register banks
  - Stack depth limited only by available internal RAM (maximum 256 bytes)
  - Multiply, divide, subtract and compare instructions.
- 8-bit ports:
  - P8xCL883: 3 (19 I/O lines)
  - P8xCL884: 3 (18 I/O lines).
- Program Memory:
  - P8xCL883/P8xCL884: 8-kbyte One Time Programmable (OTP).
- 256-byte RAM
- 128-byte EEPROM Data Memory, accessed internally via I^{2}C-bus interface (P8xCL884 only)
- Amplitude Controlled Oscillator (ACO) suitable for quartz crystal or ceramic resonator
- Improved Power-on/Power-off reset (POR) circuitry
- Low Voltage Detection (LVD) with 11 software programmable levels
- Eight interrupts on Port 1:
  - Edge or level sensitive triggering selectable via software
  - Power-saving use for keyboard control.
- Twenty source, twenty vector interrupt structure with two priority levels
- Wake-up from Power-down mode via LVD or external interrupts at Port 1
- DTMF generator (P8xCL884 only)
- MSK modem including Manchester encoder/decoder with 2 digital outputs for analog cordless telephones (standards CT0/CT1/CT1+)
- Two standard 16-bit timer/event counters
- Additional 16-bit timer/event counter with Capture, Compare and Auto-reload function
- Watchdog Timer
- Full duplex enhanced UART with double buffering
- I^{2}C-bus interface for serial transfer on two lines, maximum 400 kHz
- Very low current consumption
- Single supply voltage: 2.7 to 3.6 V
- Frequency: 3.58 MHz
- Operating temperature: –25 to +70°C
- 28 pin SO package.

2 GENERAL DESCRIPTION

The P8xCL883/P8xCL884 are manufactured in an advanced CMOS technology. The P8xCL883 is based on single-chip technology and the P8xCL884 is based on MCM (Multi-Chip-Module) technology as the EEPROM is integrated on a separate chip.

The P8xCL883/P8xCL884 are 8-bit microcontrollers especially suited for low cost analog cordless telephone applications (CT0, CT1, CT1+ standards). For this purpose, features like DTMF, EEPROM, MSK modem and POR/LVD are integrated on-chip.

The device is optimized for low power consumption. The P8xCL883/P8xCL884 have two software selectable features for power reduction: Idle and Power-down modes. In addition, all derivative blocks can switch off their clock if they are inactive.

The instruction set of the P8xCL883/P8xCL884 is based on that of the 80C51. The P8xCL883/P8xCL884 also function as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 46 two-byte, and 16 three-byte. Due to the missing port P2, there is no external data or memory access and the MOVX operations cannot be used.

This data sheet details the specific properties of the P8xCL883/P8xCL884; for details of the P8xCL883/P8xCL884 core and the derivative functions see the *"TELX family"* data sheet and *"Data Handbook IC20; 80C51-based 8-bit Microcontrollers"*.

3 ORDERING INFORMATION

TYPE NUMBER	OTP TYPE	PACKAGE		
		NAME	DESCRIPTION	VERSION
P87CL883T/000	Blank OTP	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
P87CL884T/000				
P87CL883T/xxx	Factory-programmed OTP			
P87CL884T/xxx				
P83CL883T/xxx	Pre-programmed OTP			
P83CL884T/xxx				

4 BLOCK DIAGRAM

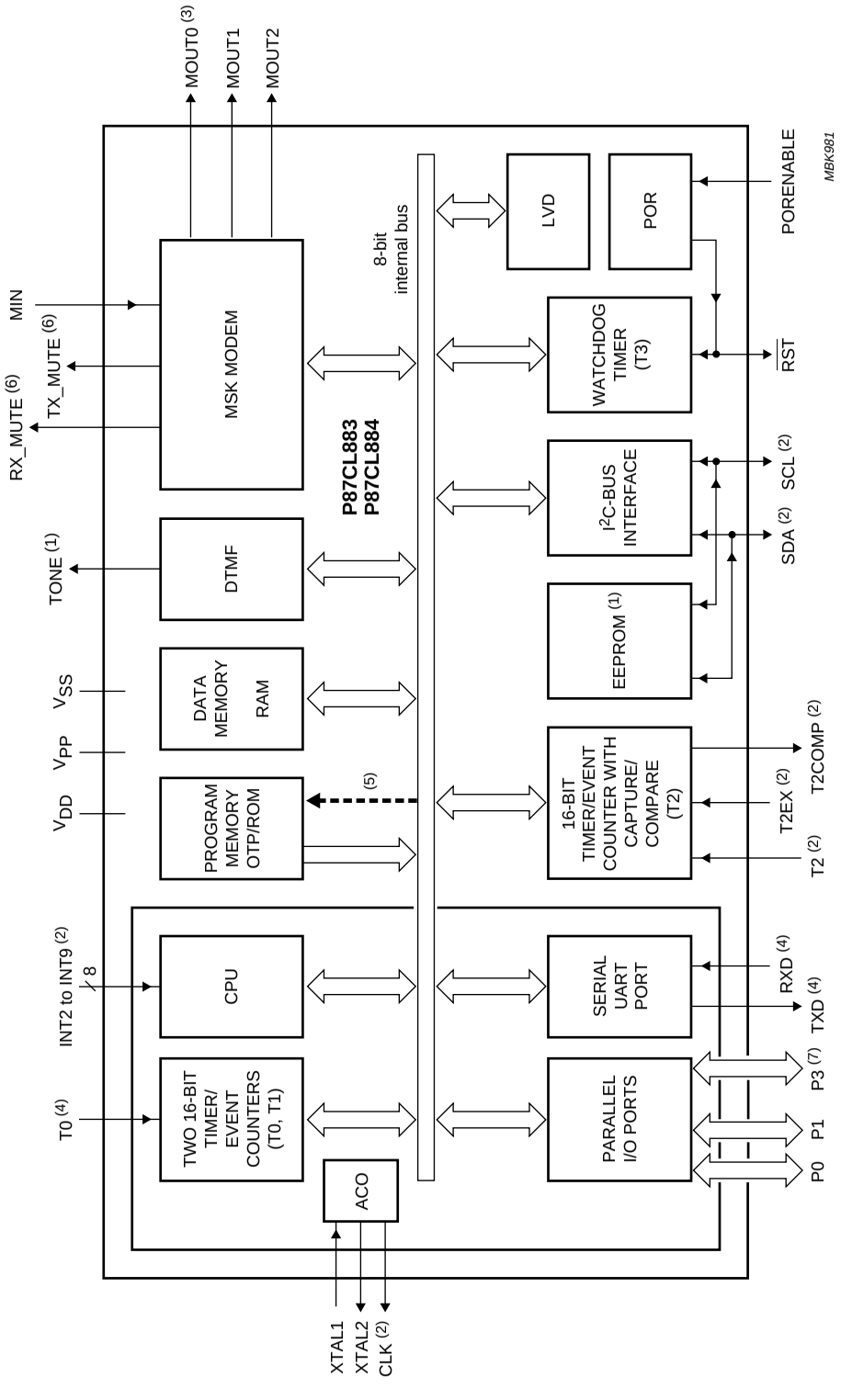
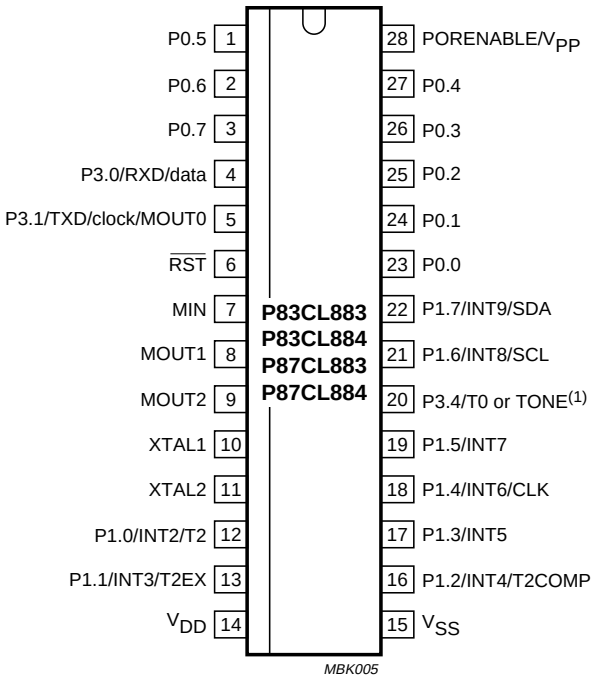


Fig.1 Block diagram.

(1) Only available on the P8xCL884.
(2) Alternative functions of Port 1.
(3) MOUT0 is the alternative function of P3.1.
(4) Alternative functions of Port 3; T0 is only available on the P8xCL883.
(5) In-circuit OTP programming.
(6) By software, any I/O pin can be used.
(7) Port 3: P3.0, P3.1 and P3.4; P3.4 is only available on the P8xCL883.

5 PINNING INFORMATION

5.1 Pinning



(1) **Pin 20**: P3.4/T0 on the P8xCL883; TONE on the P8xCL884.

Fig.2 Pin configuration.

5.2 Pin description

SYMBOL	PIN	DESCRIPTION
$\overline{RST}$	6	**Active LOW reset.** A LOW level on this pin for two machine cycles while the oscillator is running, resets the device. The $\overline{RST}$ pin is also an output which can be used to reset other ICs.
MIN	7	Digital **MSK** modem input.
MOUT1	8	Digital **MSK** modem outputs.
MOUT2	9	
XTAL1	10	**Crystal input.** Input to the Amplitude Controlled Oscillator. Also the input for an externally generated clock source.
XTAL2	11	**Crystal output.** Output of the Amplitude Controlled Oscillator. To be left unconnected when an external oscillator clock is used.
V_{DD}	14	Power supply.
V_{SS}	15	Ground.
P0.0 to P0.7	23 to 27, 1 to 3	**Port 0.** 8-bit bidirectional I/O port. Every port pin can be used as open-drain, standard port, high-impedance input or push-pull output, according to Section 6.2.
P1.0/INT2/T2	12	**Port 1**. 8-bit bidirectional I/O port with alternative functions. Every port pin except P1.6 and P1.7 (I^2C-bus pins) can be used as open-drain, standard port, high-impedance input or push-pull output, according to Section 6.2. Port P1.3 has LED drive capability. Port 1 also serves the alternative functions: **INT2 to INT9** interrupts; Timer T2 external inputs **T2** and **T2EX**; Timer T2 compare output **T2COMP**; external clock output **CLK**; I^2C-bus clock **SCL** and data in/outputs **SDA**.
P1.1/INT3/T2EX	13	
P1.2/INT4/T2COMP	16	
P1.3/INT5	17	
P1.4/INT6/CLK	18	
P1.5/INT7	19	
P1.6/INT8/SCL	21	
P1.7/INT9/SDA	22	
P3.0/RXD/data	4	**Port 3.** 3 or 2-bit bidirectional I/O port with alternative functions. Every port pin can be used as open-drain, standard port, high-impedance input or push-pull output, according to Chapter 6.2. Port 3 also serves the alternative functions: **RXD/data** is the serial port receiver data input (asynchronous) or data I/O (synchronous); **TXD/clock** is the serial port transmitter data output (asynchronous) or clock output (synchronous) or digital MSK modem output **MOUT0**; **T0** is an external input for Timer 0. **P3.4/T0** is only available on the P8xCL883.
P3.1/TXD/clock/ MOUT0	5	
P3.4/T0	20	
TONE	20	**DTMF** output; **TONE** is only available on the P8xCL884.
PORENABLE/V_{PP}	28	**PORENABLE**. Power-on reset circuit enable. If PORENABLE = 1, the internal Power-on reset circuit is enabled. If external reset circuitry is used, it is recommended to keep PORENABLE = 0 to reach lowest power consumption. This pin is also used for the OTP programming voltage V_{PP}.

6 FUNCTIONAL DESCRIPTION

6.1 Special Function Registers (SFRs)

Table 1 List of SFRs

REGISTER	ADDRESS (HEX)	RESET VALUE(1)
80C51 core		
ACC	E0	0000 0000
B	F0	0000 0000
DPL	82	0000 0000
DPH	83	0000 0000
PCH	no SFR	0000 0000
PCL	no SFR	0000 0000
PCON	87	0000 0000
PRESC	F3	0000 0000
PSW	D0	0000 0000
SP	81	0000 0111
T0/T1		
TCON	88	0000 0000
TH0	8C	0000 0000
TH1	8D	0000 0000
TL0	8A	0000 0000
TL1	8B	0000 0000
TMOD	89	0000 0000
Port		
ALTP	A3	0000 0000
P0	80	1111 1111
P0CFGA	8E	1111 1111
P0CFGB	8F	0000 0000
P1	90	1111 1111
P1CFGA	9E	0011 1111
P1CFGB	9F	0000 0000
P3	B0	XXX1 XX11
P3CFGA	BE	XXX1 XX11
P3CFGB	BF	XXX0 XX00
P4	C1	XXXX XXX0
TIMER2		
COMP2H	AB	0000 0000
COMP2L	AA	0000 0000
RCAP2H	CB	0000 0000
RCAP2L	CA	0000 0000
T2CON	C8	0000 0000
TH2	CD	0000 0000
TL2	CC	0000 0000
EEPROM interface		
EECON	FB	0000 0000
DTMF		
HGF	A2	0000 0000
LGF	A1	0000 0000
Interrupt logic		
IEN0	A8	0000 0000
IEN1	E8	0000 0000
IEN2	F1	0000 0000
IP0	B8	0000 0000
IP1	F8	0000 0000
IP2	F9	0000 0000
ISE1	E1	0000 0000
IX1	E9	0000 0000
IRQ1	C0	0000 0000
LVD		
LVDCON	F2	0000 0000
POR/ACO		
RSTAT	E6	XXX0 1000
MSK		
MCON	D3	0000 0000
MBUF	D1	XXXX XXXX
MSTAT	D2	XX00 0000
UART		
S0BUF	99	0000 0000
S0CON	98	0000 0000
I^2C-bus interface		
S1ADR	DB	0000 0000
S1CON	D8	0000 0000
S1DAT	DA	0000 0000
S1STA	D9	1111 1000

REGISTER	ADDRESS (HEX)	RESET VALUE(1)
WDT		
WDCON	A5	1010 0101
WDTIM	FF	0000 0000
OTP interface		
OAH	D5	X00X XXXX
OAL	D4	XXXX XXXX
ODATA	D6	XXXX XXXX
OISYS	DC	000X 0000
OTEST	D7	0000 0000
Reserved locations; do not write		
reserved	E7, FD	–

Note

1. Where: X = undefined state or not implemented bit.

6.2 I/O facilities

6.2.1 PORTS

The P8xCL883/P8xCL884 have 19 and 18 I/O lines respectively, treated as 19 and 18 individually addressable bits or as three parallel 8-bit addressable ports.
The alternative functions are detailed below:

Port 0 Offers no alternative functions.

Port 1 Used for a number of special functions:

- P1.0 to P1.7 provides the inputs for the external interrupts INT2 to INT9
- P1.2/T2COMP for external activation and Compare/Auto-reload output function of Timer 2
- P1.4/CLK for the clock output
- P1.6/SCL and P1.7/SDA for the I^2C-bus interface are real open-drain outputs or high-impedance; no other port configurations are available.

Port 2 Not available.

Port 3 Pins can be configured individually to provide:

- P3.0/RXD/data and P3.1/TXD/clock/MOUT0 which are serial port receiver input and transmitter output (UART)
- P3.4/T0 as counter input; available only in P8xCL883.

To enable a Port pin alternative function, the Port bit latch in its SFR must contain a logic 1.

Each port consists of a latch (Special Function Registers P0 to P3), an output driver and input buffer. All ports have internal pull-ups. Figure 3b shows that the strong transistor ‘p1’ is turned on for only one oscillator period after a LOW-to-HIGH transition in the port latch. When on, it turns on ‘p3’ (a weak pull-up) through the inverter IN1. This inverter and transistor ‘p3’ form a latch which holds the logic 1.

Port P1.3 has LED drive capability.

6.2.2 PORT I/O CONFIGURATION

I/O port output configurations are determined by the settings in port configuration SFRs. There are 2 SFRs for each port: PnCFGA and PnCFGB, where ‘n’ indicates the specific port number (0to 3). One bit in each of the 2SFRs relates to the output setting for the corresponding port pin, allowing any combination of the 2output types to be mixed on those port pins. For example, the output type of P1.3, is controlled by the setting of bit 3 in the SFRs P1CFGA and P1CFGB.

The port pins may be individually configured via SFRs with one of the following modes (P1.6 and P1.7 can be open-drain or high-impedance but never have any diodes against V_{DD}). These modes are also shown in Fig.3.

Mode 0 Open-drain; quasi-bidirectional I/O with n-channel open-drain output. Use as an output requires the connection of an external pull-up resistor; e.g. Port 0 for external memory accesses (EA = 0) or access above the built-in memory boundary. The ESD protection diodes against V_{DD} and V_{SS} are still present; seeFig.3b. Except for the I^2C-bus pins P1.6 and P1.7, ports which are configured as open-drain still have a protection diode to V_{DD}.

Mode 1 Standard port; quasi-bidirectional I/O with pull-up. The strong pull-up ‘p1’ is turned on for only two oscillator periods after a LOW-to-HIGH transition in the port latch. After these two oscillator periods the port is only weakly driven through ‘p2’ and ‘very weakly’ driven through ‘p3’ (see Fig.3b).

Mode 2 High-impedance; this mode turns off all output drivers on a port. Thus, the pin will not source or sink current and may be used as an input-only pin with no internal drivers for an external device to overcome (see Fig.3c).

Mode 3 Push-pull; output with drive capability in both polarities. Under this mode, pins can only be used as outputs (see Fig.3d).

Tables 2 and 3 show the configuration register settings for the 4 port output types.

The electrical characteristics of each output type can be found in Chapter 8. The default port configuration after reset is given in Table 3.

Table 2 Port Configuration Registers PnCFGA and PnCFGB (n = 0 to 3) settings

MODE(1)	PnCFGA	PnCFGB	PORT OUTPUT MODE	
			NORMAL PORTS	I^2C-BUS PORTS (P1.6 AND P1.7)
Mode 0	0	0	open-drain	open-drain
Mode 1	1	0	quasi-bidirectional	open-drain
Mode 2	0	1	high-impedance	high-impedance
Mode 3	1	1	push-pull	open-drain

Note

1. Mode changes may cause glitches to occur during transitions. When modifying both registers, WRITE instructions should be carried out consecutively.

Table 3 Special Function Registers for port configurations/data

REGISTER NAME	REGISTER MNEMONIC	SFR ADDRESS (HEX)	STATE AFTER RESET
Port P0 output data(1)	P0	80	1111 1111
Port P0 configuration A	P0CFGA	8E	1111 1111
Port P0 configuration B	P0CFGB	8F	0000 0000
Port P1 output data(1)	P1	90	1111 1111
Port P1 configuration A	P1CFGA	9E	0011 1111
Port P1 configuration B	P1CFGB	9F	0000 0000
Port P3 output data(1)	P3	B0	XXX1 XX11(2)
Port P3 configuration A	P3CFGA	BE	XXX1 XX11(2)
Port P3 configuration B	P3CFGB	BF	XXX0 XX00(2)

Notes

1. This means that P0, P1.0 to P1.5 and P3 are initialized in Mode1 (quasi-bidirectional, driving a weak HIGH) and the I^2C-bus ports P1.6 and P1.7 are initialized in Mode 0 (open-drain, not driven).
2. Port pin P3.4 is only available on P8xCL883.

6.2.3 Alternative Port Function Register (ALTP)

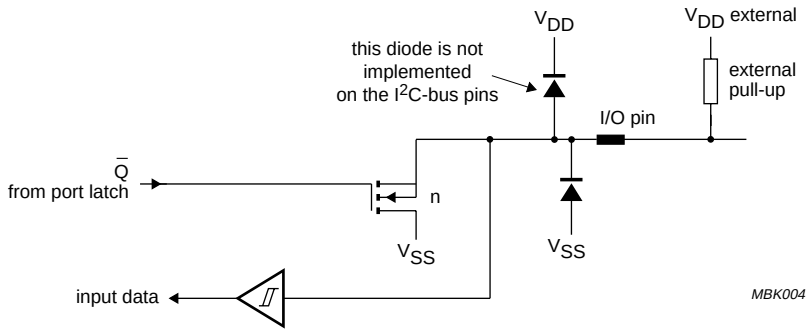
This 4-bit register selects the alternative function of certain port pins.

Table 4 Alternative Port Function Register (SFR address A3H)

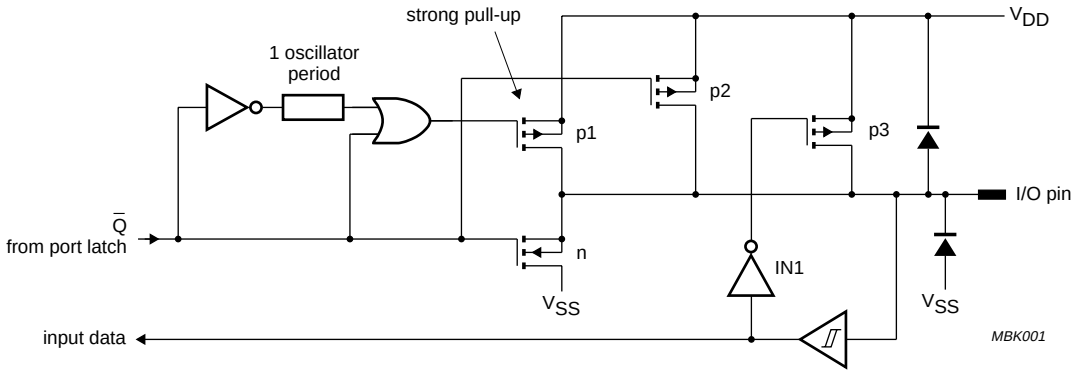
76543210							
————				EMOUT0	ECLK	EMLDY	ETONE

Table 5 Description of ALTP bits

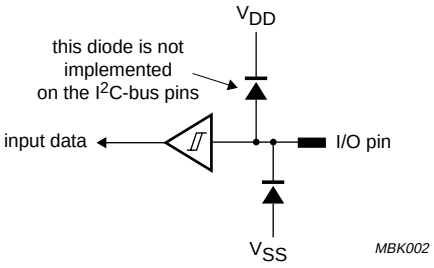
BIT	SYMBOL	DESCRIPTION
7t o4	–	These 4 bits are reserved.
3	EMOUT0	If this bit is set, P3.1 will output the MOUT0 signal.
2	ECLK	If this bit is set, P1.4 is configured to be push-pull, and P1.4 will output the system clock.
1	EMLDY	If this bit is set, P1.5 is configured to be push-pull, and P1.5 will output the digital MLDY signal of the DTMF generator.
0	ETONE	If this bit is set, the TONE output of the DTMF generator is enabled.



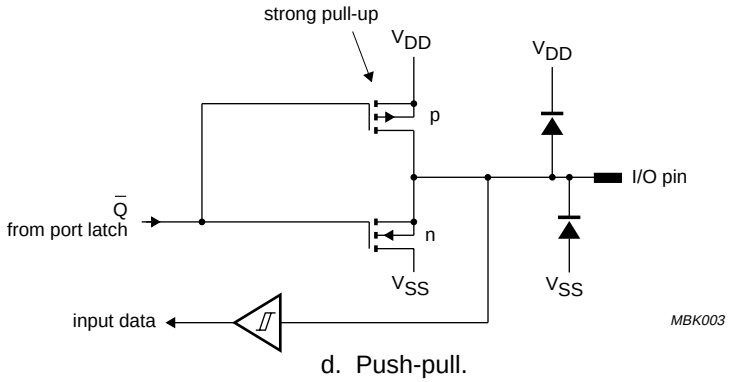
a. Open-drain.



b. Standard/quasi-bidirectional.



c. High-impedance.



d. Push-pull.

Fig.3 Port configuration options.

6.3 Timer/event counters

The P8xCL883/P8xCL884 contain three 16-bit timer/event counters: Timer 0, Timer 1 and Timer 2 which can perform the following functions:

- Measure time intervals and pulse durations
- Count events
- Generate interrupt requests
- Generate output on comparator match.

In the 'timer' mode the register is incremented every machine cycle.

Since a machine cycle consists of minimum 6 oscillator periods, the maximum count rate is $\frac{1}{6}f_{osc}$.

In the 'counter' mode, the register is incremented in response to a HIGH-to-LOW transition. Since it takes one machine cycle (minimum 6 oscillator periods) to recognize a HIGH-to-LOW transition, the maximum count rate is $\frac{1}{6}f_{osc}$. To ensure a given level is sampled, it should be held for at least one complete machine cycle.

Timer 0 and Timer 1 can be programmed independently to operate in four modes:

Mode 0 8-bit timer or 8-bit counter each with divide-by-32 prescaler.

Mode 1 16-bit time-interval or event counter.

Mode 2 8-bit time-interval or event counter with automatic reload upon overflow.

Mode 3 Timer 0 establishes TL0 and TH0 as two separate counters.

Note that the T0 input is only available on P8xCL883.

6.3.1 TIMER T2

Note that the timer T2 of the P8xCL883/P8xCL884 deviates from the timer T2 described in the *"TELX family"* data sheet.

Timer T2 is a 16-bit timer/counter that can operate either as a timer or as an event counter. These functions are selected by the state of the C/$\overline{T2}$ bit in the T2CON register. Five operating modes are available:

- Capture
- Compare
- Auto-reload
- Compare with Auto-reload
- Capture and Compare.

These modes are selected via the T2CON register.

6.3.1.1 Capture mode

In the Capture mode, two options may be selected by the EXEN2 bit in T2CON:

- If EXEN2 = 0, then Timer 2 is a 16-bit timer or counter which upon overflowing sets the Timer 2 overflow bit TF2, this may then be used to generate an interrupt.
- If EXEN2 = 1, Timer 2 operates as described above but with the additional feature that a HIGH-to-LOW transition at external input T2EX causes the current value in TL2 and TH2 to be captured into registers RCAP2L and RCAP2H respectively. In addition, the transition at T2EX causes the EXF2 bit in T2CON to be set; this may also be used to generate an interrupt.

The Capture mode is shown in Fig.4.

6.3.1.2 Compare mode

In the Compare mode, each time timerT2 is incremented, the contents of the compare registers COMP2H and COMP2L is compared with the new counter value of timer T2. When a match occurs, the interrupt flag COMP in register T2CON and port bit P1.2 are toggled. The 16-bit value held in these registers is preset by software. The first toggle after a chip reset will set the flag COMP.
The Compare mode is shown in Fig.4.

6.3.1.3 Auto-reload mode

In the Auto-reload mode there are also two options selected by the EXEN2 bit in T2CON:

- If EXEN2 = 0, then when Timer 2 rolls over, it sets the TF2 bit but also causes the Timer 2 registers to be reloaded with the 16-bit value held in registers RCAP2L and RCAP2H. The 16-bit value held in these registers is preset by software.
- If EXEN2 = 1, Timer 2 operates as described above but with the additional feature that a HIGH-to-LOW transition at external input T2EX will also trigger the 16-bit reload and set the EXF2 bit.

6.3.1.4 Compare with Auto-reload mode

The Auto-reload mode can also be used together with the Compare mode. The Auto-reload modes are shown in Fig.5.

6.3.1.5 Capture and Compare modes

The Capture and the Compare mode of timer T2 can be used separately or simultaneously. The function is chosen via the bits ECOMP, CP/$\overline{RL2}$ and TR2 in register T2CON.

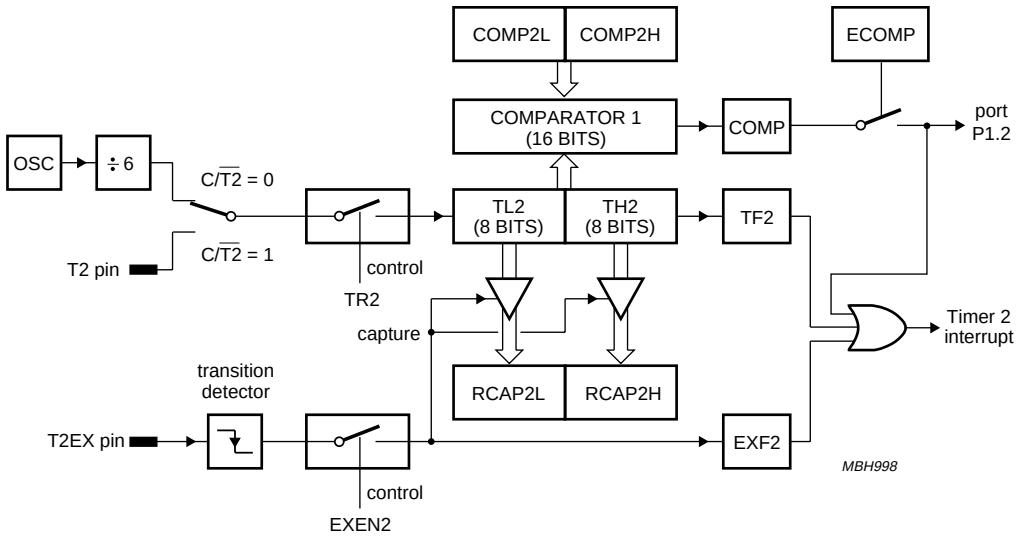


Fig.4 Timer 2 in Capture and/or Compare mode.

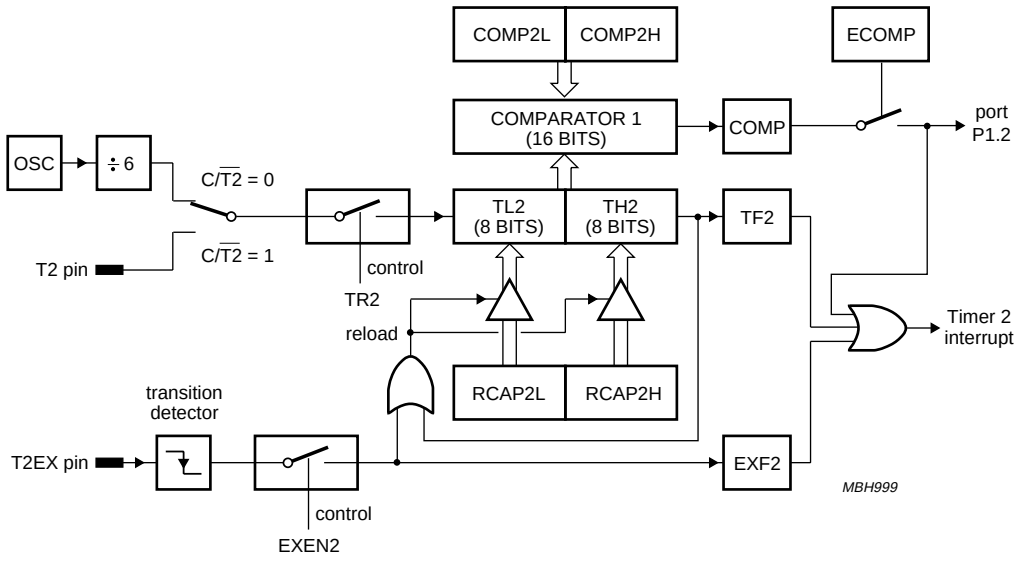


Fig.5 Timer 2 in Auto-Reload with/without Compare mode.

6.3.2 TIMER/COUNTER 2C ONTROL REGISTER (T2CON)

Table 6 Timer/Counter 2 Control Register (SFR address C8H)

76543210							
TF2	EXF2	COMP	ECOMP	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

Table 7 Description of T2CON bits

BIT	SYMBOL	DESCRIPTION
7	TF2	**Timer 2 overflow flag.** TF2 is set by a Timer 2 overflow and must be cleared by software.
6	EXF2	**Timer 2 external flag.** EXF2 is set when either a capture or reload is caused by a negative transition on T2EX and when EXEN2 = 1. When Timer T2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to Timer 2 interrupt routine. EXF2 must be cleared by software.
5	COMP	**Interrupt flag**. When a match between the 16-bit compare register (COMP2L and COMP2H) and the new counter value of timer T2 occurs, the interrupt flag COMP in register T2CON and port bit P1.2 are toggled.
4	ECOMP	**Enable compare output bit.** When set by software, the controller toggles port bit P1.2 (T2COMP) when a compare match occurs.
3	EXEN2	**Timer 2 external enable flag.** When set, allows a capture or reload to occur as a result of a negative transition on T2EX. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
2	TR2	**Timer 2 start/stop control.** Control bit for Timer 2.
1	C/$\overline{T2}$	**Timer 2 timer or counter select.** C/$\overline{T2}$ = 0 selects the internal timer with a clock frequency of $\frac{1}{6}f_{osc}$. C/$\overline{T2}$ = 1 selects the external event counter; negative edge-triggered.
0	CP/$\overline{RL2}$	**Capture/reload flag.** When set captures will occur on negative transitions at T2EX, if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1.

Table 8 Timer 2 operating modes

ECOMP	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	0	1	16-bit Compare
1	1	1	16-bit Capture and Compare
1	0	0	16-bit Compare with Auto-reload
0	0	0	off

6.4 MSK modem

For the P8xCL883/P8xCL884, MIN is no longer the alternative function of P4.0, but MIN is a separate pin. The polarity of MIN can however still be programmed with the P4.0 bit. P4.0 is a data SFR but no port logic is connected.

Only the most significant bits of MOUT, i.e. MOUT2 and MOUT1 are directly available as separate pins. In order to be able to further increase the signal quality, the MOUT0 signal is available as an alternative port function of P3.1.

For controlling this alternative port function the EMOUT0 bit has been added to the Alternative Port Function Register (ALTP); see Section 6.2.3.

6.5 Watchdog Timer

The Watchdog Timer differs from the description in the *"TELX family"* data sheet in that the external $\overline{EW}$ pin does not exist on the P8xCL883/P8xCL884.

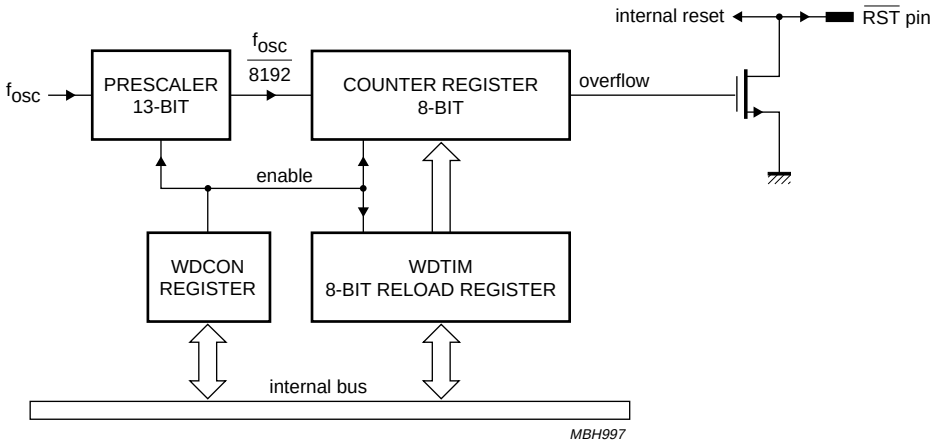


Fig.6 Functional diagram of the Watchdog Timer (T3).

6.6 OTP programming

6.6.1 OTP PROGRAMMING BY A PROGRAMMER

The 8 kbytes One Time Programmable (OTP) memory can be programmed by using a programmer (OM4260) together with a programmer adapter OM5508. Since the memory is programmable only once, programming an already programmed address results in a logical AND of the old and new code. The OTP code can be read out by the programmer for verification.

6.6.1.1 Signature bytes

The OTP memory contains three signature bytes which can be read by the programmer to identify the device. A special address space has been used for these bytes which does not influence the user address space.

The values of the signature bytes are:

(030H) = 15H, indicates manufactured by Philips Semiconductors

(031H) = C5H, indicates P8xCL883/P8xCL884

(060H) = 00H, currently not used.

6.6.2 IN-SYSTEM PROGRAMMING MODE

In the In-System Programming mode the OTP can be programmed under control of the CPU. A program to control programming has to be available in the OTP. This mode can be used to program several bytes in the OTP if the chip is already in a system e.g. to store tuning parameters.

In the In-System Programming mode the complete address space OTP can be programmed.

The user should take care not to overwrite the existing code.

For In-System Programming four SFRs are used to control the OTP.

Table 9 SFRs for In-System Programming

SFR NAME	DESCRIPTION
OAH	OTP Address High Register
OAL	OTP Address Low Register
ODATA	OTP Data Register
OISYS	OTP In-System Register

6.6.2.1 OTP In-System Programming Register (OISYS)

The OISYS SFR controls the In-System Programming mode. The data that has to be programmed is stored in the SFR ODATA and the address for this data is held in the SFRs OAH and OAL.

Table 10 OTP In-System Programming Register (SFR address DCH)

7	6	5	4	3	2	1	0
–––			VPon	SEC	SIG	WE	InSysMode

Table 11 Description of OISYS bits

BIT	SYMBOL	DESCRIPTION
7t o5	–	These bits are reserved.
4	VPon	V_{PP} status (read only).
3	–	This bit is reserved.
2	SIG	Signature bytes enable.
1	WE	Write Enable, enables programming.
0	InSysMode	In-System Programming status bit.

6.6.2.2 Mode entry

The In-System Programming mode is entered by setting the InSysMode bit of the OISYS SFR. The I^2C-bus is used for data transfer in this mode. If the I^2C-bus interface is addressed by an external master, the interface generates an interrupt request. The interrupt handler can now read the OISYS SFR and determine the status of the external high voltage (VPon). If high voltage is not present the interrupt is a standard I^2C-bus interrupt.

If high voltage is present the In-System Program interrupt routine has to start that writes the InSysMode bit (OISYS.0) and controls the address and data transfer.

This paragraph is valid for version 2 ('2' ending on type number). During In-System Programming the OTP memory must be in the DC read mode. This is achieved by writing 08H to the OTEST SFR. If the In-System Programming mode is left, 00H must be written into the OTEST SRF.

The program voltage must be available and stable for at least 10 μs before the mode is entered and has to be stable until the circuit has left the In-System Programming mode. The high voltage can be applied for maximum 60 seconds during the complete lifetime of the circuit.

6.6.2.3 Program cycle

The data and address must be supplied to the microcontroller and the control program must write to the SFRs: ODATA, OAH and OAL. A timer has to be initialized for a 100 μs cycle and the WE bit of the OISYS SFR must be set. Now the core has to be set into Idle mode. As long as the circuit is in idle mode a programming pulse is applied. After the interrupt request of the timer the OTP is available for normal code fetching.

The address applied to the OAH and OAL SFRs must be in the 8 kbytes address space.

6.6.2.4 Verify for In-System Programming

Verify is done in similar way as programming. The circuit is put into Idle mode and at the start of this mode the sense amplifiers are switched to verify mode and a read cycle is started. The timer must be initialized for a cycle of at least 1 μs. The address is supplied by the SFRs OAH and OAL. The WE bit of the OISYS SFR has to be reset. The OTP output data is latched in the ODATA SFR. After Idle mode is finished this SFR can be read in a normal way.
To ensure that the verified data is written into the SFR it is advised to write FFH into the ODATA SFR before a verify is started.

6.6.2.5 Signature bytes

The signature bytes can be read by setting the SIG bit of the OISYS SFR and applying the address of the signature byte. Applying a write pulse while the SIG bit of the OISYS SFR is HIGH is forbidden although the contents of the signature bytes will never be destroyed.

6.6.2.6 How to connect the PORENABLE/V_{PP} pin in the In-System Programming mode

If the V_{PP} pin is dual-mode (e.g. PORENABLE/V_{PP}), ICs connected to the signal PORENABLE **must be able to withstand up to 13V**, i.e. cannot have clamping diodes or low break-down voltages. If the pin is connected to a fixed voltage (V_{DD} or V_{SS}) there must be a way of switching-off this connection on the PCB. One possible implementation is presented in Fig.7 where POR is enabled in normal mode of operation (pin PORENABLE/V_{PP} = 1 by the pull-up), the V_{PP} source must supply enough current in R_p in order to guarantee a minimum 12.5 V on the PORENABLE/V_{PP} pin.

Note that if in the application the Power-on reset is disabled (pin PORENABLE/V_{PP} = 0), applying a high voltage to the PORENABLE/V_{PP} pin will also enable the POR circuit. This will cause a reset independent of the actual V_{DD} value.

6.7 Oscillator circuitry

General information on the oscillator circuitry can be found in the *"TELX family"* data sheet.

6.7.1 Resonator requirements

For correct function of the oscillator, the values of R_1 and C_0 of the chosen resonator (quartz or PXE) must be below the line shown in Fig.8a. The value of the parallel resistor R_0 must be less than 47 kΩ.

The wiring between chip and resonator should be kept as short as possible.

6.7.2 Recommended resonator types

- CSA 3.58MG (supplier Murata)
- FCR3.58M5 (supplier TDK).

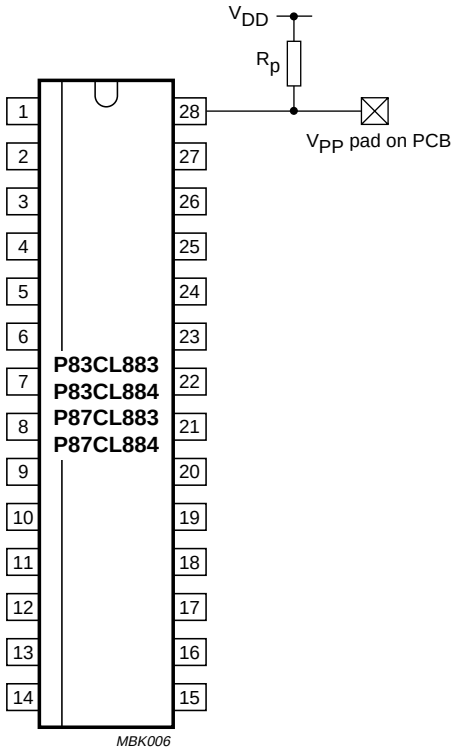
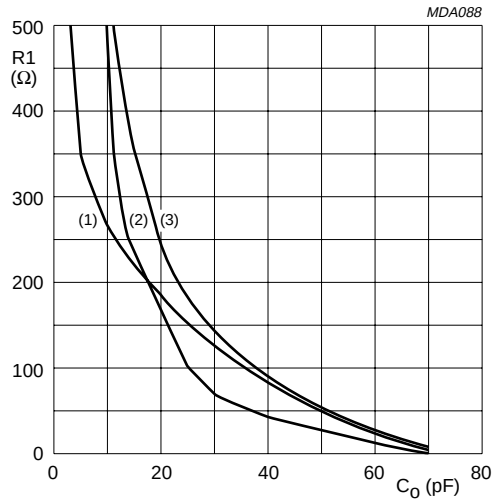


Fig.7 PORENABLE/V_{PP} connection on a PCB.



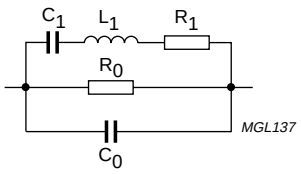
C_{1e} and C_{2e} are the external load capacitances; normally not needed due to integrated load capacitances of typically 10 pF.

(1) $C_{1e} = C_{2e} = 22$ pF.

(2) $C_{1e} = C_{2e} = 0$ pF.

(3) $C_{1e} = C_{2e} = 12$ pF.

a. Resonator curves.



b. Resonator equivalent circuit.

Fig.8 Resonator requirements for the ACO.

6.8 Emulation

The emulator for the P8xCL883/P8xCL884 uses the P87CL880 microcontroller in emulation mode. The P87CL880 is a super-set of the P8xCL883/P8xCL884, i.e. it contains all the functions of the P8xCL883/P8xCL884 plus a number of other additional functions. It should be noted that some functional differences between P87CL880 and P8xCL883/P8xCL884 exist; see Table 12.

Table 12 Differences between functions existing in P87CL880 and P8xCL883/P8xCL884

FUNCTION	P87CL880	P8XCL883/P8XCL884
Timer 2	see P87CL880 specification	see P8xCL883/P8xCL884 specification
OTP Program Memory	32 kbytes AFPROM	8 kbytes EPROM or pre-programmed ROM
RAM	512 bytes	256 bytes
$\overline{EW}$ pin (Watchdog enable)	yes	no
Security concept	see P87CL880 specification	see P8xCL883/P8xCL884 specification
In-System Programming	no	yes
Reset value of SFRs	see P87CL880 specification	see P8xCL883/P8xCL884 specification
POR	hardware programmable	fixed
Frequency	DC to 12.5 MHz	3.58 MHz
Package	QFP64	SO28

6.9 Non-conformance

6.9.1 Programming interface/Transparent mode

The Transparent mode is a special operating mode of the microcontroller used for parallel and In-System OTP programming.

For certain combinations of data written to Port1 (used for control signal during parallel programming mode) the Transparent mode may be incorrectly active during normal operation of the microcontroller. In this case, a transition on any of Port 0 pins can influence the read out of the on-chip program memory, resulting in incorrect code execution.

To avoid this problem, the InSysMode bit in the OTP In-System Programming Register (SFR address DCH) **must** be set in the start-up sequence of the program code.

Apart from preventing incorrect operation as described above, the setting of this bit does not affect the normal operation.

6.9.2 Low Voltage Detection

The LVDI bit (LVDCON.6) may incorrectly be set due to a glitch on the LVD output, when the LVD is enabled, by changing the bits LVDCON(3:0) from ‘0000’ to any value within the range ‘0001’ to ‘0101’. If bit EA in register IEN0 is enabled, an unwanted interrupt may occur.

A software workaround for this problem exists. During the initialisation sequence:

- Enable LVD by writing to register LVDCON
- Enable LVD interrupt by writing to register IEN2
- Clear the LVDI bit by writing to LVDCON a second time
- Set bit EA in register IEN0 (ensures LVDI to be cleared after initialisation).

6.9.3 Edge detection on UART

In receive mode 1, 2 and 3 it is possible that an internal setup/hold condition of a flip-flop is violated. This results in a not detected start bit (start condition) during receive mode. The probability of occurrence (verified on sampling basis) is below 3%.

There is no workaround for this problem other than to use the UART only in Mode 0 for reception.

7 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+4.0	V
V_I	input voltage on any pin with respect to ground (V_{SS})	–0.5	V_{DD} + 0.5	V
P_{tot}	total power dissipation	–	800	mW
T_{stg}	storage temperature	–65	+150	°C

8 CHARACTERISTICS

V_{DD} = 2.7 to 3.6 V; V_{SS} = 0 V; f_{xtal} = 3.58 MHz; T_{amb} = –25 to +70 °C;
T_{amb} (during In-System Programming) = +20 to +40 °C; all voltages with respect to V_{SS} unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage					
	operating		2.7	–	3.6	V
	RAM data retention in Power-down mode		1.0	–	3.6	V
	In-System Programming		3.0	–	3.6	V
V_{PP}	OTP programming voltage		12.5	–	13.0	V
I_{DD}	operating supply current	V_{DD} = 3 V; note 1	—		3.0	mA
		V_{DD} =3V ; T_{amb} =2 5 °C; note 1; see Fig.10	–	1.8	–	mA
$I_{DD(id)}$	supply current Idle mode	V_{DD} = 3 V; note 2	—		0.55	mA
		V_{DD} =3V ; T_{amb} =2 5 °C; note 2; see Fig.11	–	0.38	–	mA
$I_{DD(pd)}$	supply current Power-down mode	V_{DD} =3V ; T_{amb} =2 5 °C; note 3; see Fig.12				
		POR and LVD enabled	–	25		µA
		POR and LVD disabled	–	100	–	nA
$I_{DD(block)}$	supply current per block:	V_{DD} =3V ; T_{amb} =2 5 °C; notes 4 and 5				
	EEPROM erase/write		–	460	–µ	A
	DTMF	no load on TONE output	–	240	–µ	A
	MSK modem		–	140	–µ	A
	Watchdog		–	110	–µ	A
	I^2C-bus		–	90	–µ	A
	UART		–	90	–µ	A
	Timer T2		–	90	–µ	A
	Timer T0 or T1		–	5	–µ	A

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs (Ports, MIN, $\overline{RST}$, MOUT0 to MOUT2, PORENABLE)						
V_{IL}	LOW-level input voltage	notes 6 and 7	0	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage	note 6	$0.8V_{DD}$	–	V_{DD}	V
$\lvert I_{IL}\rvert$	LOW-level input current (ports in Mode 1)	V_{IN} = 0.4 V; note 8; see Fig.9	–	10	50	µA
$\lvert I_{IL(T)}\rvert$	LOW-level input current; HIGH-to-LOW transition (ports in Mode 1)	$V_{IN} = 0.5V_{DD}$; note 8; see Fig.9	–	200	1000	µA
$\lvert I_{LI}\rvert$	input leakage current (ports in Mode 0 or 2)	$V_{SS} \leq V_I \leq V_{DD}$	—		1	µA
Port outputs (Ports, $\overline{RST}$, MOUT0 to MOUT2)						
I_{OL}	LOW-level output current; except P1.3, SDA, SCL and MOUT2	V_{OL} = 0.4 V	2	—		mA
I_{OL1}	LOW-level output current; P1.3 (for LED)	V_{OL} = 0.4 V	6	–	–	mA
I_{OL2}	LOW-level output current; SDA, SCL and MOUT2	V_{OL} = 0.4 V; note 9	3	—		mA
I_{OH}	HIGH-level output current except P1.3; push-pull options only	$V_{OH} = V_{DD} - 0.4$ V	2	—		mA
I_{OH1}	HIGH-level output current P1.3 (for LED); push-pull options only	$V_{OH} = V_{DD} - 0.4$ V	6	—		mA
I_{OH2}	HIGH-level output current MOUT2	$V_{OH} = V_{DD} - 0.4$ V	3	—		mA
$I_{\overline{RST}}$	$\overline{RST}$ pull-up transistor current	V_{DD} = 3 V; $V_{OH} = V_{DD} - 0.4$ V	0.05	0.2	–	µA
		V_{DD} =3V ; $V_{OH} = V_{SS}$	–	0.6	2.5	µA
Power-on reset (POR); for the LVD (Low Voltage Detection) see note 10						
V_{PORH}	Power-on reset trip level HIGH	option 5 in *"TELX family"* specification	2.13	2.37	2.61	V
V_{PORL}	Power-on reset trip level LOW	option A in *"TELX family"* specification	1.98	2.27	2.56	V
TONE output (note 11 and Fig.13)						
$V_{HG(rms)}$	HGF voltage (RMS)	V_{DD} = 3 V	158	181	205	mV
$V_{LG(rms)}$	LGF voltage (RMS)		125	142	160	mV
$\Delta f/f$	frequency deviation		–0.6	–	+0.6	%
V_{DC}	DC voltage level		–	$0.5V_{DD}$	–	V
V_G	pre-emphasis of group		1.5	2.0	2.5	dB
THD	total harmonic distortion	V_{DD} =3V ; T_{amb} =2 5 °C; notes 5 and 12	–	25	–	dB
EEPROM (notes 5 and 13)						
$t_{E/W}$	erase/write time		8	10	12	ms
$N_{E/W}$	erase/write cycles		10^5	—		
t_{DR}	data retention time	T_{amb} = +70 °C1	0	—		years

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
In-System Programming for the OTP						
t_{prog}	program cycle time		90	100	110	µs
t_{ver}	verify cycle time		1	––		µs
$t_{Vpp(setup)}$	program voltage setup time		10	––		µs
$t_{Vpp(max)}$	maximum program voltage time	cumulative for the product lifetime	––		60	s
I_{Vpp}	program voltage current	In-System Programming	––		40	mA
ACO (Amplitude Controlled Oscillator)						
V_{XTAL1}	external clock signal amplitude peak-to-peak		500	–	V_{DD}	mV
$Z_{i(XTAL1)}$	input impedance on XTAL1		300	1000	–	kΩ
C_{1i}; C_{2i}	input capacitance on XTAL1 and XTAL2	notes 5 and 15	–	10	–	pF

Notes

1. The operating supply current is measured with all output pins disconnected; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; $\overline{RST} = V_{DD}$; XTAL1 driven with square wave; XTAL2 not connected; fetch of NOP instructions; all derivative blocks disabled.
2. The Idle mode supply current is measured with all output pins and $\overline{RST}$ disconnected; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; XTAL1 driven with square wave; XTAL2 not connected; all derivative blocks disabled.
3. The Power-down current is measured with all output pins and $\overline{RST}$ disconnected; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; XTAL1 and XTAL2 not connected;.
4. The typical currents are only for the specific block. To calculate the typical power consumption of the microcontroller, the current consumption of the CPU must be added. Example: the typical current consumption of the microcontroller in operating mode with CPU, Watchdog and UART active can be calculated as (1.8 + 0.11 + 0.09) mA = 2.0 mA.
5. Verified on sampling basis.
6. The input threshold voltage of P1.6/SCL and P1.7/SDA meet the I^2C-bus specification. Therefore, an input voltage below $0.3V_{DD}$ will be recognized as a logic 0 and an input voltage above $0.7V_{DD}$ will be recognized as a logic 1.
7. For pin PORENABLE the $V_{IL(max)} = 0.1V_{DD}$.
8. Not valid for pins SDA, SCL, $\overline{RST}$, MIN and PORENABLE.
9. The maximum allowed load capacitance C_L is in this case limited to around 200 pF.
10. The LVD is tested according to the specification in the data sheet *“TELX family; Chapter: Low Voltage Detection”*.
11. Values are specified for DTMF frequencies only (CEPT CS203).
12. Related to the Low Group Frequency (LGF) component (CEPT CS203).
13. After final testing the value of each EEPROM bit is typically logic 1.
14. Can also be done by two 100 µs pulses.
15. C_{1i} and C_{2i} are the total internal capacitances (including gate capacitance, leadframe capacitance).

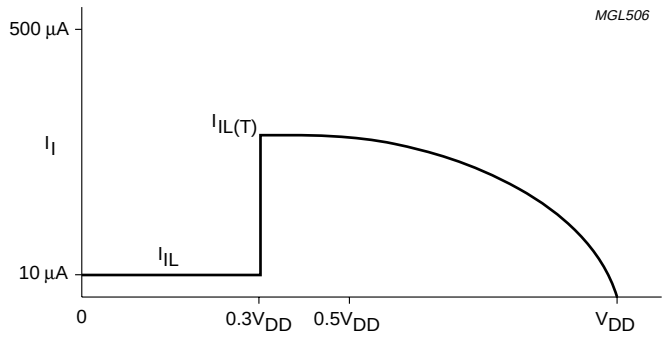


Fig.9 Input current.

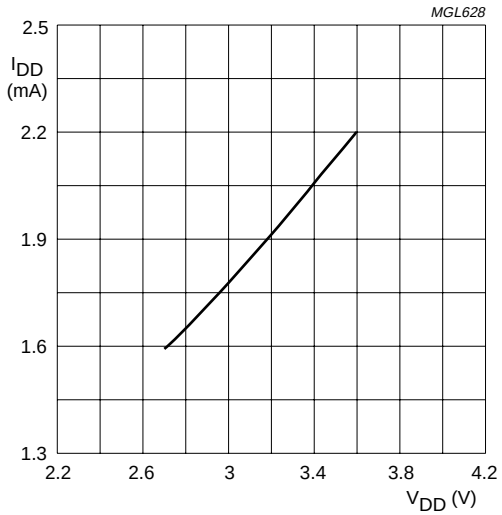


Fig.10 Typical operating current as a function of V_{DD}, T_{amb} = 25 °C.

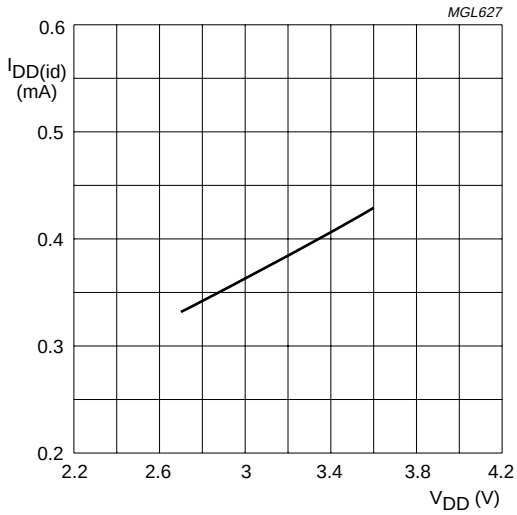
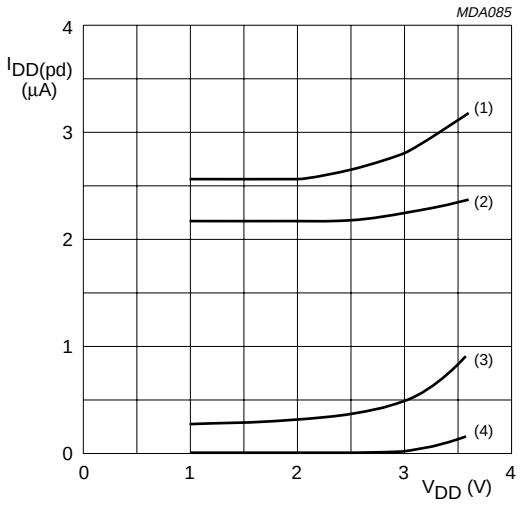
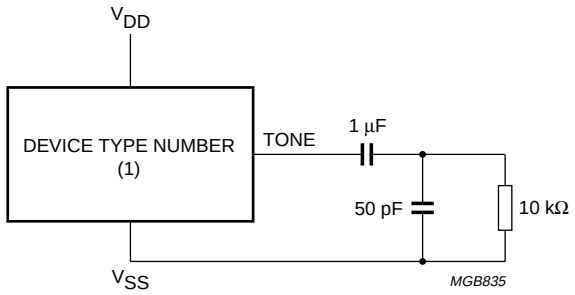


Fig.11 Typical Idle current as a function of V_{DD}, T_{amb} = 25 °C.



(1) POR and LVD enabled (T_{amb} = 70 °C).
(2) POR and LVD enabled (T_{amb} = 25 °C).
(3) POR and LVD disabled (T_{amb} = 70 °C).
(4) POR and LVD disabled (T_{amb} = 25 °C).

Fig.12 Typical Power-down current as a function of V_{DD}.

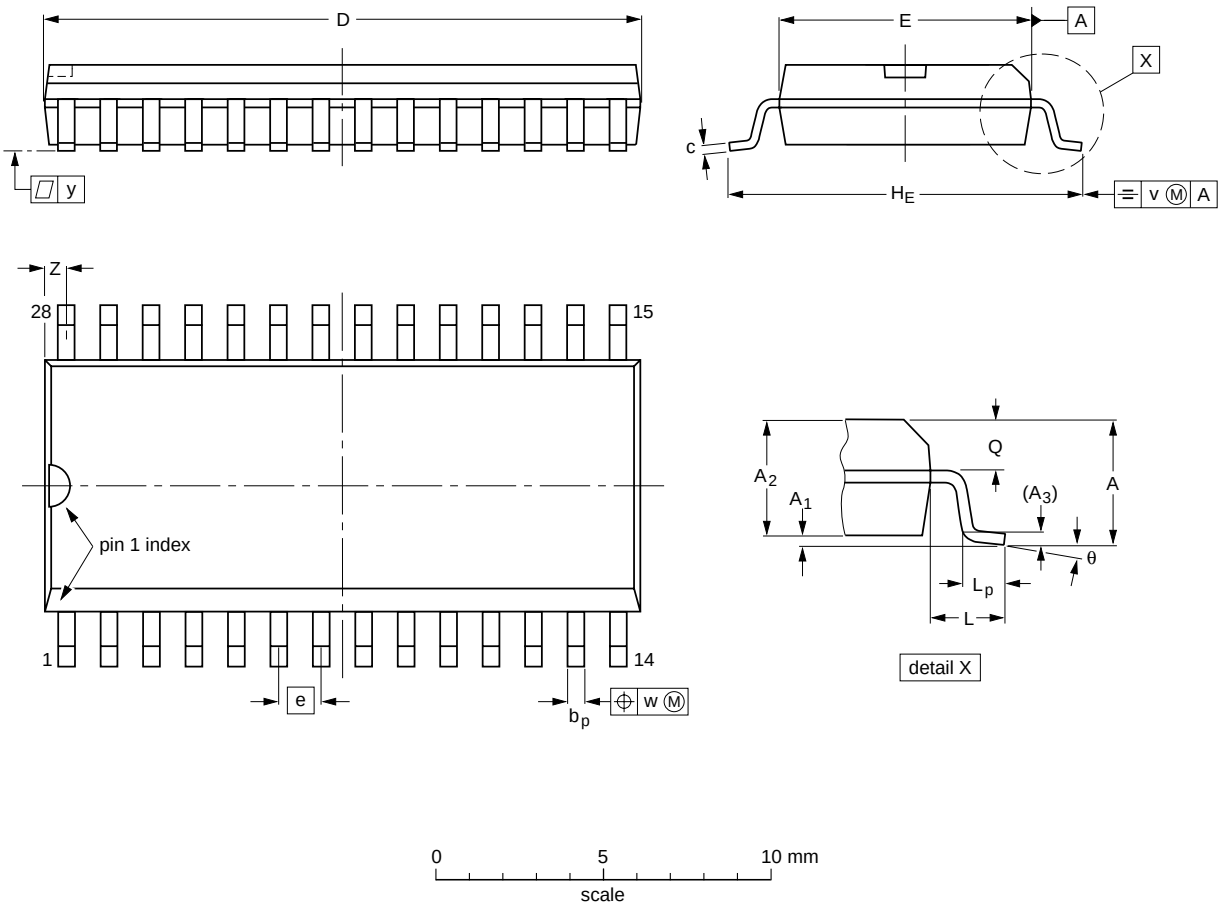


(1) P8xCL883/P8xCL884.

Fig.13 TONE output test circuit.

9 PACKAGE OUTLINE

SO28: plastic small outline package; 28 leads; body width 7.5 mm **SOT136-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	eH	E	LL	p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~95-01-24~~ 97-05-22

10 SOLDERING

10.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

10.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

10.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

10.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

10.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

11 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

12 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

13 PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

NOTES

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