Version : 5.0

TECHNICAL SPECIFICATION

MODEL NO. : PA050DS7

The content of this information is subject to be changed without notice.

Please contact PVI or its agent for further information.

☐Customer's Confirmation

Customer _____

Date _____

By _____

☐PVI's Confirmation

Confirmed By Emmy Chang

Prepared By 李穎敏

Revision History

Rev.	Issued Date	Revised Contents
0.1	Jun. 19 , 2003	NEW
0.2	Aug. 5 , 2003	Page 4 : Update Mechanical Drawing of TFT-LCD Module
1.0	Sep. 01 , 2003	Page 4 : Update Mechanical Drawing of TFT-LCD Module Page 8 : Modify Electrical Characteristics(V_{GL} from –12V to –15V)
2.0	Nov. 24, 2003	Page 21: Modify Optical Characteristics (Contrast Ratio Min. from 110 to 200 & Typ. From 150 to 350)
3.0	Oct. 05, 2004	Page 9: Add Note about Lamp Kick-off Voltage
4.0	April.14.2008	Add Page 26 11.Handling Cautions 11-1 item d)
5.0	Oct. 20 , 2008	Page 5 4. Mechanical Drawing of TFT-LCD Module Add outline UL Label

TECHNICAL SPECIFICATION

CONTENTS

1. Application

This technical specification applies to 5” color TFT-LCD module , PA050DS7. The applications of the panel are car TV , portable DVD and GPS.

2. Features

. Compatible with NTSC & PAL system

. Pixel in stripe configuration

. Slim and compact

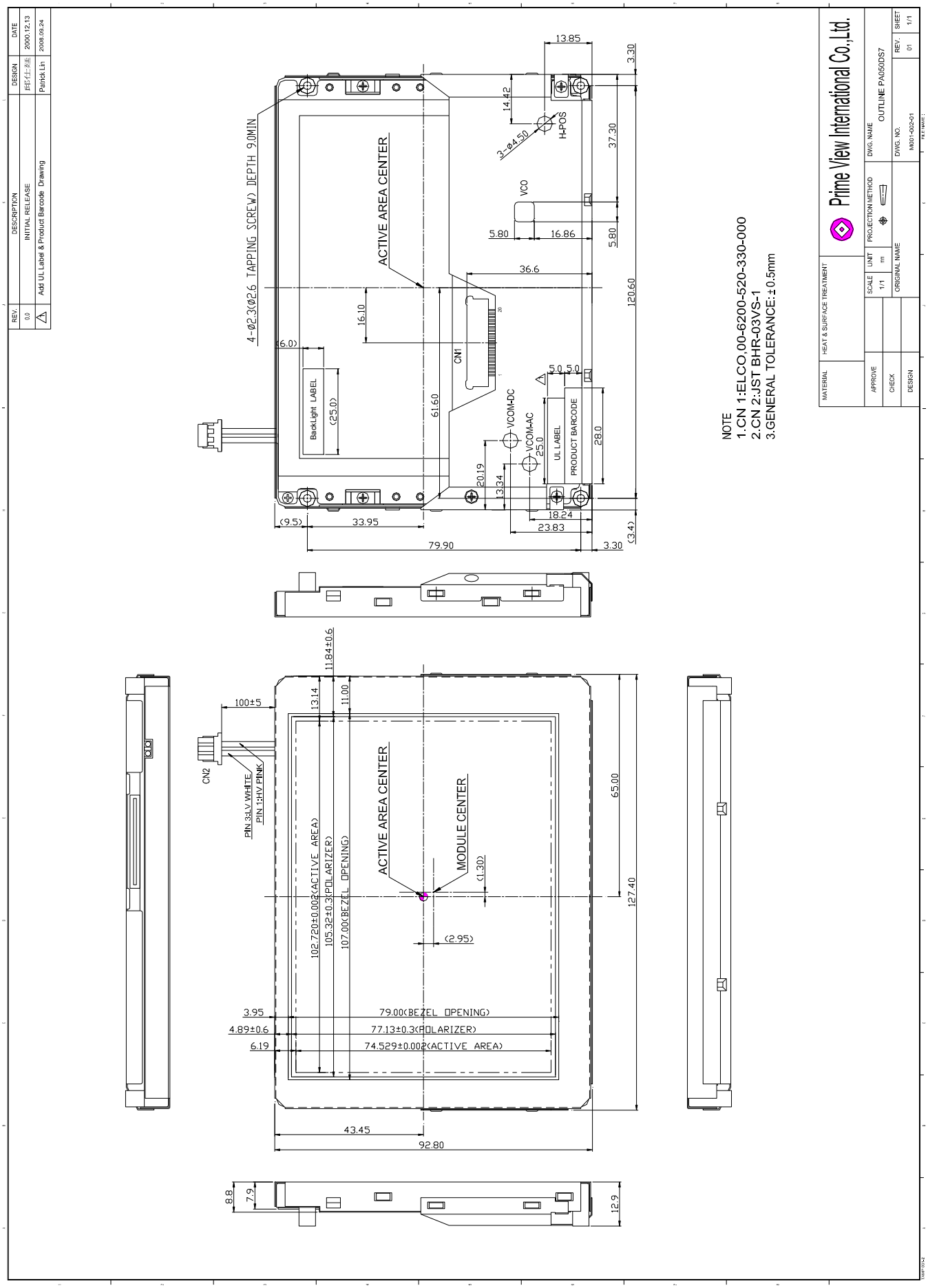
. Vcom Toggle

. Image Reversal : Up/Down and Left/Right

3. Mechanical Specifications

Parameter	Specifications	Unit
Screen Size	5 (diagonal)	inch
Display Format	320×(RGB)×234	dot
Active Area	102.72 (H)×74.53 (V)	mm
Pixel Pitch	0.107 (H)×0.319 (V)	mm
Pixel Configuration	Stripe	
Surface Treatment	AG	
Outline Dimension	127.4 (W)×92.8 (H)×12.9 (D)(typ.)	mm
Weight	164±10	g
Gray scale inversion direction	6 o’clock [ref to Note 10-1]	

4. Mechanical Drawing of TFT-LCD Module



5. Input / Output Terminals

5-1) TFT-LCD Panel Driving

Pin No	Symbol	I/O	Description	Remark
1	$\overline{HSY}$	I/O	Horizontal Sync. Input / Output	Note 5-1
2	POLC	O	Video Polarity Alternating Signal	
3	CSY	I	Composite Sync. Signal	Note 5-1
4	V_{GH}	I	Gate on voltage	Note 5-2
5	V_{GL}	I	Gate off voltage	Note 5-3
6	V_B	I	Video Input B	
7	V_R	I	Video Input R	
8	V_G	I	Video Input G	
9	GND	I	GND	
10	V_{DD}	I	Digital power input	Note 5-4
11	V_{CC}	I	Analogue power input for source driver	Note 5-5
12	GND	I	GND	
13	CKC	I	Select Pin for Internal / External Clock Mode	Note 5-1
14	$\overline{VSY}$	I/O	Vertical Sync. Input / Output	
15	PSI	I	Synchronize Pulse for Decoder	Note 5-6
16	COMPS	I	Select Pin for Composite Sync. Mode & Sync. Separate Mode	Note 5-1
17	$\overline{VIY}$	I	Vertical Sync. Input Pin for Sync. Separate Mode	
18	U/D	I	Up/Down Control for gate driver	Note 5-8
19	R/L	I	Left/Right Control for source driver	Note 5-7
20	NP	I	NTSC / PAL Input	Note 5-9

Note 5-1 : The relation between Pin13 (CKC) and Pin 16 (COMPS) :

Pin13 (CKC)	Pin16 (COMPS)	Pin 1 ($\overline{HSY}$)	Pin3 (CSY)	Pin14 ($\overline{VSY}$)	Pin17 ($\overline{VIY}$)
High	**High**	**$\overline{HSY}$ output**	**CSY input**	**$\overline{VSY}$ output**	**NC**
High	**Low**	**$\overline{HSY}$ output**	**CSY (Hsync.) input**	**$\overline{VSY}$ output**	**$\overline{VIY}$ (Vsync.) input**
Low	**-**	**Hsync. Input**	**External clock**	**Vsync. Input**	**NC**

Note 5-1-1 : CKC = High , COMPS = High (Composite sync. Mode & Internal clock mode)

a. If CKC = 1, COMPS = 1 the phase lock loop (PLL) is adopted in the LCD module (internal clock mode).
b. Input sync. Is CSY.
c. Output sync. Are Horizontal Sync ($\overline{HSY}$, Pin 1) and Vertical Sync ($\overline{VSY}$, Pin 14).

Note 5-1-2 : CKC = High , COMPS = Low (Sync. Separate mode & Internal clock mode)

a. If CKC = 1, COMPS = 0 the phase lock loop (PLL) is adopted in the LCD module (internal clock mode).
b. Input sync. Are Horizontal sync. (CSY , Pin3) and Vertical sync. ($\overline{VIY}$, Pin17).
c. Output sync. Are Horizontal Sync ($\overline{HSY}$, Pin 1) and Vertical Sync ($\overline{VSY}$, Pin 14).

Note 5-1-3 : CKC = Low , COMPS = Don't care (External clock mode)

a. If CKC = 0 , the phase lock loop (PLL) is not adopted in the LCD module.
   If CKC = 0 , the external clock input frequency of Pin 3 is 6.4 MHz.
b. Input external Vertical Sync ($\overline{VSY}$, Pin 14) and Horizontal Sync ($\overline{HSY}$, Pin 1) to synchronize the LCD module.
c. The pulse width of external Horizontal Sync input is 4.7μs±2 μs. The pulse width of external Vertical Sync input is 2H~4H.
d. The pulse length of external input Vertical Sync of system is 262H±4H.

Note 5-1-4 : If there is any question about CKC = 0 , please contact PVI.

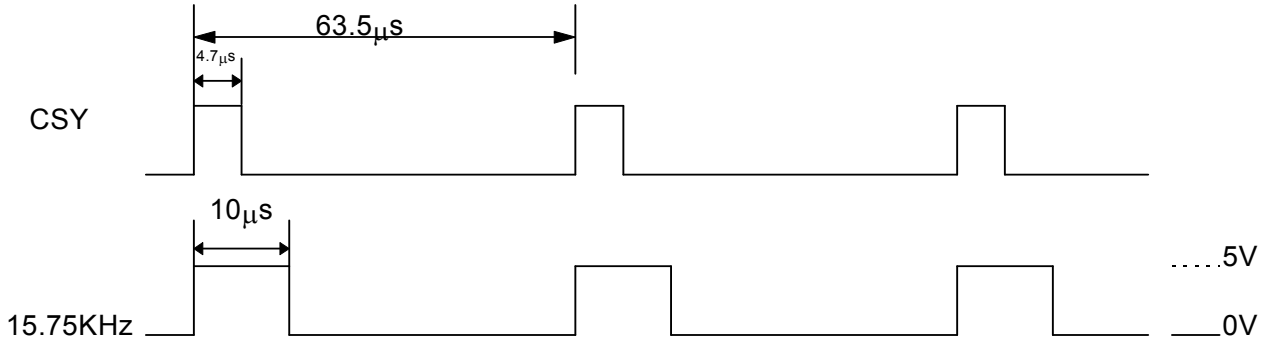
Note 5-2 : V_{GH} TYP.＝+17V

Note 5-3 : V_{GL} TYP.＝-15V

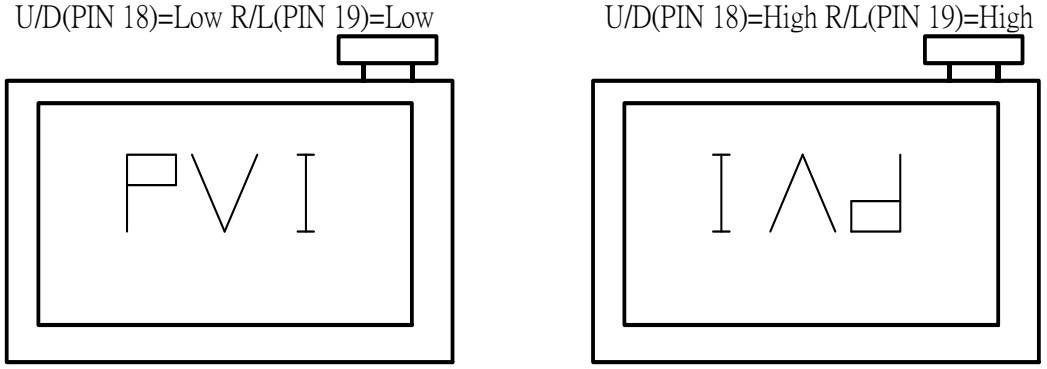
Note 5-4 : V_{DD} TYP.＝+5V

Note 5-5 : V_{CC} TYP.＝+5V

Note 5-6 : The frequency of PSI is 15.75KHz.

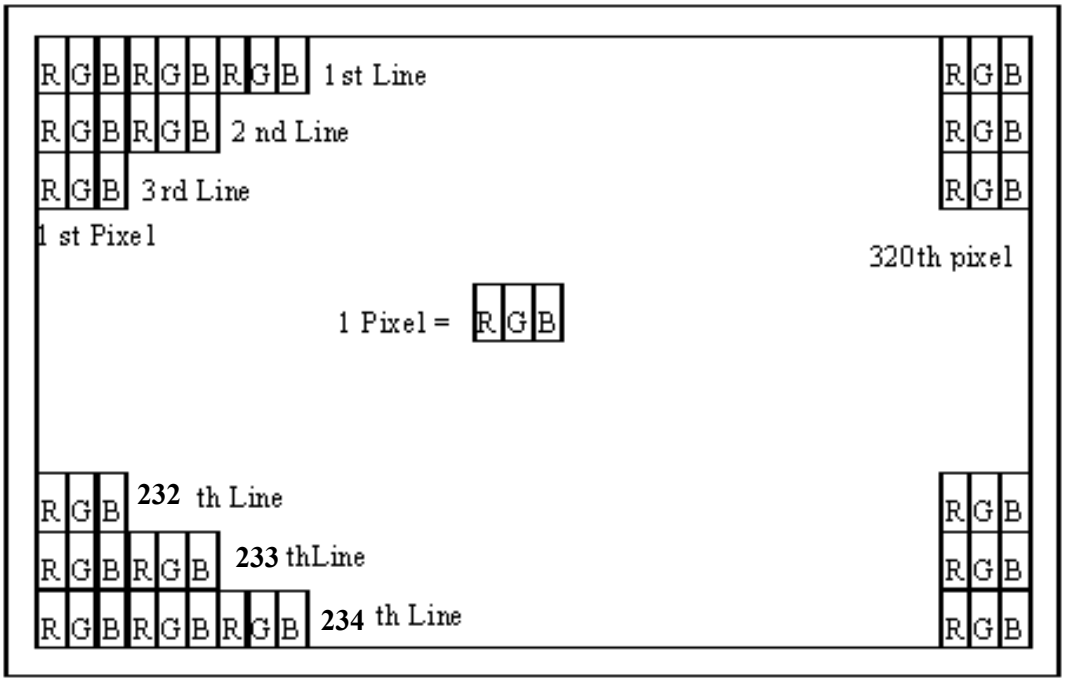


Note 5-7,5-8 : The definitions of U/D & R/L



Note 5-9 : NTSC = Hi (+5V) , PAL = LOW (0V).

6. Pixel Arrangement



7. Absolute Maximum Ratings :

The followings are maximum values, which if exceeded, may cause faulty operation or damage to the unit.

GND = 0 V， Ta = 25 ℃

Parameter		Symbol	MIN.	MAX.	Unit	Remark
Supply Voltage For Source Driver		V_{CC}	-0.3	+7.0	V	
		V_{DD}	-0.3	+7.0		
Supply Voltage For Gate Driver	H Level	V_{GH}	-0.3	+45	V	
	L Level	V_{GL}	-23	+0.3	V	
		V_{GH}–V_{GL}	+15	+40	V	
Analog Signal Input Level		V_R、V_G、V_B	-0.3	+7.3	V	Note 7-1
Digital input signals			-0.5	+5.5	V	Note 7-2
Digital output signals			-0.5	+5.5	V	

Notes 7-1 : Analog Input Voltage means V_R,V_G,V_B.

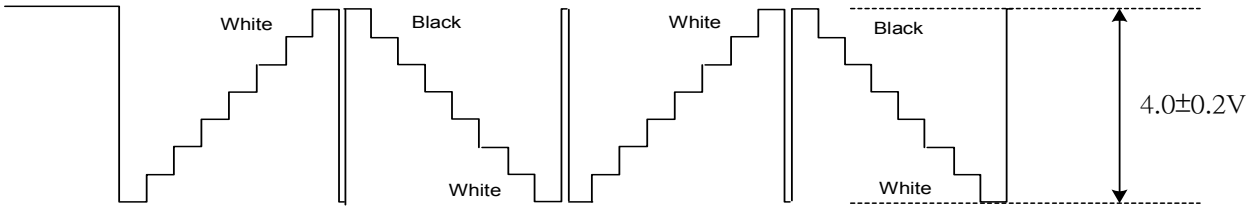
Notes 7-2 : $\overline{HSY}$, POLC, CSY , $\overline{VSY}$, CKC , PSI , COMPS , $\overline{VIY}$

8. Electrical Characteristics

8-1) Operating Condition

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power Supply		V_{CC}	+4.5	+5.0	+5.5	V	
		V_{DD}	+4.5	+5.0	+5.5	V	
		V_{GH}	+15.0	+17.0	+19.0	V	
		V_{GL}	-16.0	-15.0	-14.0	V	DC Component of V_{GL}
Video Signal (V_R, V_G, V_B)		$V_{i\,AC}$	-	+4.0	+4.2	V_{P-P}	AC Component Note 8-1
		$V_{i\,DC}$	-	+2.5	-	V	DC Component
Digital input voltage	H Level	V_{IH}	+0.7 V_{DD}	-	V_{DD}	V	
	L Level	V_{IL}	-0.3	-	+0.3 V_{DD}	V	
Digital output voltage	H Level	V_{OH}	+0.7 V_{DD}	-	V_{DD}	V	
	L Level	V_{OL}	-0.3	-	+0.3 V_{DD}	V	

Note 8-1: Both NTSC and PAL system Video Signal input waveform is based on 8 steps gray scale.



8-2) Current Consumption (GND=0V)

Ta= 25 ℃

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Current for Driver	I_{GH}	V_{GH}=+17V	-	5.2	6.76	mA	
	I_{GL}	V_{GL}=-15V	-	9.3	12.1	mA	V_{GL} center voltage
	I_{CC}	V_{CC}=+5V	-	7.5	9.75	mA	
	I_{DD}	V_{DD}=+5V	-	14.2	18.46	mA	

8-3) Backlight driving & Power Consumption

Pin No	Symbol	Description	Remark
1	VL1	Input terminal (Hi voltage side)	
3	VL2	Input terminal (Low voltage side)	Note 8-2

Note 8-2 : Low voltage side of backlight inverter connects with Ground of inverter circuits.

Ta= 25 ℃

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Lamp voltage	V_L	423 (8mA)	448	494 (3mA)	Vrms	
Lamp current	I_L	3.0	6.0	8.0	mA	Note 8-3
Lamp frequency	F_L	40	55	80	KHz	Note 8-4
Kick-off voltage(25℃)	Vs	-	-	600	Vrms	Note 8-5
Kick-off voltage(0℃)	Vs	-	-	760	Vrms	Note 8-5

Note 8-3 : In order to satisfy the quality of B/L , no matter use what kind of inverter , the output lamp current must between Min. and Max. to avoid the abnormal display image caused by B/L.

Note 8-4 : The waveform of lamp driving voltage should be as closed to a perfect SIN wave as possible.

Note 8-5 : This value is not output voltage of inverter.
The voltage of inverter must larger than the starting voltage.
The kick-off time must larger than 1 second.

Power Consumption

Ta= 25 ℃

Parameter	Symbol	Conditions	TYP.	Unit	Remark
LCD Panel Power Consumption			0.25	W	Note 8-6
Backlight Lamp Power Consumption			2.69	W	Note 8-7
Total Power Consumption			2.95	W	

Note 8-6：The power consumption for backlight is not included.

Note 8-7：Backlight lamp power consumption is calculated by $I_L \times V_L$.

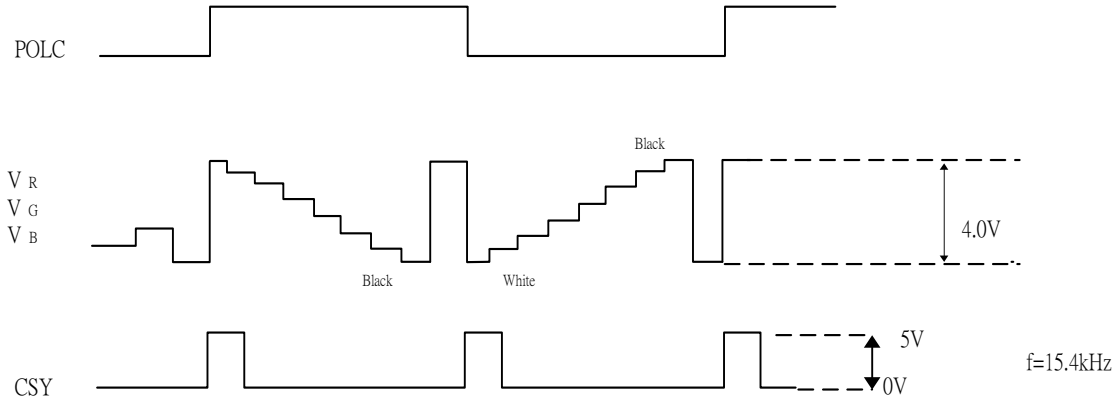
8-4) Input / Output Connector

A) LCD Module Connector
ELCO,00-6200-520-330-000
FFC Down Connector
20 Pins
Pitch : 1.0 mm

B) Backlight Connector
JST BHR-03VS-1
Pin No. : 3
Pitch : 4 mm
Pink : High Voltage
White : Low Voltage

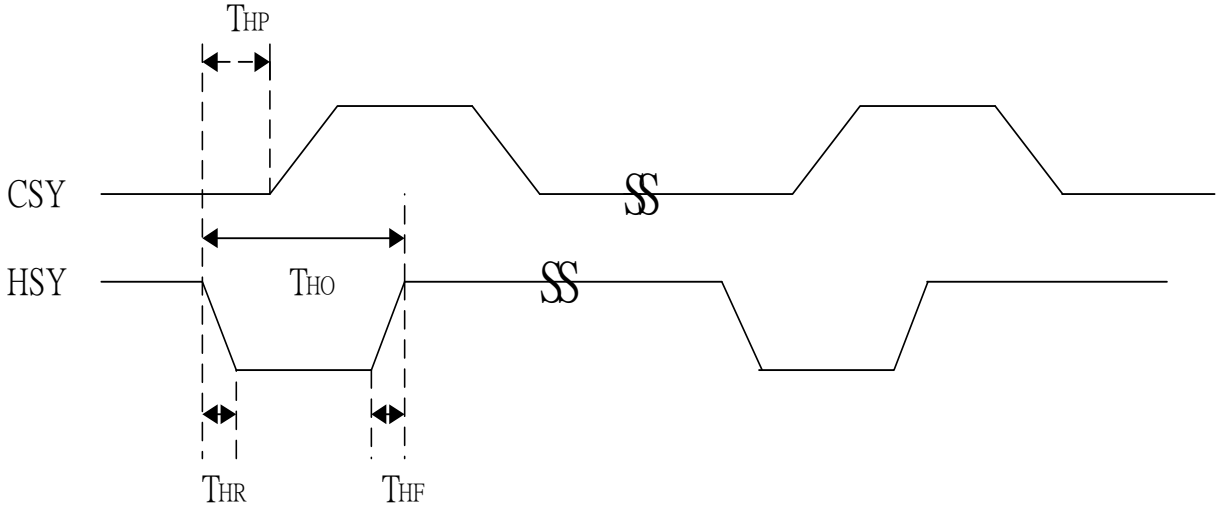
8-5) Input / Output signal timing chart

A)Composite sync. & sync. Separate mode's timing



Parameter			Symbol	MIN.	TYP.	MAX.	Unit	Remarks
Horizontal Sync. Output Pulse	Frequency	NTSC	$F_{HO}(N)$	-	15.75	-	KHz	
		PAL	$F_{HO}(P)$	-	15.63	-	KHz	
	Pulse Width		T_{HO}	4.4	4.7	5.0	μs	
	Phase Difference		T_{HP}	0	2	-	μs	
	Rising Time		T_{HR}	-	-	0.05	μs	
	Falling Time		T_{HF}	-	-	0.05	μs	
Vertical Sync. Output Pulse	Frequency	NTSC			fh/262.5			
		PAL			fh/312.5			
	Pulse Width		T_{VO}	-	4H	-	μs	
	Phase Difference	NTSC	$T_{VPO(N)}$	-	1H	-	μs	odd field
		PAL	$T_{VPO(P)}$	-	1H	-		
	Phase Difference	NTSC	$T_{VPE(N)}$	-	1.5H	-	μs	even field
		PAL	$T_{VPE(P)}$	-	0.5H	-		

B)External clock mode's timing



Parameter		Symbol	MIN.	TYP.	MAX.	Unit	Remarks
Input Clock signal	Frequency	f_{CLI}	5.8	6.4	7.0	MHz	
	Hi pulse width	τ_{WH}	20.0	-	-	ns	
	Lo pulse width	τ_{WL}	20.0	-	-	ns	
	Rising edge time	τ_{rCLI}	-	-	10.0	ns	
	Falling edge time	τ_{fCLI}	-	-	10.0	ns	
Input Horizontal synchronize signal	Frequency	f_{HI}	f_{CLI} / 430	f_{CLI} / 406	f_{CLI} / 396	Hz	
	Pulse width	τ_{HI}	1.0	5.0	9.0	μs	
	Rising edge time	τ_{rHI}	-	-	0.05	μs	
	Falling edge time	τ_{fHI}	-	-	0.05	μs	
Input Vertical Synchronize signal	Frequency	f_{VI}	50	f_{HI} / 262	f_{HI} / 258	Hz	
	Pulse width	$\tau_{VI(P)}$	1H	3H	5H		
	Rising edge time	τ_{rVI2}	-	-	0.5	μs	
	Falling edge time	τ_{fVI2}	-	-	0.5	μs	
Data set up time		t_{SU1}	25	-	-	ns	
Data hold time		t_{HO1}	25	-	-	ns	
Data set up time		t_{SU2}	1.0	-	-	μs	
Data hold time		t_{HO2}	1.0	-	-	μs	

8-6) Display Time Range

Composite sync. & sync. Separate mode

The Both two timing can adjust with H-position

A) When sync. Signal of NTSC system is applied.

a) Horizontally

11.35 ~ 61.36 μs.

b) Vertical

22 ~ 255 H

B) When sync. Signal of PAL system is applied.

1. Horizontal

11.54 ~ 61.9 μs .

2. Vertical

30 ~ 302 H

3. Odd field : Scan lines 14n+7 14n+13 (n=2,3,4…) are not displayed.

4. Even field : Scan lines 14n+4 14n+10 (n=2,3,4…) are not displayed.

C) External clock mode (CKC = " LOW ")

1. Horizontal direction

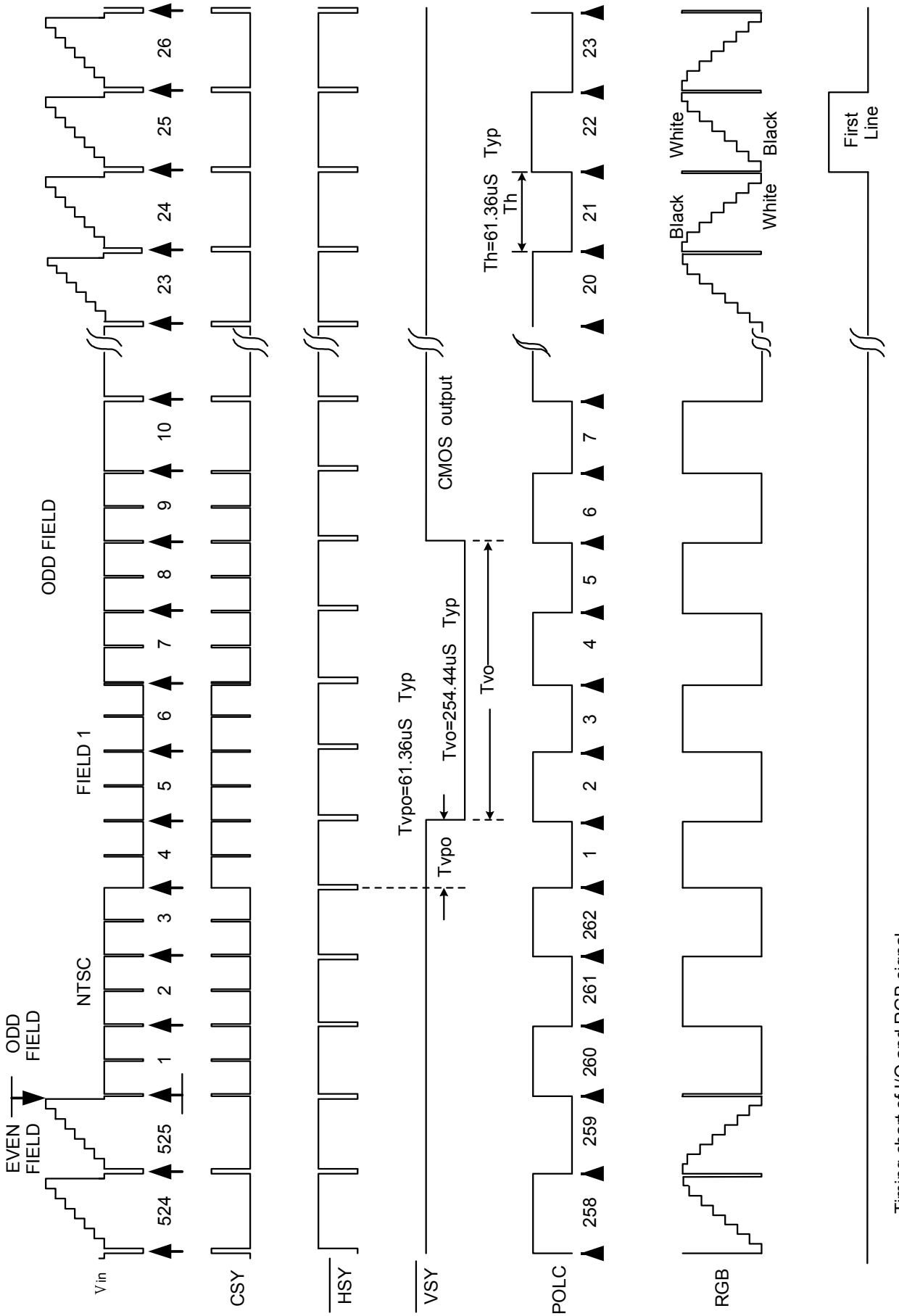
69 ~ 388 CLK from the falling edge of $\overline{HSY}$

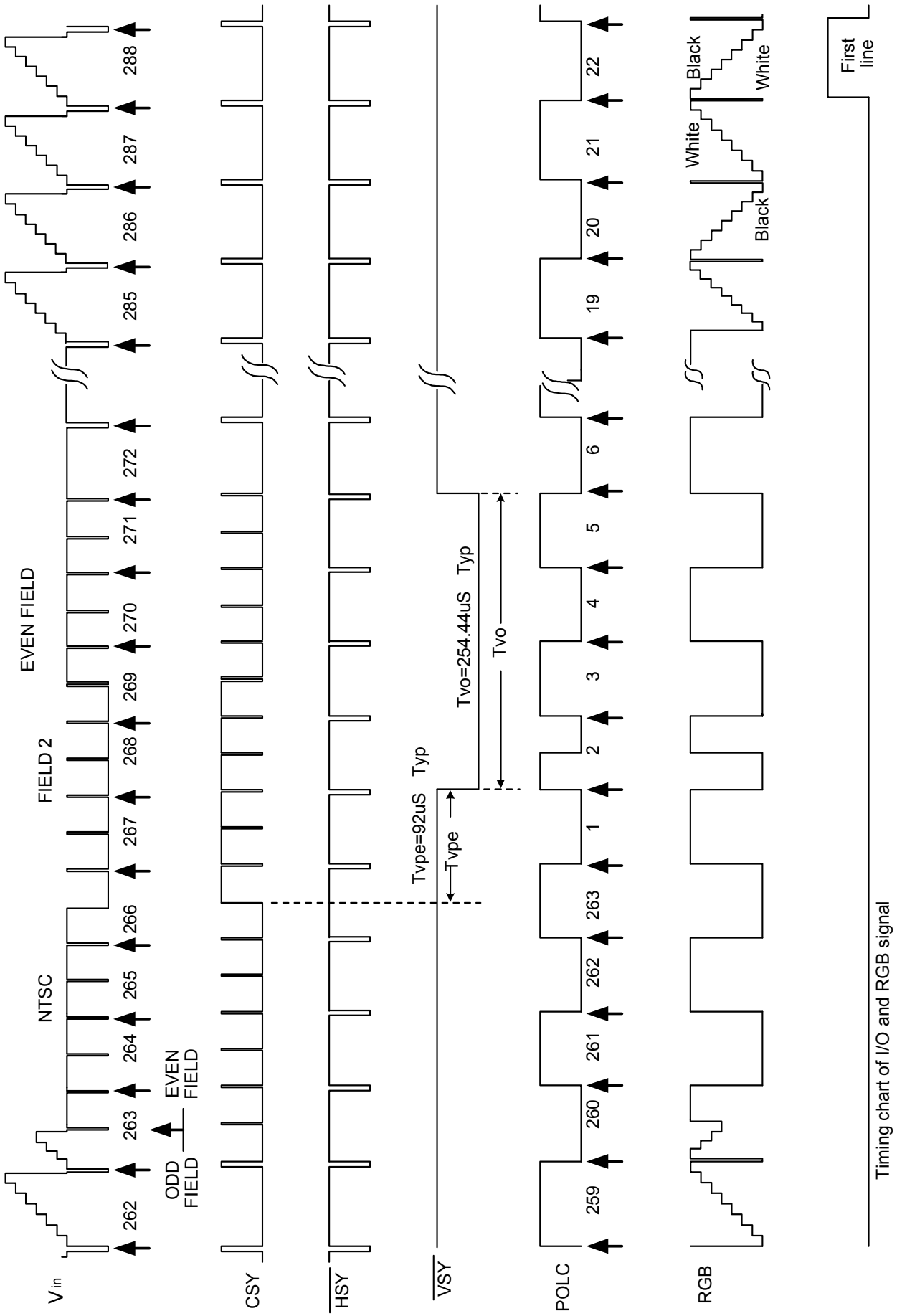
CLK means input external clock. (6.4MHz TYP.)

2. Vertical direction

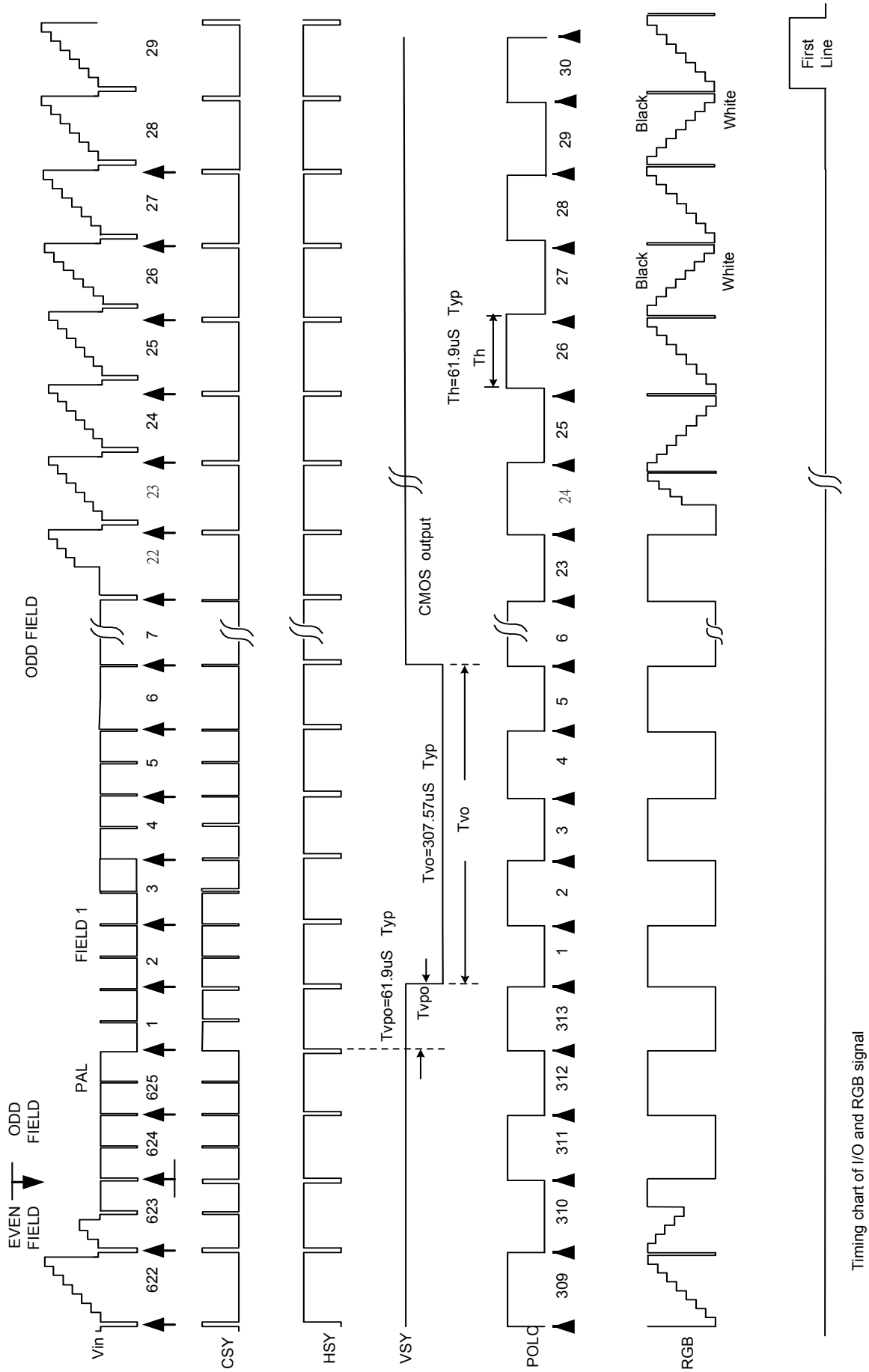
22 ~ 255 H from the falling edge of $\overline{VSY}$

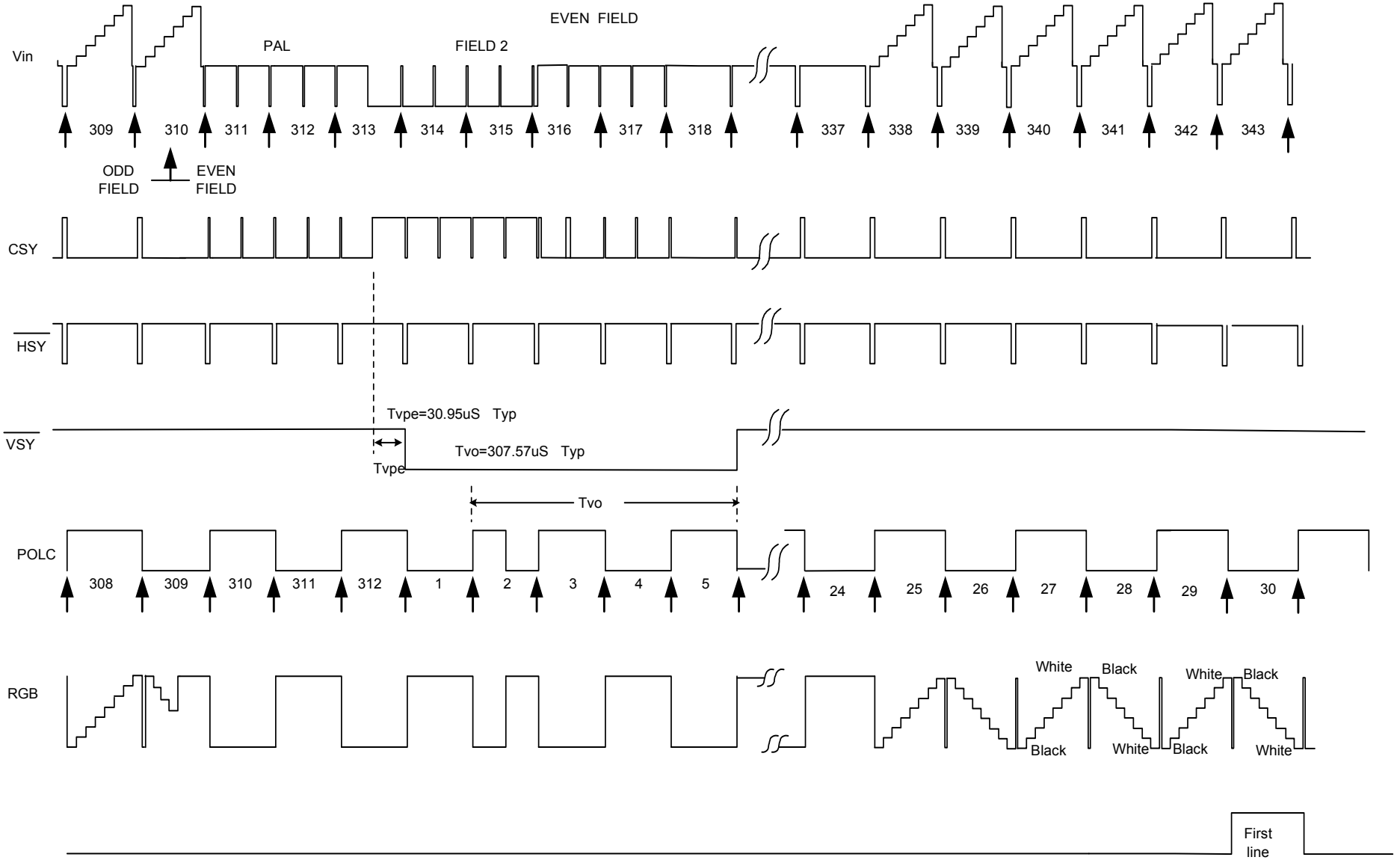
D) NTSC System (Composite sync. Mode)





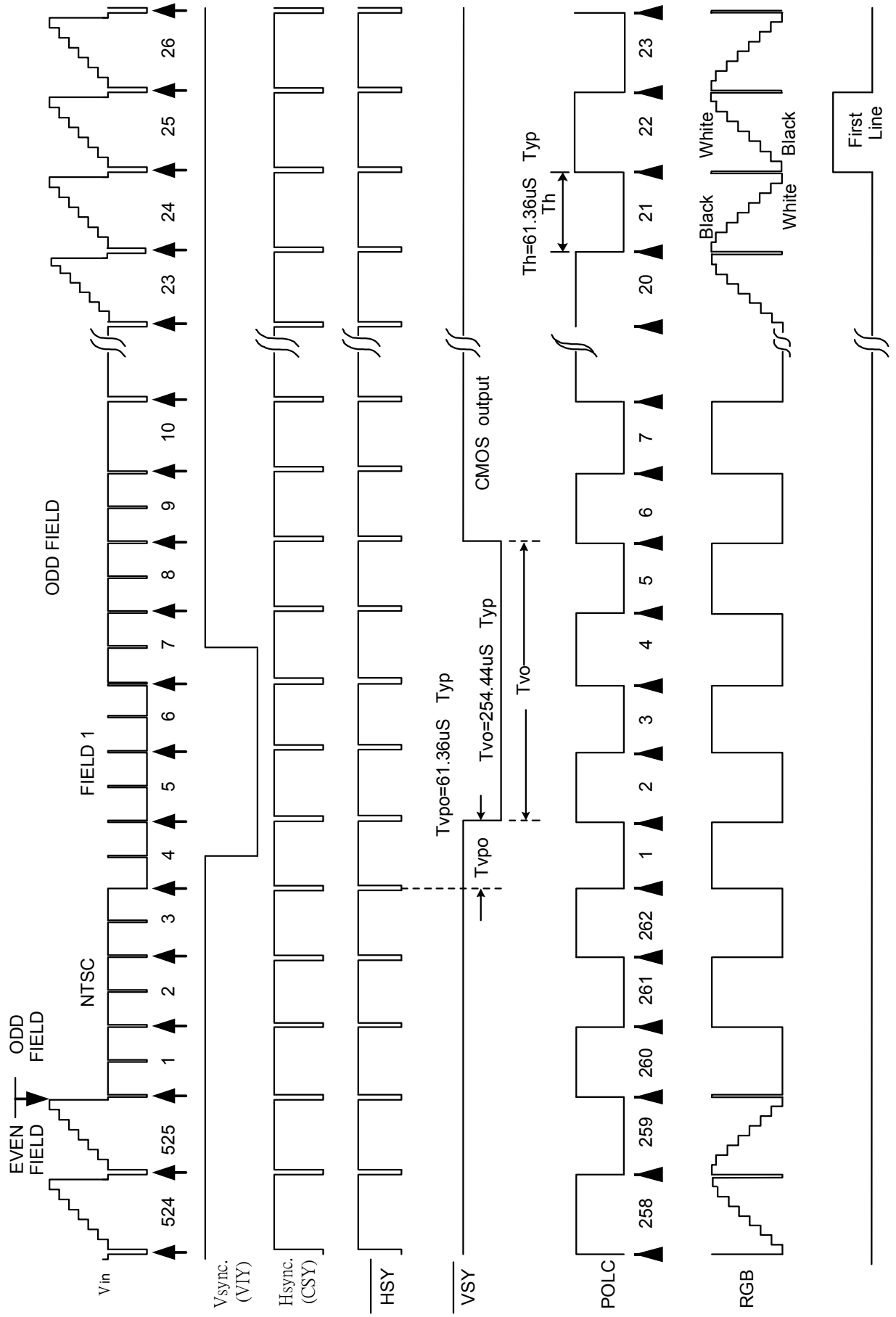
E) PAL System (Composite sync. Mode)



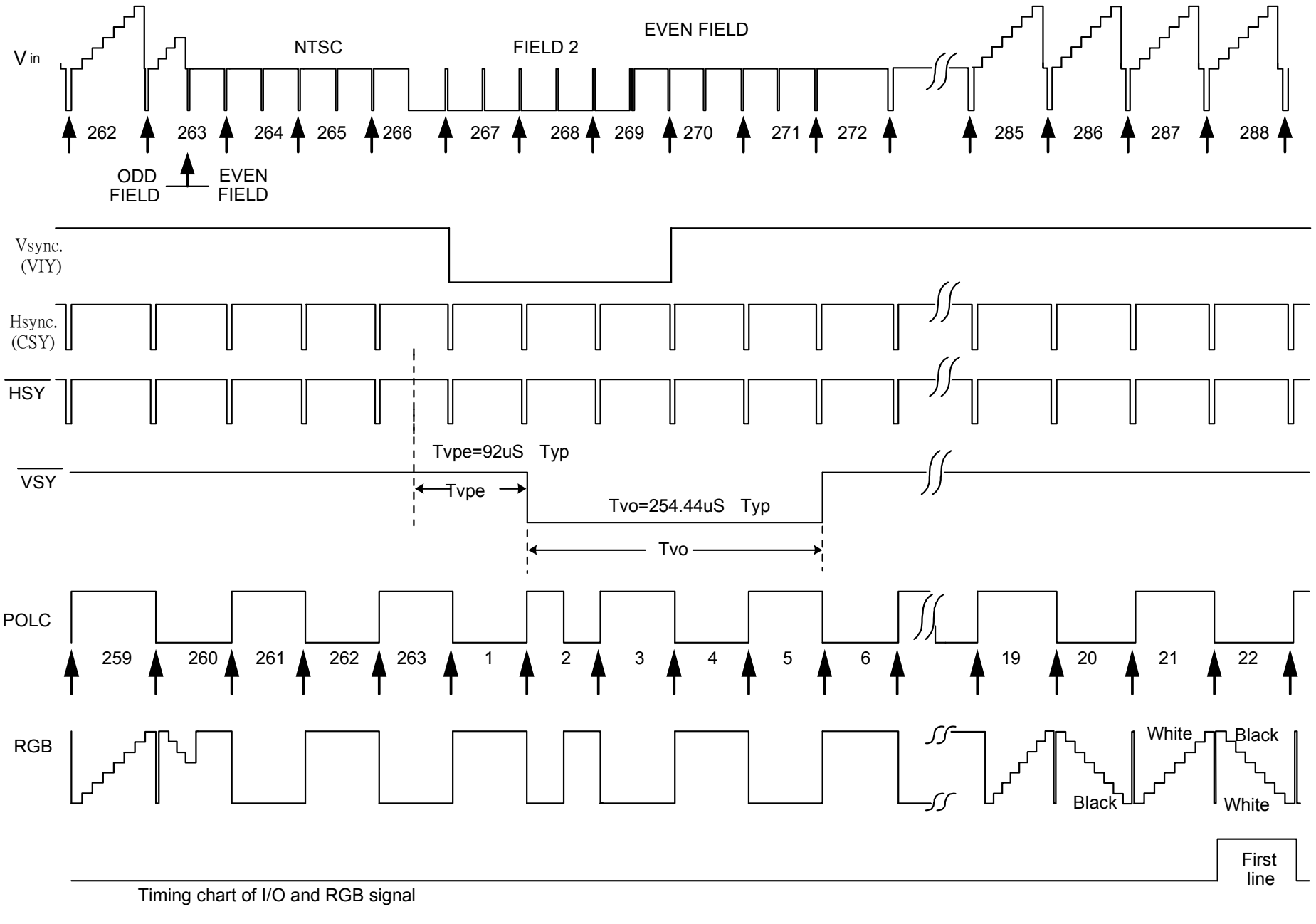


Timing chart of I/O and RGB signal

F) NTSC System (Sync. Separate mode)



Timing chart of I/O and RGB signal



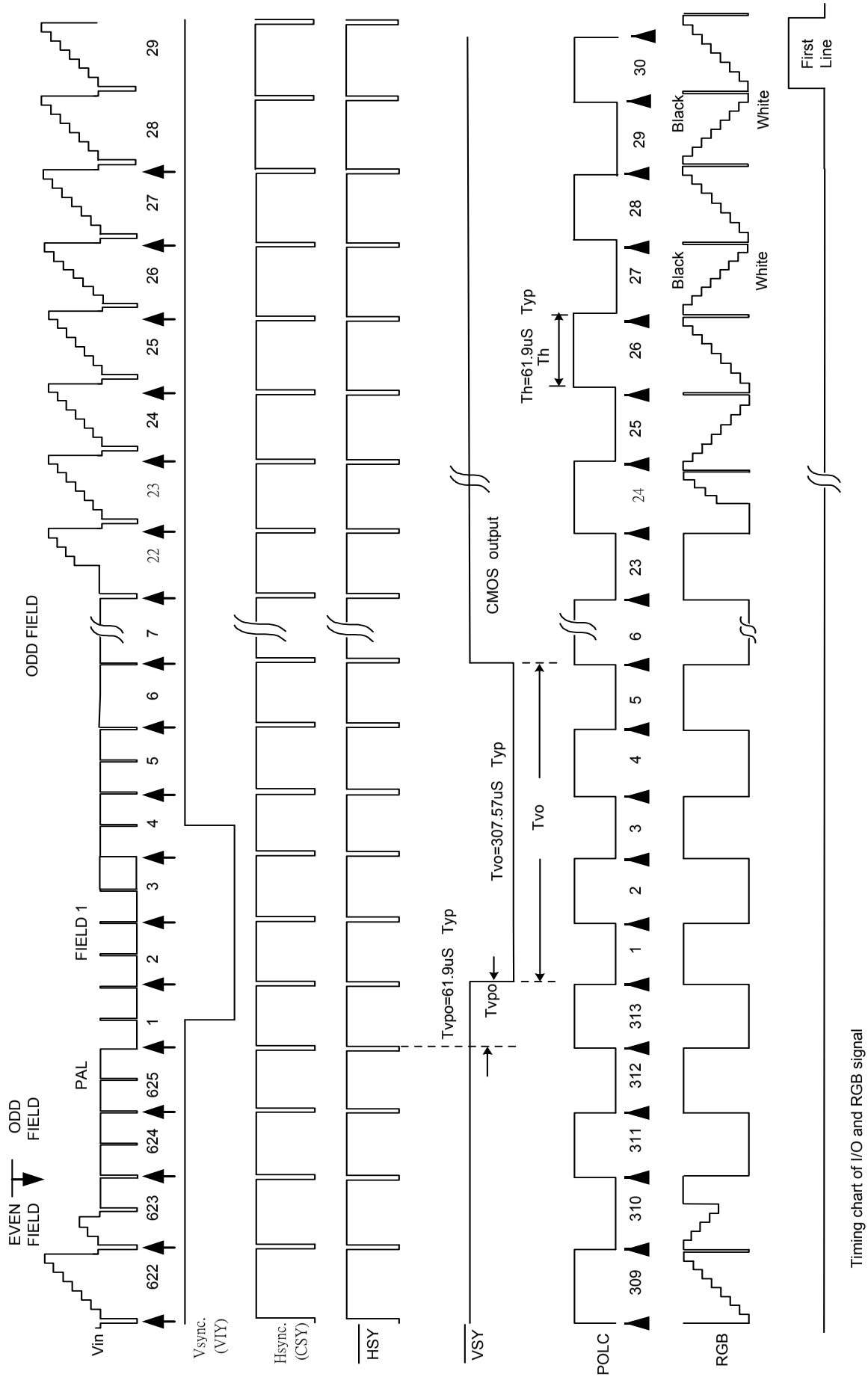
Timing chart of I/O and RGB signal

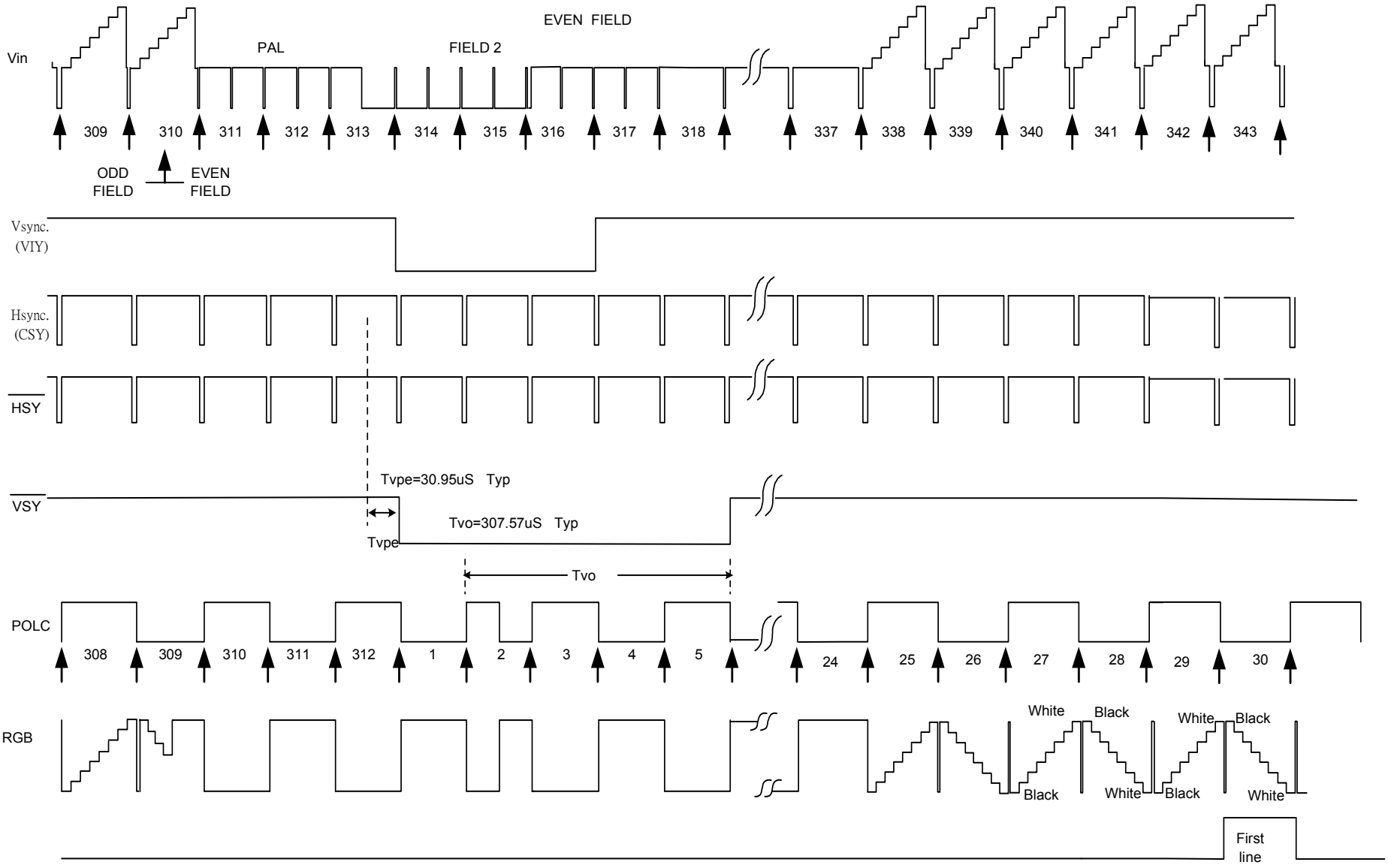
PRIME VIEW

PA050DS7

P-511-152(V:5)

G) PAL System (Sync. Separate mode)



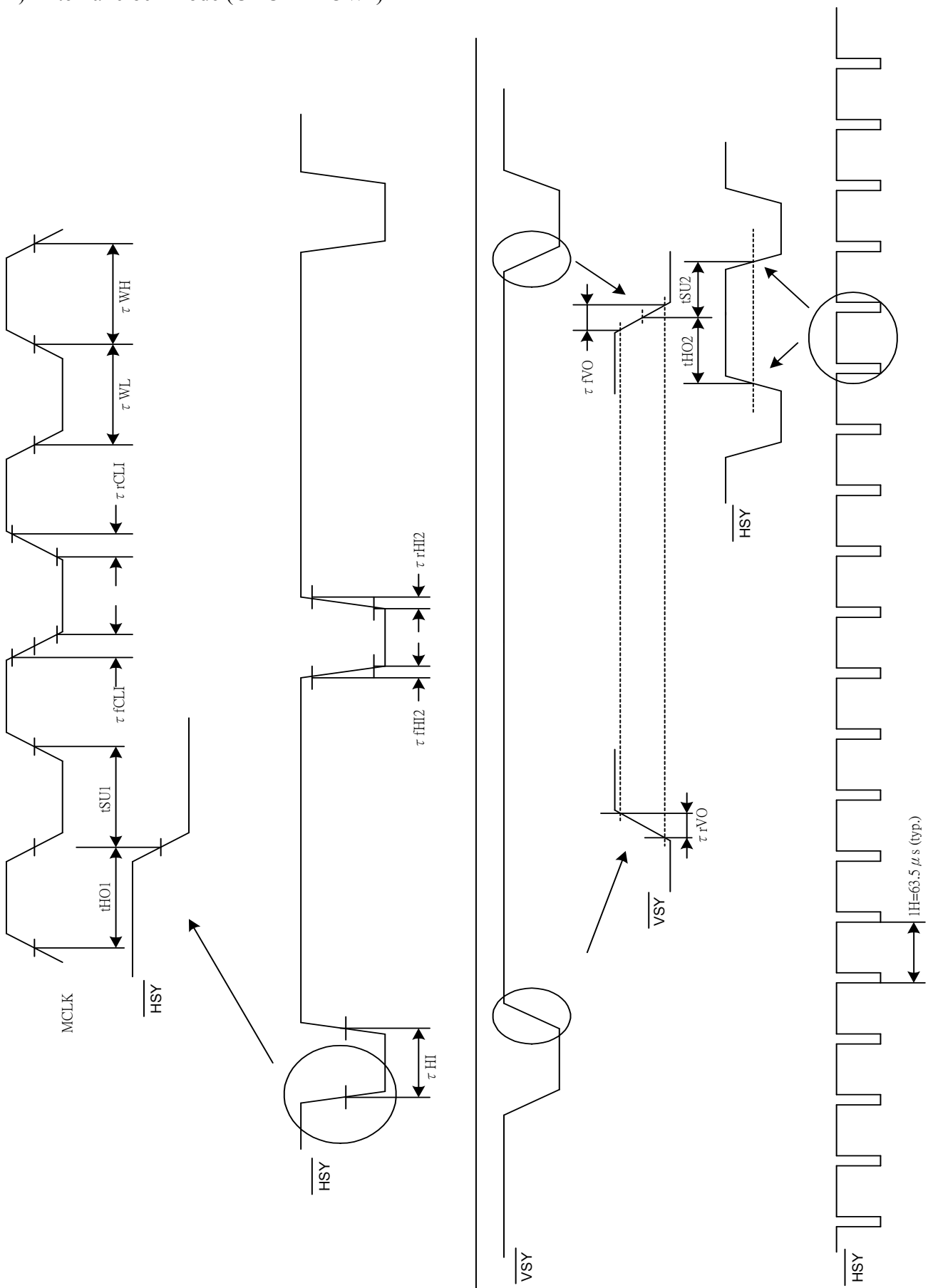


Timing chart of I/O and RGB signal

PRIME VIEW

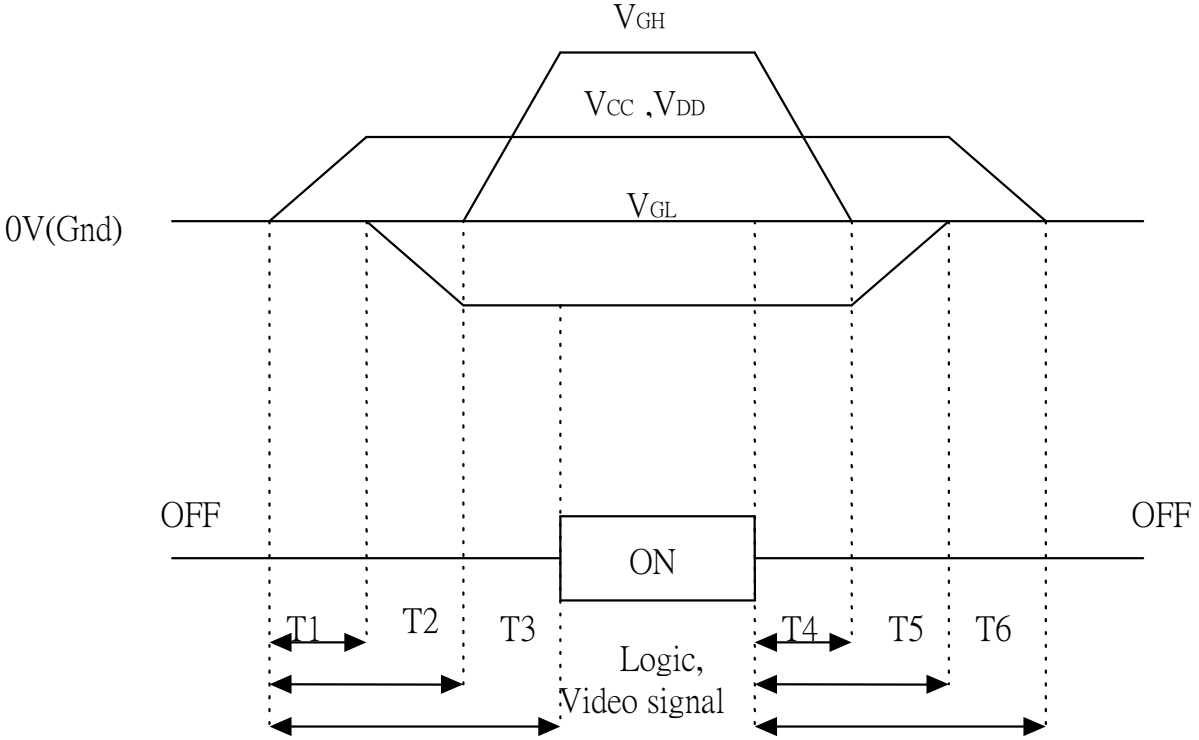
PA050DS7

H) External clock mode (CKC = “LOW”)



9. Power On Sequence

The Power on Sequence only effect by V_{CC},V_{SS},V_{DD},V_{EE} and $V_{GH,}$ the others do not care.



1) 10ms≦T1≦T2≦T3
2) 10ms≦T4≦T5≦T6

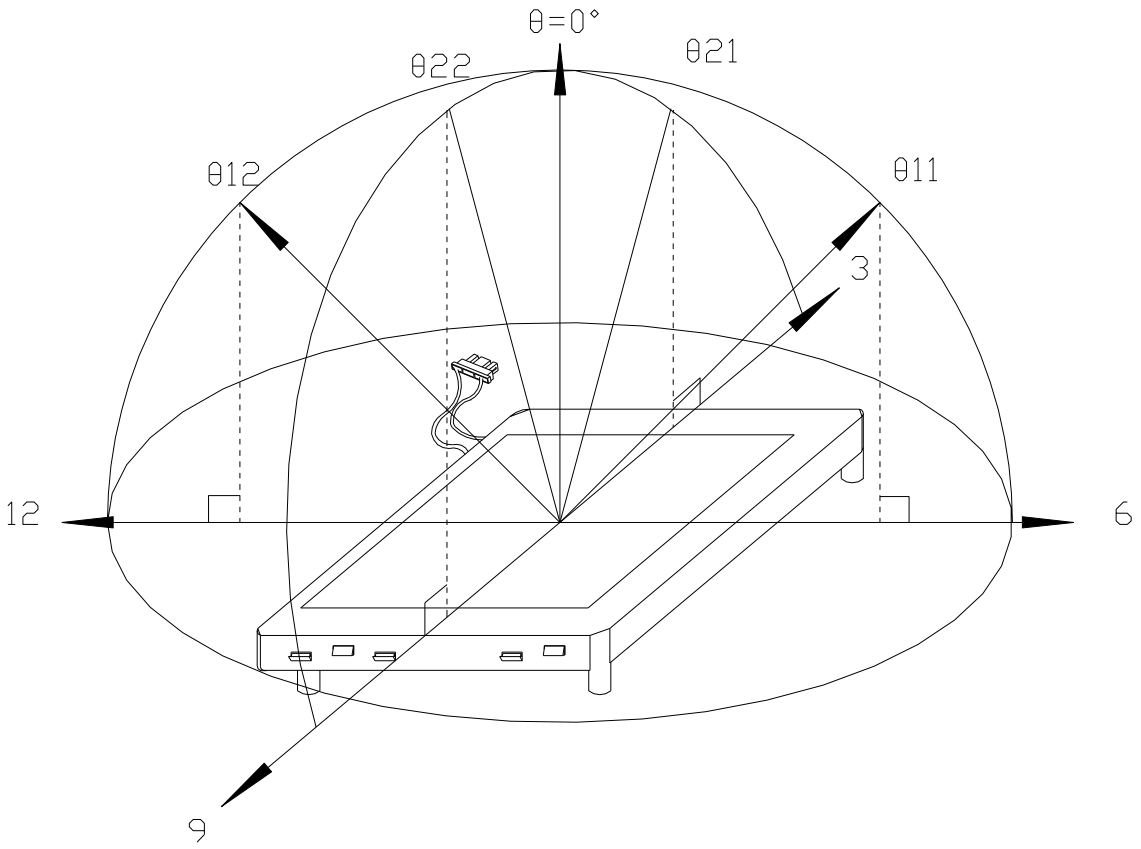
10. Optical Characteristics

10-1) Specification:

Ta = 25℃

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	θ21, θ22	CR≧10	45	50	---	deg	Note 10-1
	Vertical	θ11		30	35	---	deg	Note 10-1
		θ12		10	15	---	deg	Note 10-1
Contrast Ratio		CR	At optimized Viewing angle	200	350	---		Note 10-2
Response time	Rise	Tr	θ=0°	---	15	30	ms	Note 10-4
	Fall	Tf		---	30	50	ms	
Transmission Ratio				8.0	8.5	---	%	
Uniformity		U		70	80	---	%	Note 10-5
Brightness				350	400	---	cd/㎡	Note 10-3
White Chromaticity		x	θ=0°	0.270	0.300	0.330		Note 10-3
		y	θ=0°	0.310	0.340	0.370		
Lamp Life Time +25℃				30,000	---	---	hr	

Note 10-1 : The definitions of viewing angles



Note 10-2 : CR = $\frac{\text{Luminance when Testing point is White}}{\text{Luminance when Testing point is Black}}$

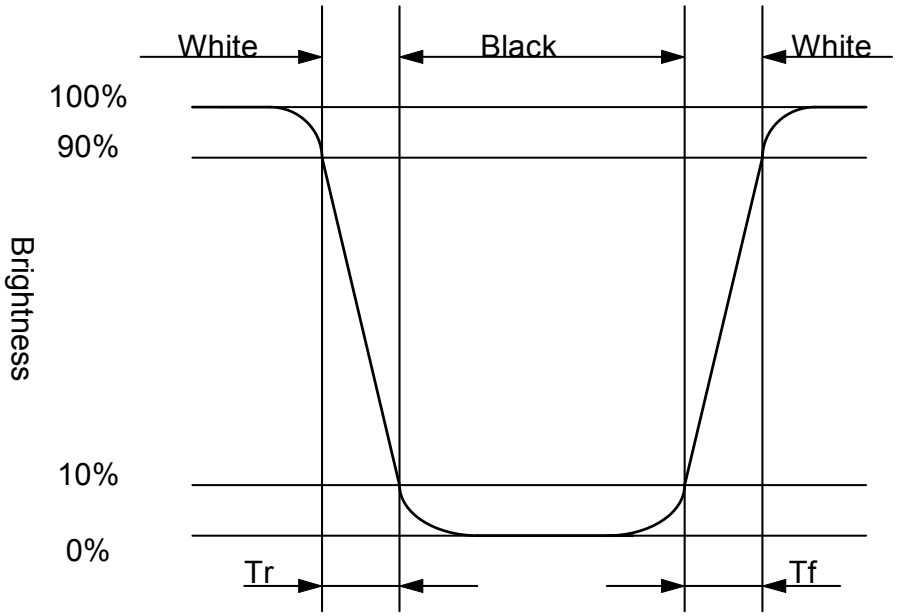
(Testing configuration see 10-2)

Contrast Ratio is measured in optimum common electrode voltage.

Note 10-3 : Topcon BM-7(fast) luminance meter 2°field of view is used in the testing (after 20~30 minutes operation).

Lamp Current 6mA

Note 10-4 : The definition of response time :



Note 10-5: The uniformity of LCD is defined as

$$U = \frac{\text{The Minimum Brightness of the 9 testing Points}}{\text{The Maximum Brightness of the 9 testing Points}}$$

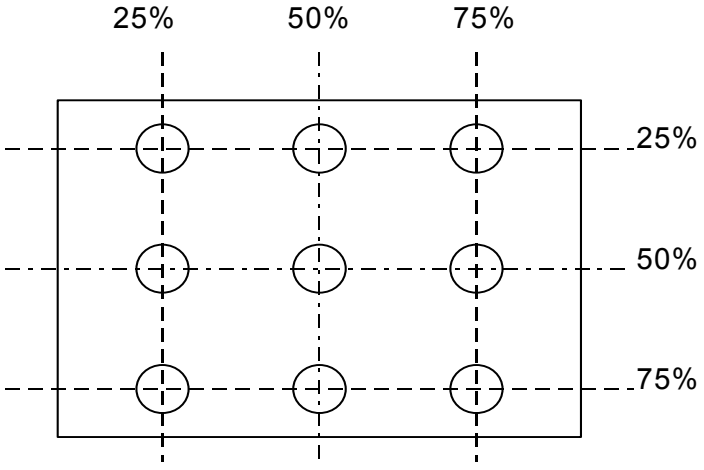
Luminance meter : BM-5A or BM-7 fast(TOPCON)

Measurement distance : 500 mm +/- 50 mm

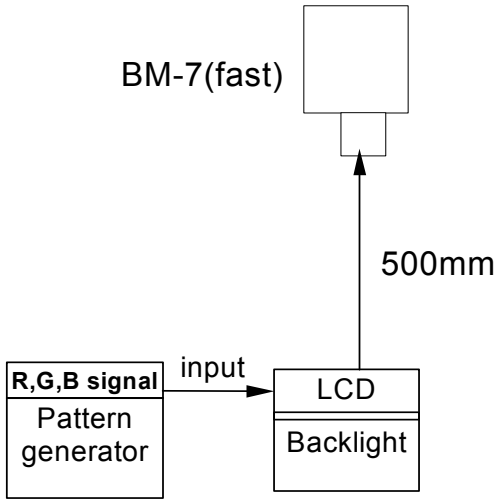
Ambient illumination : < 1 Lux

Measuring direction : Perpendicular to the surface of module

The test pattern is white (Gray Level 63).

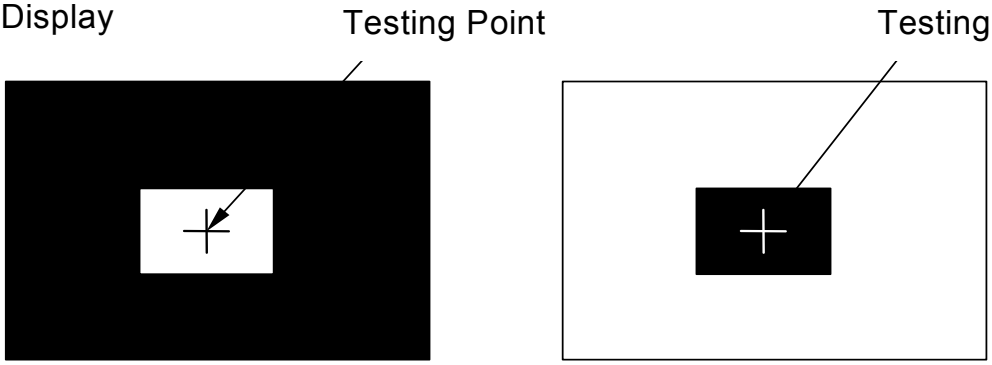


10-2) Testing configuration



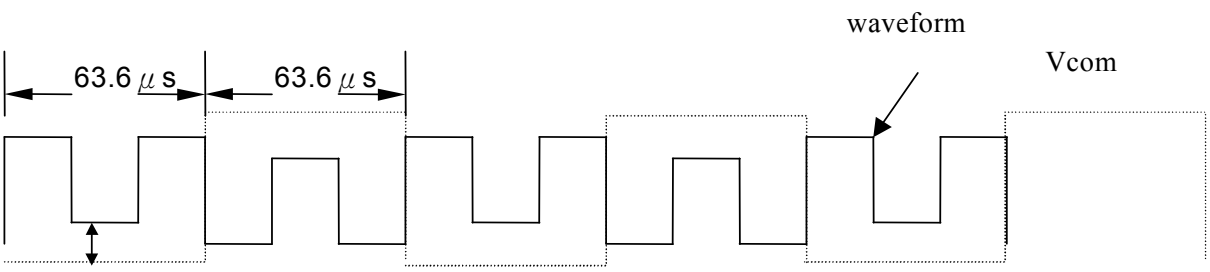
Caution: 1. Environmental illumination ≦ 1 lux
2. Before test CR, Vcom voltage must be adjusted carefully to get the best CR.

- LCD Display



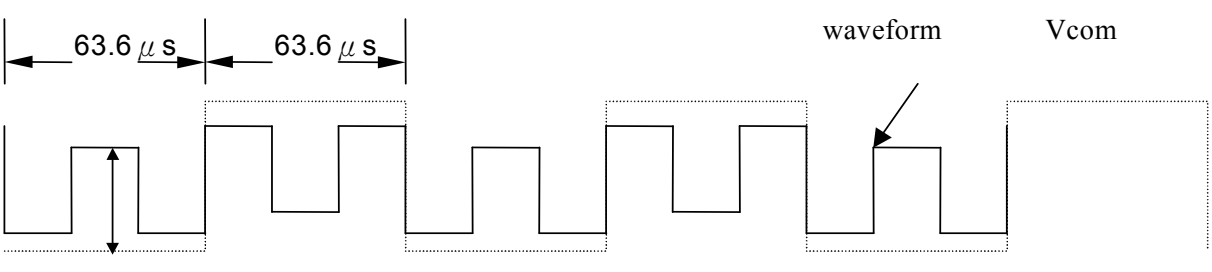
Pattern A Pattern B

- R, G, B Waveform of Pattern A at Testing Point



Vw=1.3V +/- 0.2V

- R, G, B Waveform of Pattern B at Testing Point



Vb=5.0V +/- 0.2V

11. Handling Cautions

11-1) Mounting of module

a)Please power off the module when you connect the input/output connector.

b)Please connect the ground pattern of the inverter circuit surely. If the connection is not perfect, some following problems may happen possibly.

1.The noise from the backlight unit will increase.

2.The output from inverter circuit will be unstable.

3.In some cases a part of module will heat.

c)Polarizer which is made of soft material and susceptible to flaw must be handled carefully.

d)Protective film (Laminator) is applied on surface to protect it against scratches and dirt.

e)Please following the tear off direction as figure11-1 to remove the protective film as slowly as possible, so that electrostatic charge can be minimized.

11-2) Precautions in mounting

a) When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.

b) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.

c) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.

d) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

11-3) Adjusting module

a) Adjusting volumes on the rear face of the module have been set optimally before shipment.

b) Therefore, do not change any adjusted values. If adjusted values are changed, the specifications described may not be satisfied.

11-4) Others

a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.

b) Store the module at a room temperature place.

c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.

d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.

e) Observe all other precautionary requirements in handling general electronic components.

f) Please adjust the voltage of common electrode as material of attachment by 1 module.

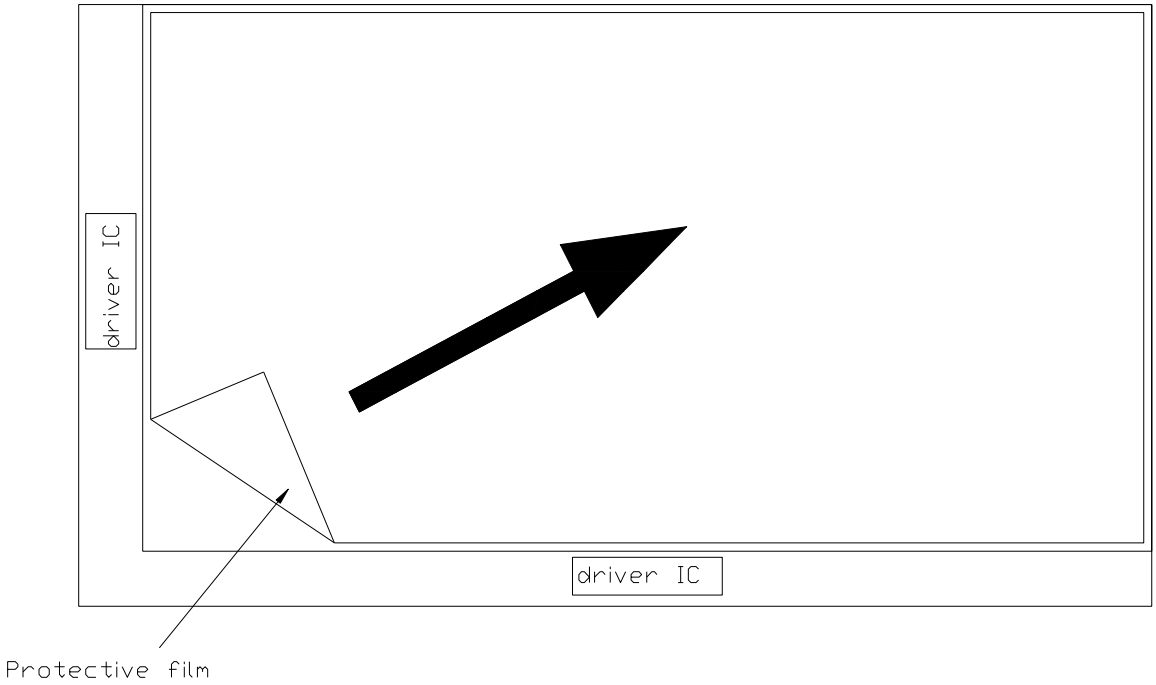


Figure 11-1 the way to peel off protective film

12. Reliability Test

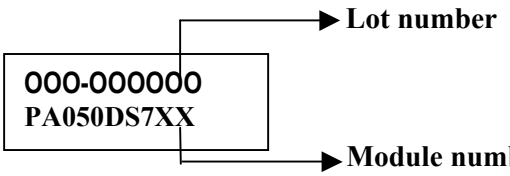
No	Test Item	Test Condition
1	High Temperature Storage Test	Ta = +80℃, 240 hrs
2	Low Temperature Storage Test	Ta = -30℃, 240 hrs
3	High Temperature Operation Test	Ta = +70℃, 240 hrs
4	Low Temperature Operation Test	Ta = -20℃, 240 hrs
5	High Temperature & High Humidity Operation Test	Ta = +60℃, 90%RH, 240 hrs
6	Thermal Cycling Test (non-operating)	-25℃→ +70℃, 200 Cycles 30 min 30 min
7	Vibration Test (non-operating)	Frequency：10 ~ 55 H_Z Amplitude：1.5 mm Sweep time: 11 mins Test Period : 6 Cycles for each direction of X, Y, Z
8	Shock Test (non-operating)	100G, 6ms Direction : ±X, ±Y, ±Z Cycle : 3 times
9	Electrostatic Discharge Test (non-operating)	150pF, 330Ω Air : ±15KV ; Contact : ±8KV 10 times/point, 5 points/panel face

Ta: ambient temperature

[Criteria]
Under the display quality test conditions with normal operation state, there should be no change which may affect practical display function.

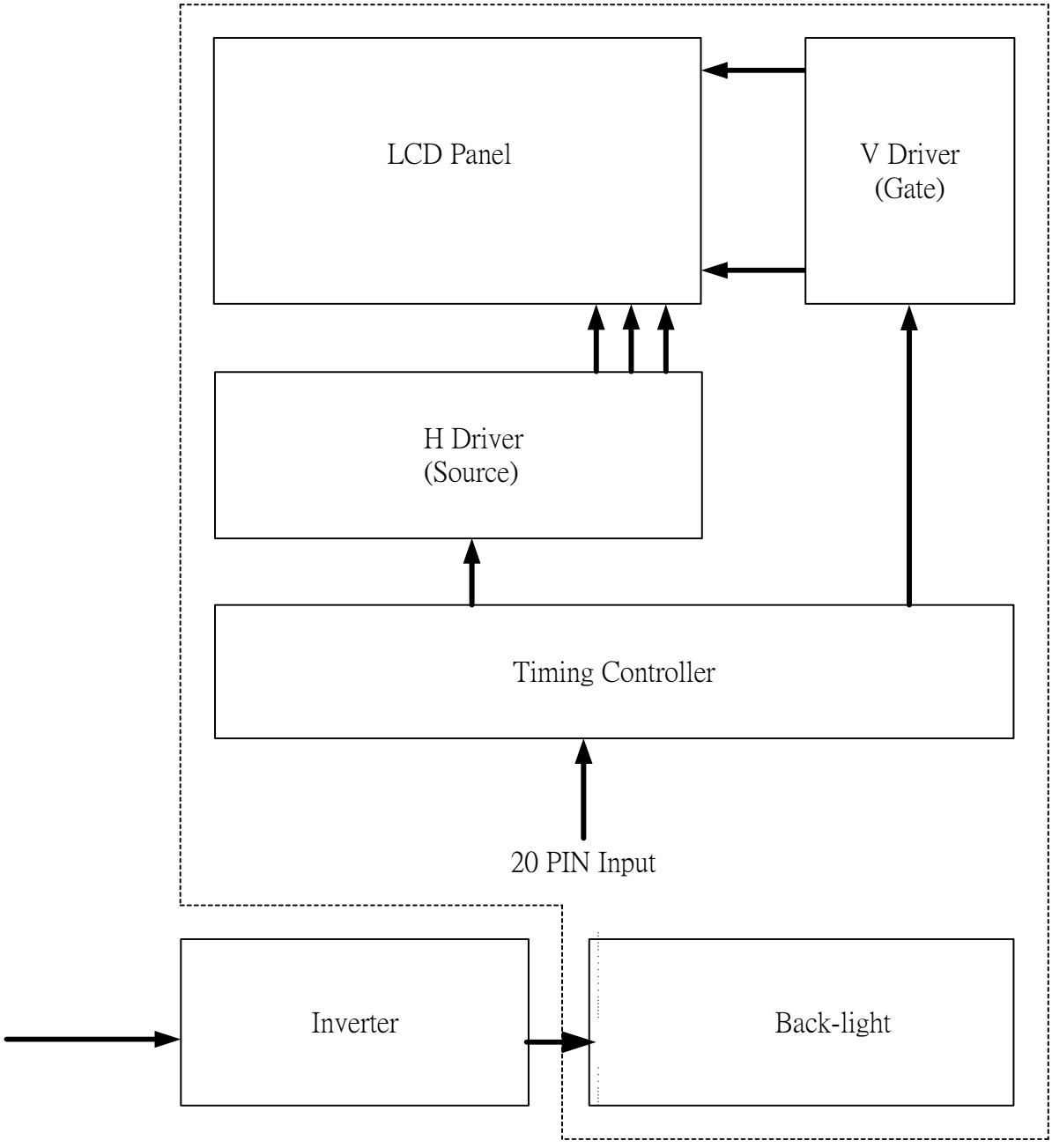
13. Indication of Lot Number Label

Indicated contents of the label



Contents of lot number : 1_{st}~3_{rd}—The OEM product
5_{th}—Production year : 1999⇒9, 2000⇒A, 2001⇒B……..
6_{th}—Production month : 1, 2, 3,….9, A, B, C
7_{th}~8_{th}—Production size : 5” ⇒50
9_{th}~10_{th}— Serial numbers : 01~99

14. Block Diagram



15. Packing