TECHNICAL SPECIFICATION

MODEL NO. : PA050XU4

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Please contact PVI or its agent for further information

☐Customer•s Confirmation

Customer _____

Date _____

By _____

☐PVI•s Confirmation

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Revision History

Rev.	Issued Date	Revised Contents
1.0	July.2,2007	New
2.0	March.24.2008	Add Page 23 11.Handling Cautions 11-1 item e)
3.0	Oct.22.2008	Page 5 4. Mechanical Drawing of TFT-LCD Module Add outline UL Label
4.0	Nov.13.2008	Modify Page 4 3.Mechanical Specifications Anti-Glare change to Anti-Glare + EWV Page 19 10.Optical Characteristics Viewing angle、Contrast

TECHNICAL SPECIFICATION

CONTENTS

1. Application

This technical specification applies to 5" color TFT-LCD module, PA050XU4. The applications of the panel are car TV, portable DVD, GPS, multimedia applications and others AV system..

2. Features

. Compatible with NTSC & PAL system

. Pixel in stripe configuration

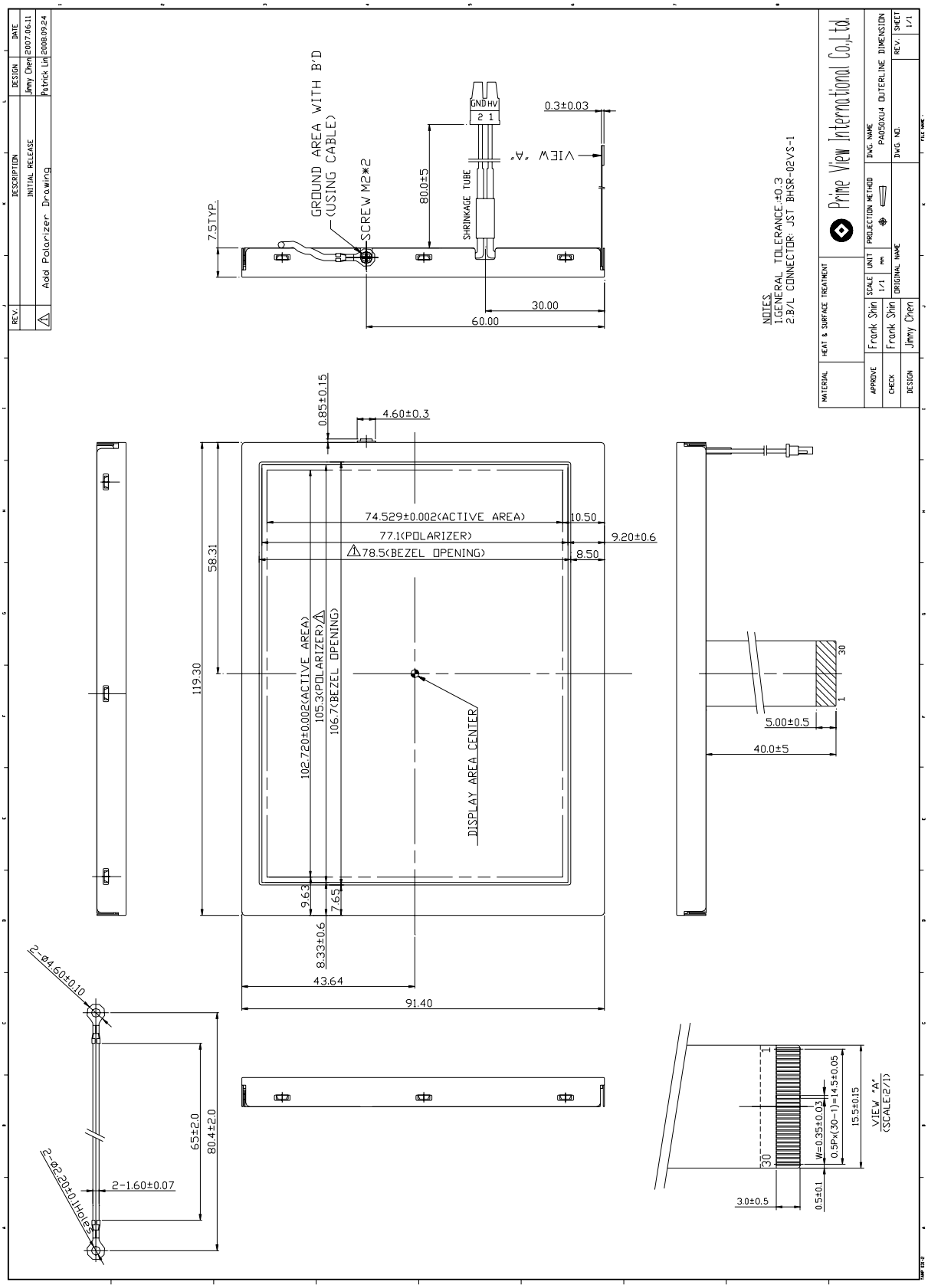
. Slim and compact

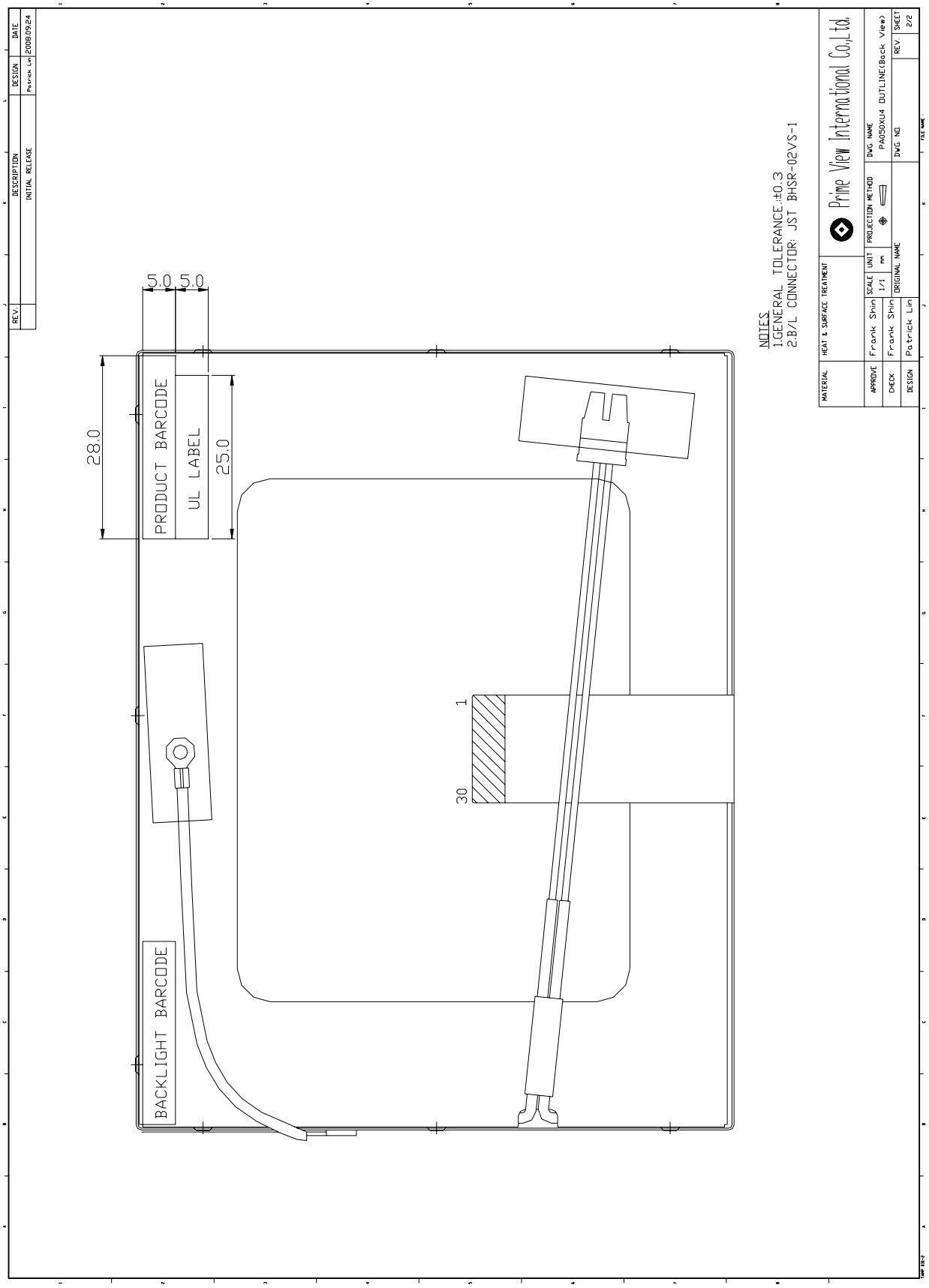
. Image Reversal : Up/Down and Left/Right

3. Mechanical Specifications

Parameter	Specifications	Unit
Screen Size	5 (diagonal)	Inch
Display Format	320×(RGB)×234	Dot
Active Area	102.72(H) × 74.529(V)	mm
Pixel Pitch	0.321 (H) × 0.3185 (V)	mm
Pixel Configuration	Stripe	-
Outline Dimension	119.3(W)× 91.4(H)× 7.5(D)(typ.)	mm
Surface Treatment	Anti – Glare+EWV	-
Back-light	CCFL	-
Weight	114±5	g
Display mode	Normal White	-
Gray scale inversion direction	6 o'clock [ref to Note 10-1]	-

4. Mechanical Drawing of TFT-LCD Module





5. Input / Output Terminals

TFT-LCD Module Connector
FPC Down Connect , 30Pins , Pitch : 0.5 mm

Pin No	Symbol	I/O	Description	Remark
1	DIO1	I/O	Vertical start pulse	Note 5 – 5
2	CPV	I	Shift clock for gate driver	-
3	VGL	I	Power for gate driver (AC voltage)	-
4	NC	-	No connection	-
5	VEE	I	Negative power for gate driver (DC voltage)	Note 5 - 2
6	NC	-	No connection	-
7	XOE	I	Output enable for gate driver	-
8	VSS	-	Ground for digital circuit	-
9	VCC	I	Supply voltage for logic control circuit for gate driver	Note 5 - 3
10	NC	-	No connection	-
11	VGH	I	Positive power for gate driver	Note 5 - 4
12	NC	-	No connection	-
13	U/D	I	Up/Down control for gate driver	Note 5 – 5
14	DIO2	I/O	Vertical start pulse	Note 5 – 5
15	VCOM	I	Common electrode voltage	Note 5 – 1
16	STH1	I/O	Start pulse for source driver	Note 5 – 5
17	VDD1	I	Supply power for digital circuit	Note 5 – 3
18	VSS1	-	Ground for digital circuit	-
19	VDD2	I	Supply power for analog circuit	Note 5 – 3
20	VSS2	-	Ground for analog circuit	-
21	R/L	I	Left/Right control for source driver	Note 5 – 5
22	VR	I	Video input R	Note 5 – 1
23	VG	I	Video input G	
24	VB	I	Video input B	
25	CPH1	I	Sampling and shift clock for source driver	Note 5 -- 6
26	CPH2	I	Sampling and shift clock for source driver	
27	CPH3	I	Sampling and shift clock for source driver	
28	STH2	I/O	Start pulse for source driver	Note 5 – 5
29	OEH	I	Output enable for source driver	-
30	NC	-	No connection	-

Note 5 – 1 : V_{COM} = $6V_{PP}$.

Phase of the video signal input and V_{COM}
The relation between these values could refer to 8-1 Operating condition.

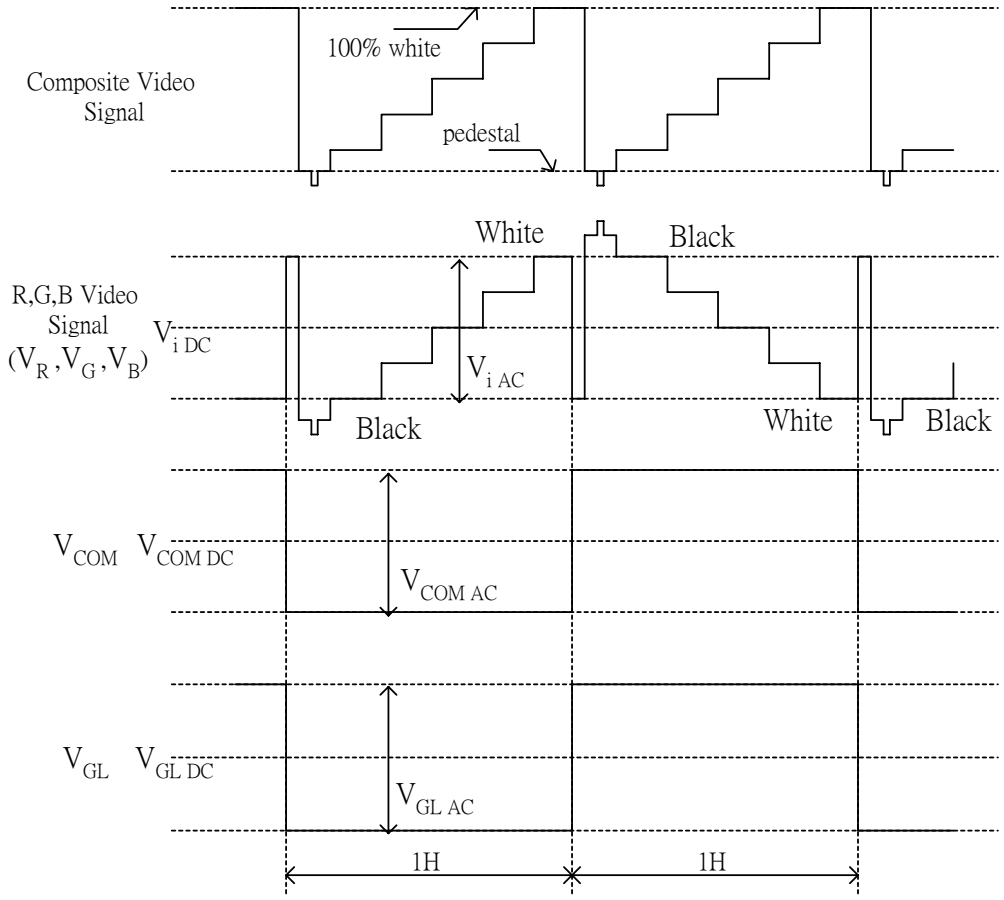


Fig.1

Liquid crystal transmission of the video signal input, V_{COM} and timing

	V_{COM}	
	H Level	L Level
Video Signal Input Maximum	Black	White
Video Signal Input Minimum	White	Black

White : maximum transmission / Black : minimum transmission

Note 5 – 2 : V_{EE} = -15V(Typ)

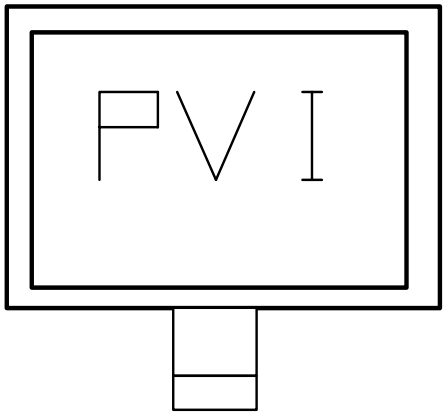
Note 5 – 3 : V_{DD1}, V_{CC} = +3.3V, V_{DD2} = +5V(Typ)

Note 5 – 4 : V_{GH} = +17V(Typ).

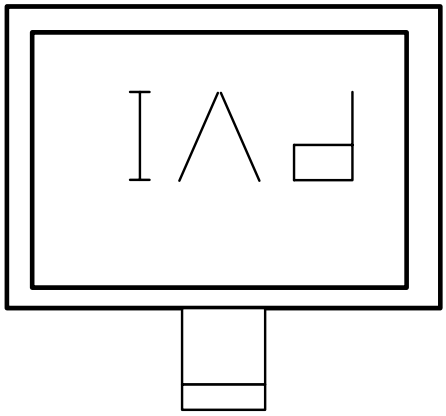
Note 5 – 5 : STH1, STH2 and R/L mode

R/L	STH1	STH2	Remark
High(VDD)	Input	Output	Left to Right
Low(0 Volt)	Output	Input	Right to Left

U/D (PIN 13) =High R/L (PIN 21) = High



U/D (PIN 13) =Low R/L (PIN 21) =Low

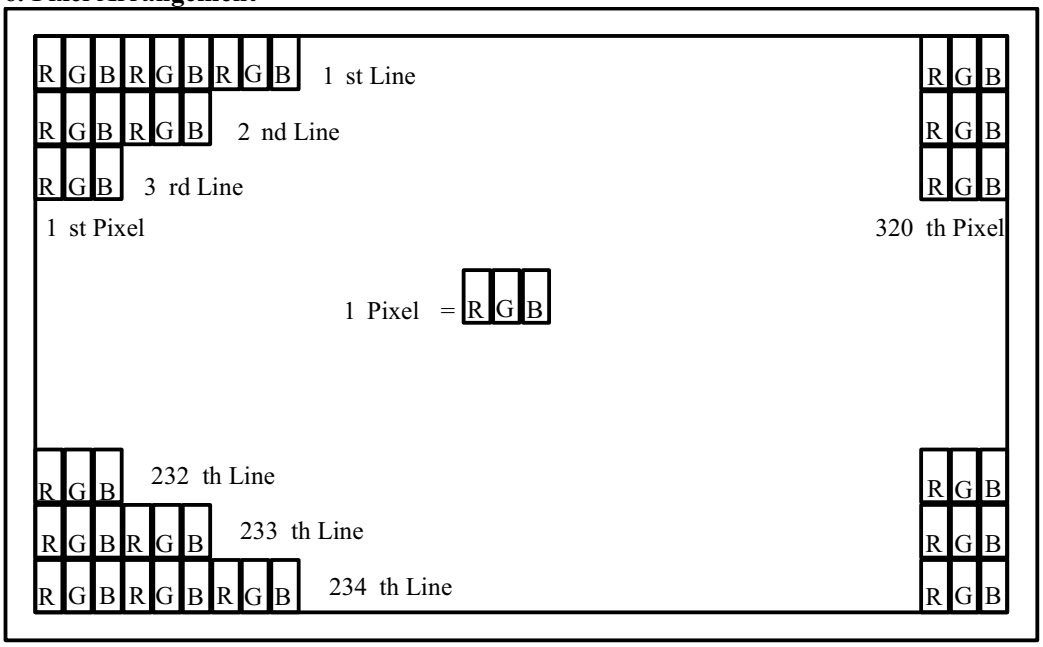


DIO1, DIO2, and U/D mode

U/D	DIO1	DIO2	Remark
High(VDD)	Input	Output	Up to Down
Low(0 Volt)	Output	Input	Down to Up

Note 5 – 6 : The CPH1 reference Fig.8-1 Sampling clock timing
CPH2 and CPH3 connect GND.

6. Pixel Arrangement



7. Absolute Maximum Ratings:

The followings are maximum values, which if exceeded, may cause faulty operation or damage to the unit.

GND = 0 V， Ta = 25 ℃

Parameter		Symbol	MIN.	MAX.	Unit	Remark
Supply Voltage For Source Driver		V_{DD2}	-0.3	+5.8	V	
		V_{DD1}	-0.3	+7.0	V	
Supply Voltage For Gate Driver		V_{CC}	-0.3	+6.0	V	
		V_{GH}-V_{EE}	-0.3	+40.0	V	
	H Level	V_{GH}	-0.3	+25.0	V	
	L Level	V_{EE}	-16	+0.3	V	

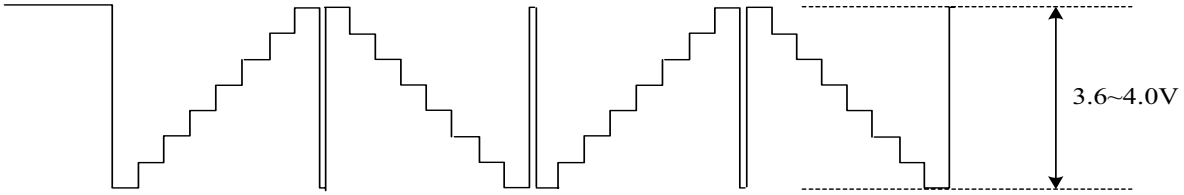
8. Electrical Characteristics

8-1) Operating Condition

Parameter		Symbol	MIN.	Typ.	MAX.	Unit	Remark
Supply Voltage For Source Driver	Analog	V_{DD2}	+4.5	+5.0	+5.5	V	
	Logic	V_{DD1}	+3.0	+3.3	+3.6	V	Depend on T/C signal voltage
			+4.5	5.0	5.5	V	
Supply Voltage For Gate Driver	V_{GH}		+15	+17	+19	V	
	$V_{GL\ DC}$		-13	-12	-11	V	DC Component of V_{GL}
	$V_{GL\ AC}$		-	+6.0	-	V_{P-P}	AC Component of V_{GL}
	Logic	V_{CC}	+3.0	+3.3	+3.6	V	Depend on T/C signal voltage
			+4.5	+5.0	+5.5	V	
Analog Signal input Level	V_{iAC}		-	4.0	-	V	Note 8-2
	V_{iDC}		-	2.5	-	V	
Digital input voltage	H level	V_{IH}	0.7 V_{DD1}	-	V_{DD1}	V	
	L level	V_{IL}	-0.3	-	0.3 V_{DD1}	V	
Digital output voltage	H level	V_{OH}	0.7 V_{DD1}	-	V_{DD1}	V	
	L level	V_{OL}	-0.3	-	0.3 V_{DD1}	V	
V_{COM}		$V_{COM\ AC}$	-	+6.0	-	V_{P-P}	AC Component of V_{COM}
		$V_{COM\ DC}$	-	2.2	-	V	DC Component of V_{COM} Note 8-1

Note 8-1 : PVI strongly suggests that the $V_{COM\ DC}$ level shall be adjustable , and the adjustable level range is 2.2±1V , every module's $V_{COM\ DC}$ level shall be carefully adjusted to show a best image performance.

Note 8-2: Both NTSC and PAL system Video Signal input waveform is based on 8 steps gray scale.



8-2) Current Consumption (GND=0V)

Ta= 25 ℃

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Current for Driver	I_{GH}	V_{GH}=+17V	-	0.1	0.3	mA	
	I_{GL}	V_{GL}=-12V	-	0.1	0.3	mA	V_{GL} center voltage
	I_{CC}	V_{CC}=+3.3V	-	0.1	0.3	mA	
	I_{DD1}	V_{DD1}=+3.3V	-	0.6	1.2	mA	
	I_{EE}	V_{EE}=-15V	-	0.1	0.2	mA	
	I_{DD2}	V_{DD2}=5V	-	3.2	6.4	mA	

8-3) Backlight driving & Power Consumption

Pin No	Symbol	Description	Remark
1	VL1	Input terminal (Hi voltage side)	
2	VL2	Input terminal (Low voltage side)	Note 8-3

Note 8-3 : Low voltage side of backlight inverter connects with Ground of inverter circuits.

Ta= 25 ℃

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Lamp voltage	V_L	392	427	480	Vrms	
Lamp current	I_L	3	6	8	mA	Note 8-4
Lamp frequency	P_L	40	43	80	KHz	Note 8-5
Starting voltage(25℃) (Reference Value)	Vs	-	-	890	Vrms	Note 8-6
Starting voltage(0℃) (Reference Value)	Vs	-	-	1180	Vrms	Note 8-6

Note 8-4 : In order to satisfy the quality of B/L , no matter use what kind of inverter , the output lamp current must between Min. and Max. to avoid the abnormal display image caused by B/L.

Note 8-5 : The waveform of lamp driving voltage should be as closed to a perfect SIN wave as possible.

Note 8-6 : The "Max of kick off voltage" means the minimum voltage of inverter to turn on the CCFL and it should be applied to the lamp for more than 1 second to start up. Otherwise the lamp may not be turned on.

Power Consumption Ta= 25 ℃

Parameter	Symbol	Conditions	TYP.	Unit	Remark
LCD Panel Power Consumption	-	-	22.7	mW	Note 8-7
Backlight Lamp Power Consumption	-	-	2.5	W	Note 8-8
Total Power Consumption	-	-	2.6	W	

Note 8-7：The power consumption for backlight is not included.

Note 8-8：Backlight lamp power consumption is calculated by $I_L \times V_L$.

8-4) Input / Output Connector

1. Backlight Connector
   JST BHSR-02VS-1,
   Pin No. : 2
   Pitch : 3.5 mm

8-5) Timing Characteristics of Input Signals

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Remark
Rising time	t_r	-	-	10	ns	
Falling time	t_f	-	-	10	ns	
High and low level pulse width	t_{CPH}	147	156	166	ns	CPH1
CPH pulse duty	t_{CWH}	30	50	70	%	CPH1
STH setup time	t_{SUH}	20	-	-	ns	STH1,STH2
STH hold time	t_{HDH}	20	-	-	ns	STH1,STH2
STH pulse width	t_{STH}	-	1	-	t_{CPH}	STH1,STH2
STH period	t_H	61.5	63.5	65.5	μs	STH1,STH2
OEH pulse width	t_{OEH}	-	1.6	-	μs	OEH
Sample and hold disable time	t_{DIS1}	-	4.4	-	μs	
OEV pulse width	t_{OEV}	-	12	-	μs	XOE
CKV pulse width	t_{CKV}	-	32	-	μs	CPV
Clean enable time	t_{DIS2}	-	6	-	μs	
Horizontal display timing range	t_{DH}	-	960	-	t_{CPH}/3	
STV setup time	t_{SUV}	400	-	-	ns	DIO1,DIO2
STV hold time	t_{HDV}	400	-	-	ns	DIO1,DIO2
STV pulse width	t_{STV}	-	-	1	t_H	DIO1,DIO2
Horizontal lines per field	t_V	256	262	268	t_H	
Vertical display start	t_{SV}		3	-	t_H	
Vertical display timing range	t_{DV}		234	-	t_H	
VCOM rising time	t_{rCOM}		-	5	μs	
VCOM falling time	t_{fCOM}		-	5	μs	
VCOM delay time	t_{DCOM}		-	3	μs	
RGB delay time	t_{DRGB}		-	1	μs	

8 -6) Signal Timing Waveforms

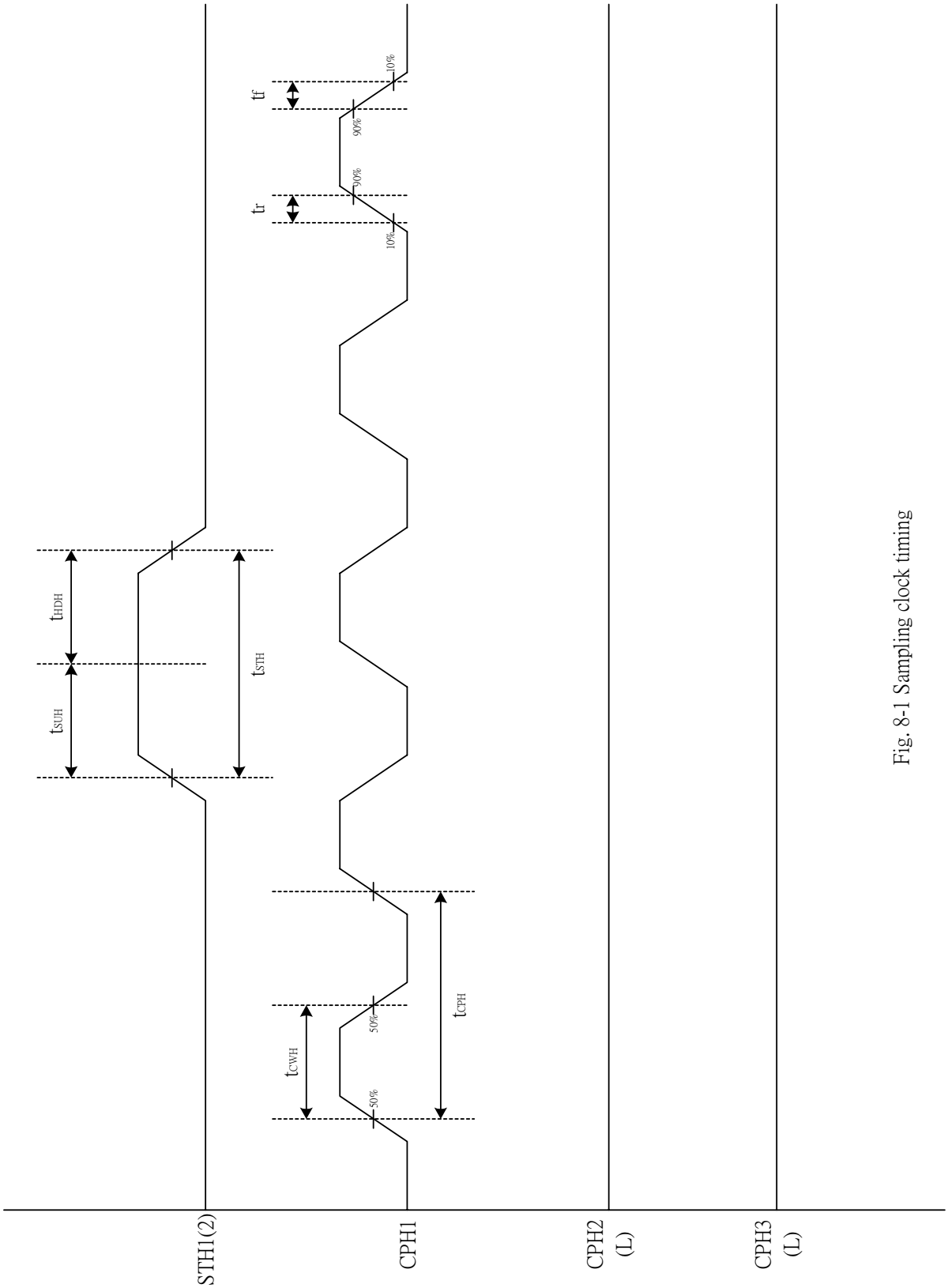


Fig. 8-1 Sampling clock timing

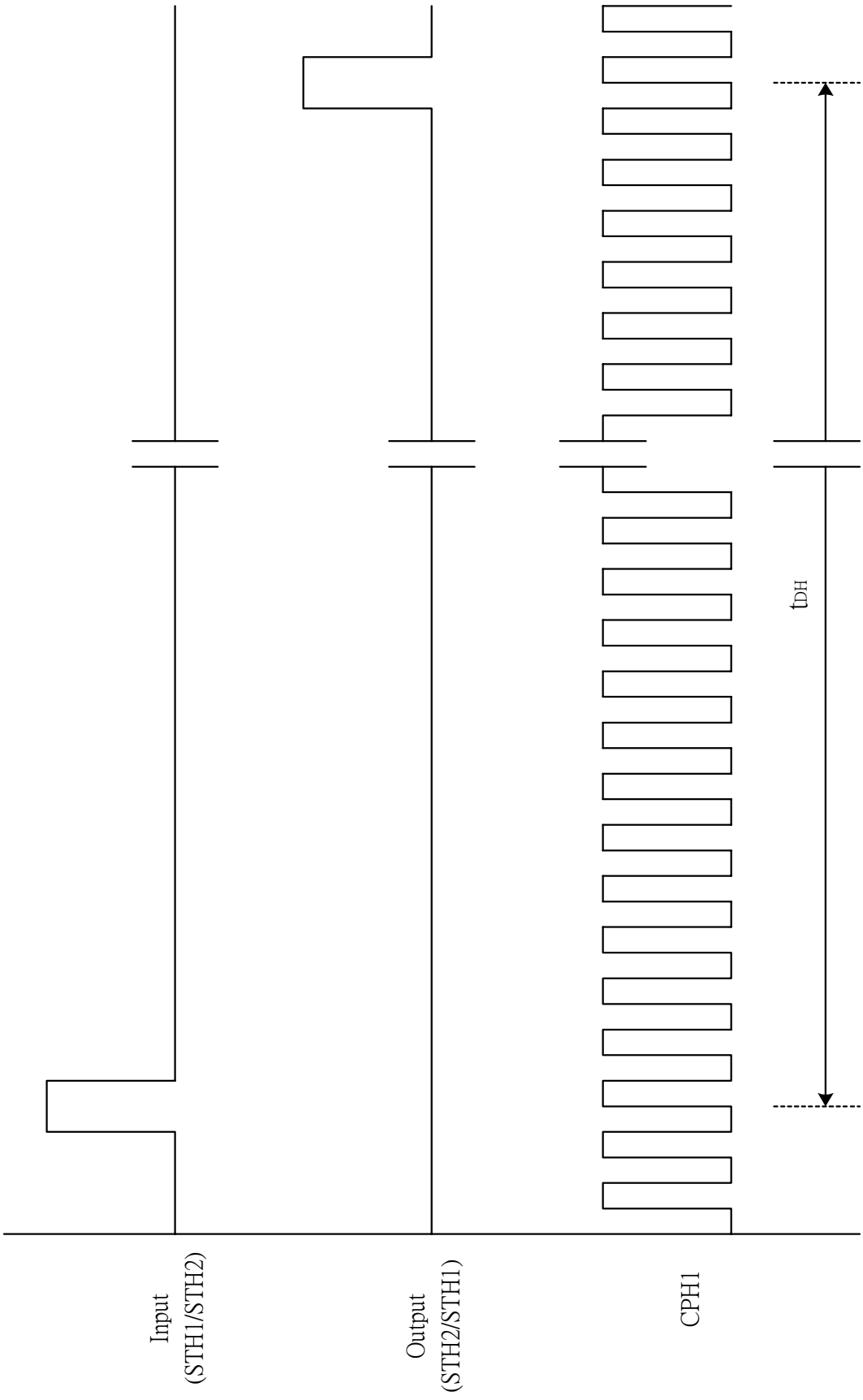


Fig. 8-2 Horizontal display timing range

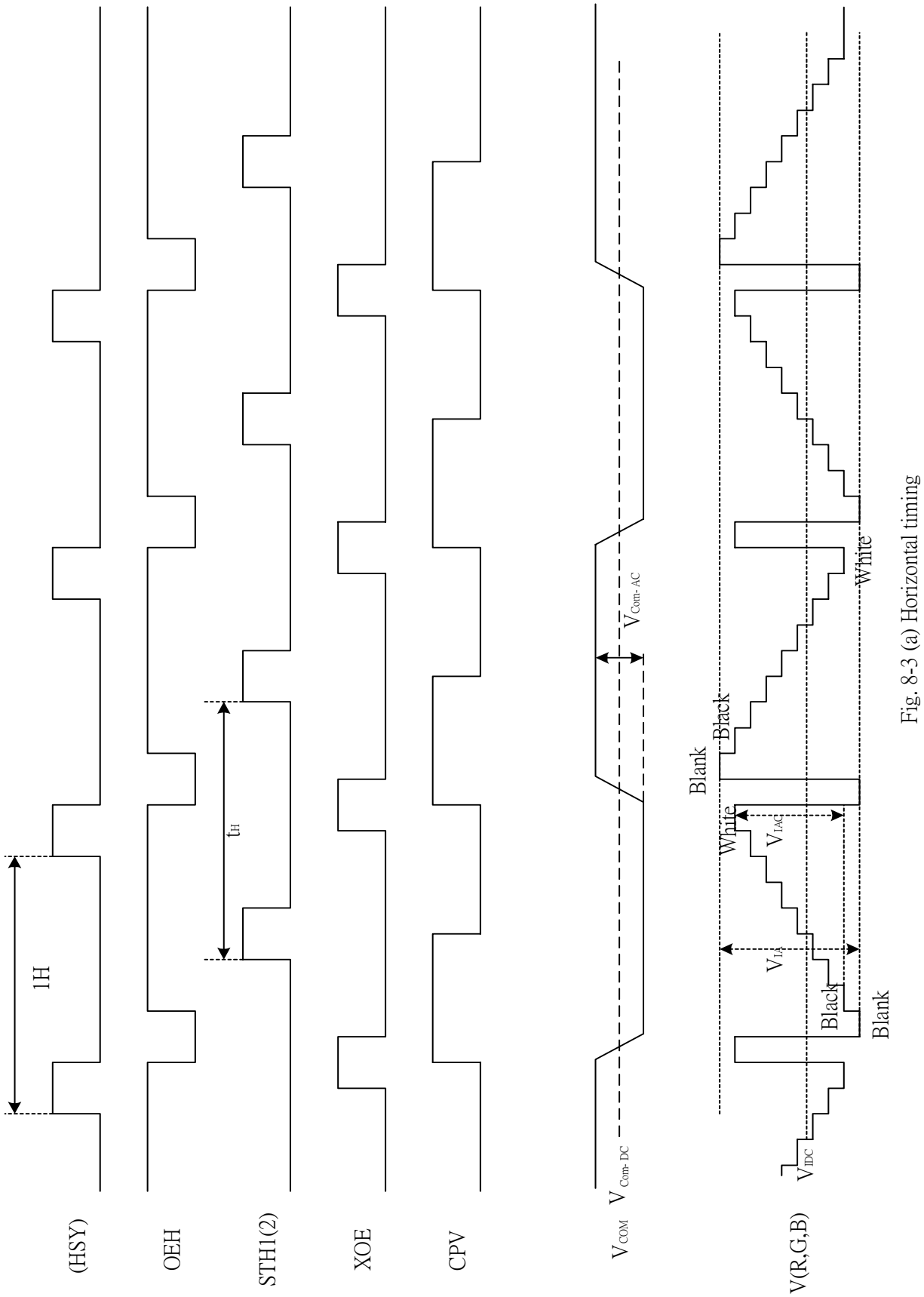
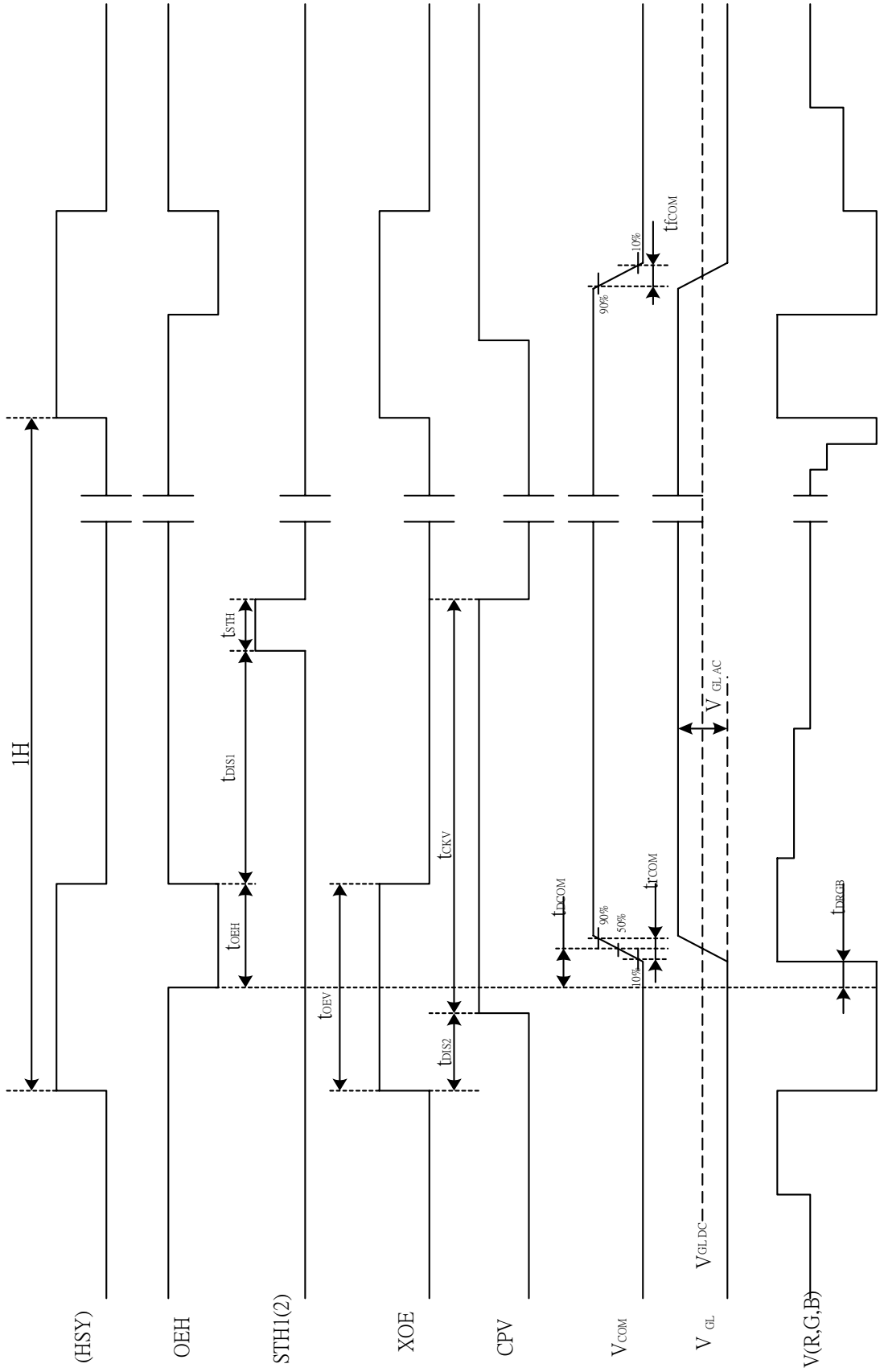


Fig. 8-3 (a) Horizontal timing



Note : The falling edge of OEV should be synchronized with the falling edge of OEH

Fig. 8-3 (b) Detail horizontal timing

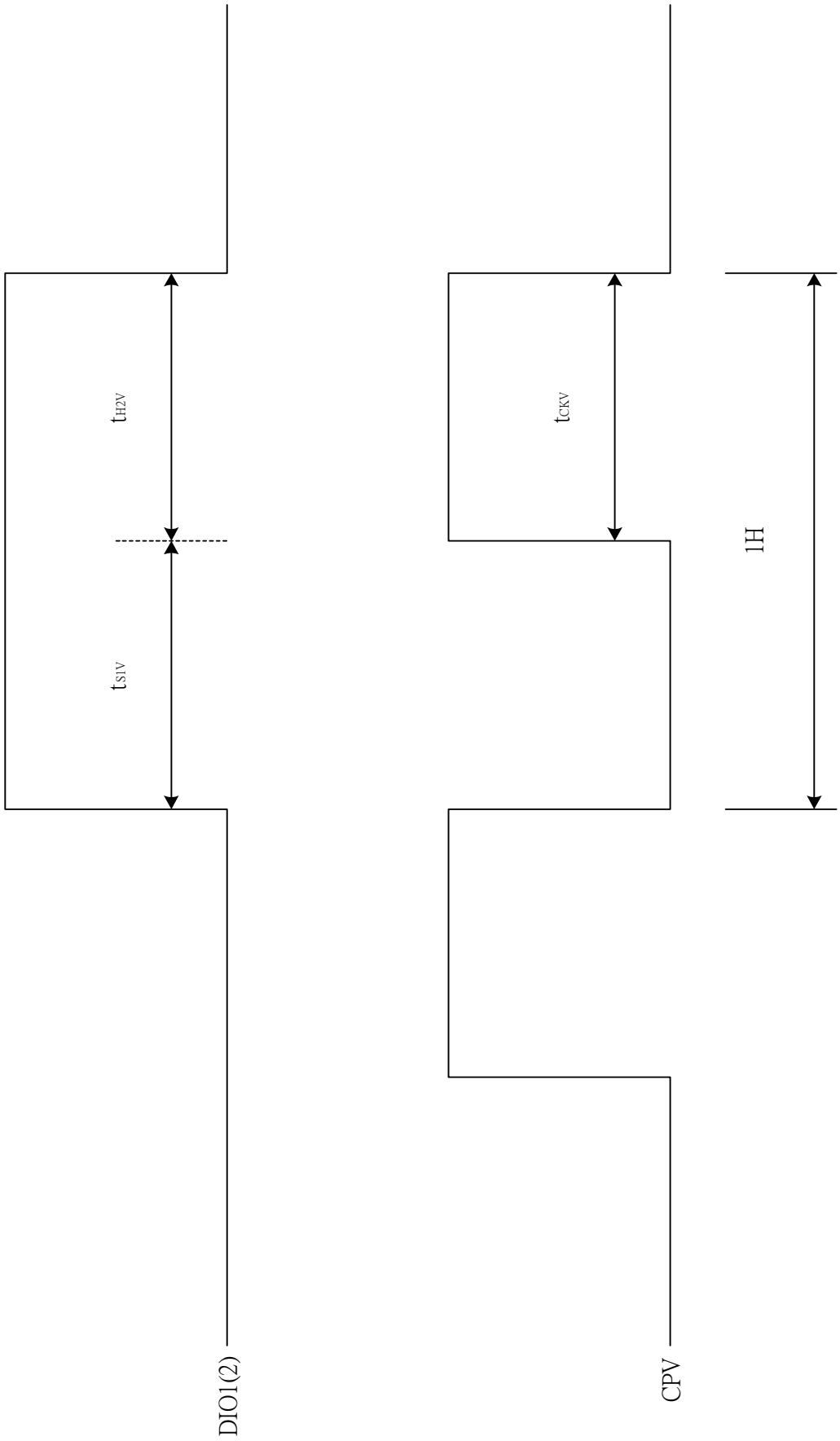


Fig. 8-4 Vertical shift clock timing

Vertical timing (From up to down)

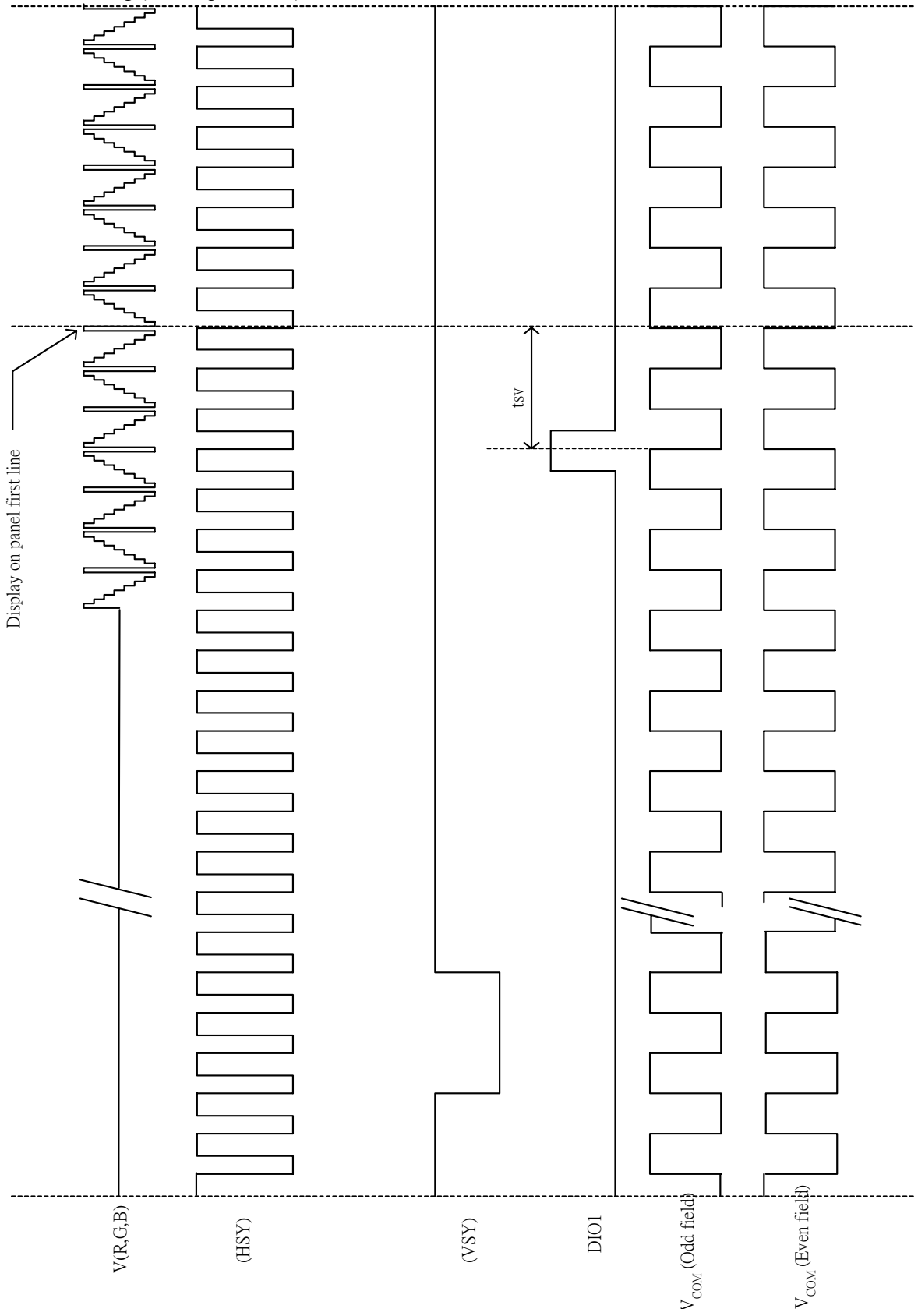


Fig. 8-5 (a) Vertical timing (From Up to Down)

Vertical timing (From down to up)

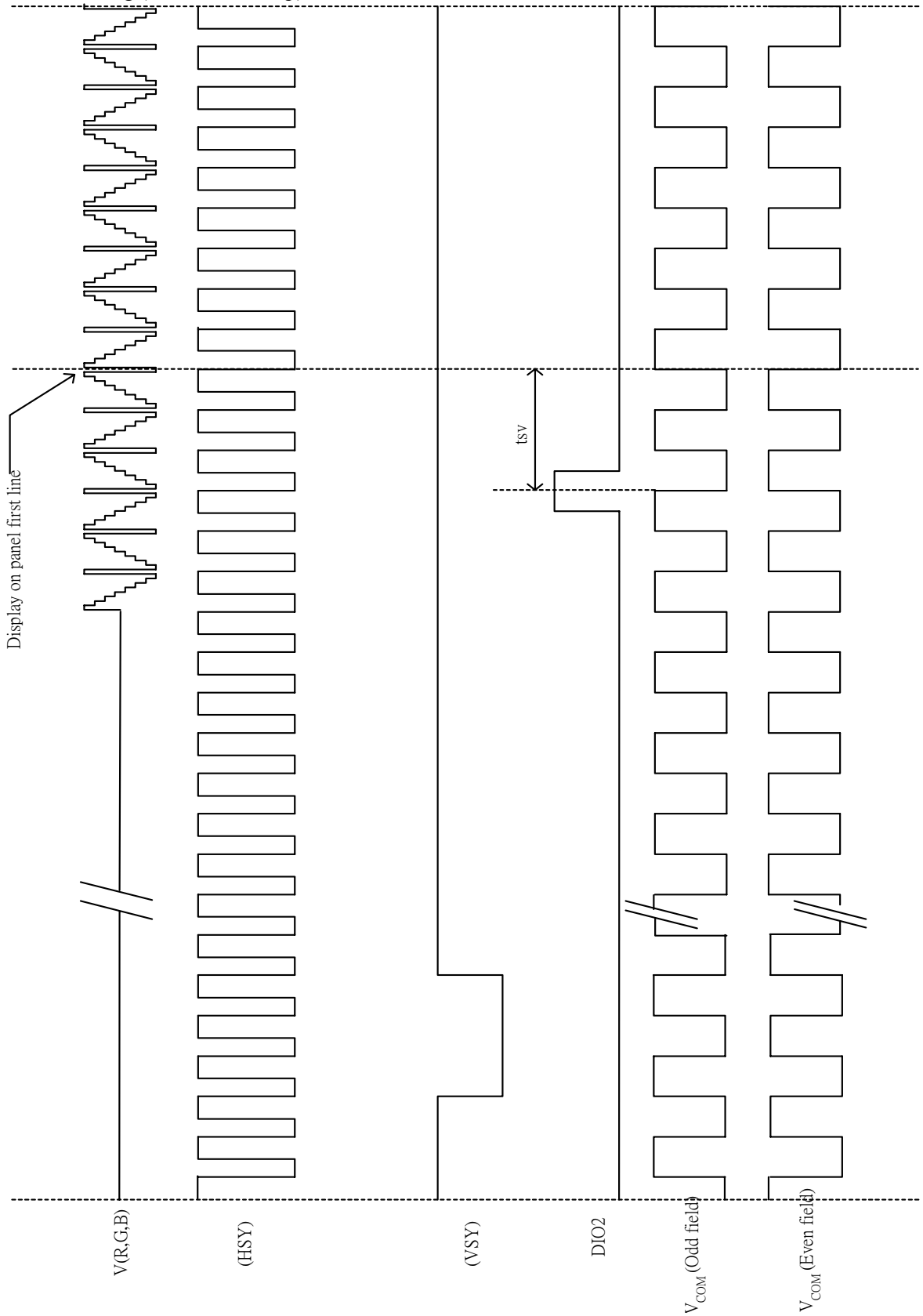
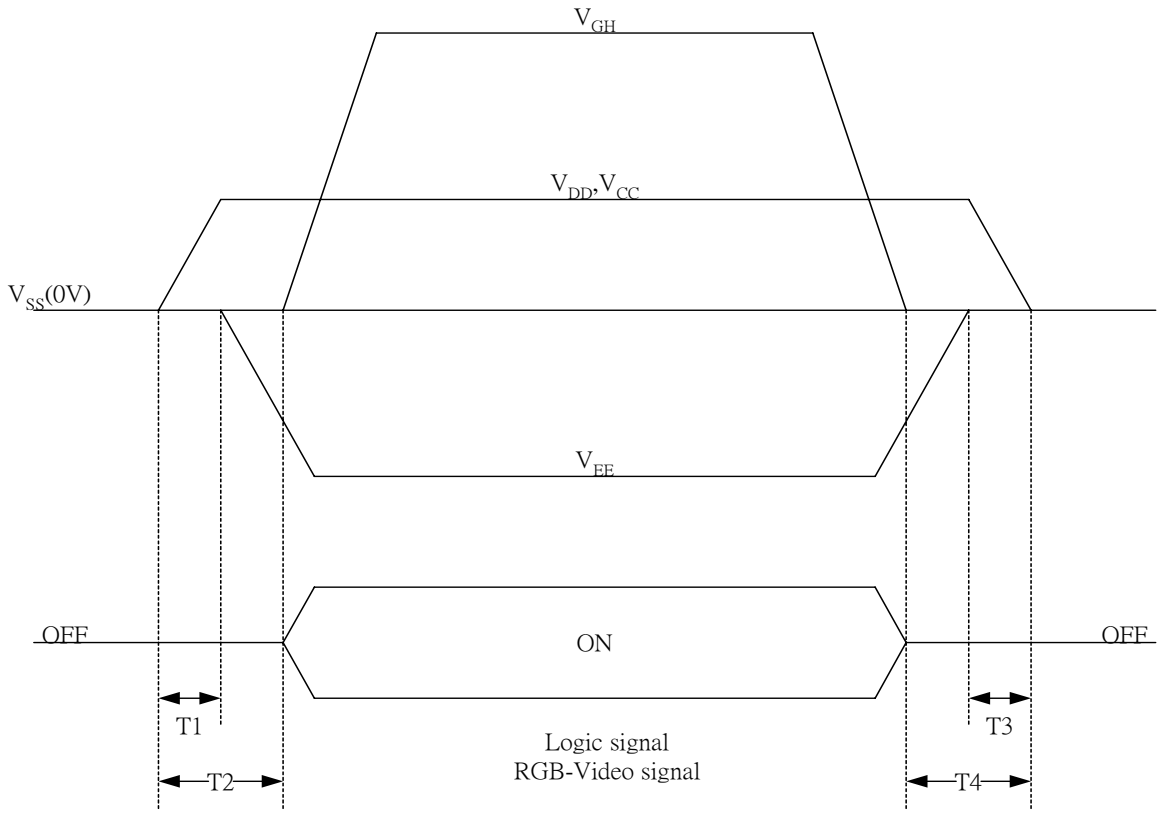


Fig. 8-5 (b) Vertical timing (From Down to Up)

9. Power On Sequence



1) 10ms≦T1<T2
2) 0ms<T3≦T4≦10ms

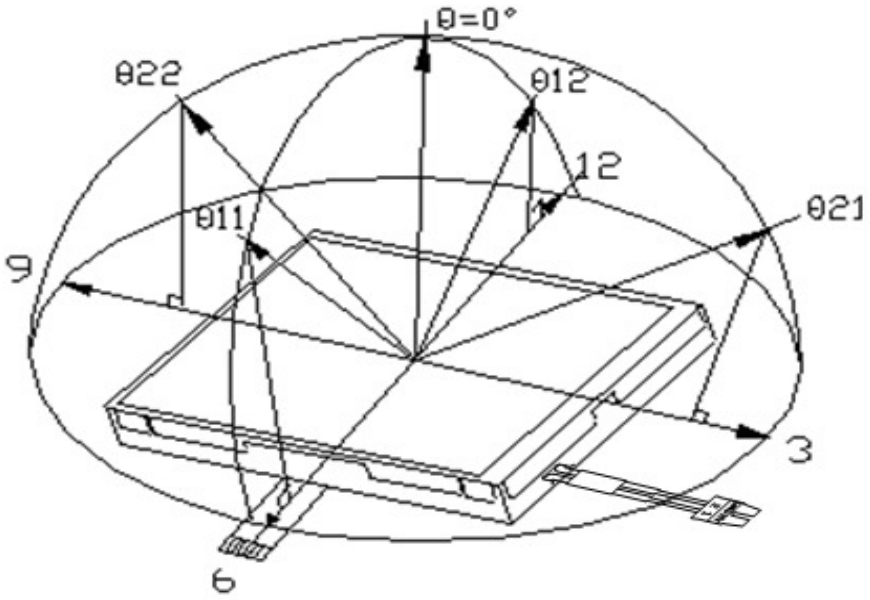
10. Optical Characteristics

10-1) Specification:

Ta = 25℃

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	θ21, θ22	CR≧10	65	70	---	deg	Note 10-1
	Vertical	θ11		55	60	---	deg	Note 10-1
		θ12		35	40	---	deg	Note 10-1
Contrast Ratio		CR	At optimized Viewing angle	200	400	---	-	Note 10-2
Response time	Rise	Tr	θ=0°	---	15	30	ms	Note 10-4
	Fall	Tf		---	30	50	ms	
Uniformity		U	-	70	80	---	%	Note 10-5
Brightness		L	-	350	400	---	cd/㎡	Note 10-3
White Chromaticity		x	θ=0°	0.270	0.300	0.330	-	Note 10-3
		y	θ=0°	0.320	0.350	0.380	-	
Lamp Life Time		-	+25℃	50000	-	-	hr	

Note 10-1 : The definitions of viewing angles



Note 10-2 : CR = $\frac{\text{Luminance when Testing point is White}}{\text{Luminance when Testing point is Black}}$

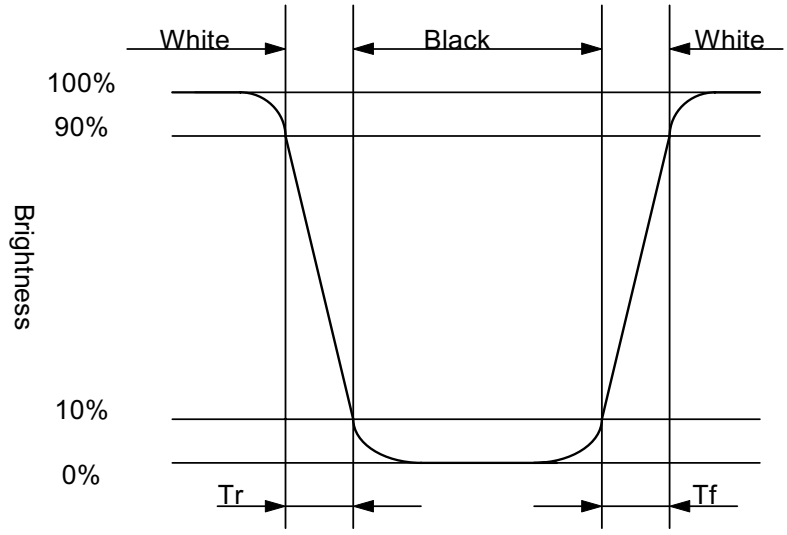
(Testing configuration see 10-2)

Contrast Ratio is measured in optimum common electrode voltage.

Note 10-3 : Topcon BM-7(fast) luminance meter 1° field of view is used in the testing (after 20~30 minutes operation).

Lamp Current 6mA

Note 10-4 : The definition of response time :



Note 10-5: The uniformity of LCD is defined as

$$U = \frac{\text{The Minimum Brightness of the 9 testing Points}}{\text{The Maximum Brightness of the 9 testing Points}}$$

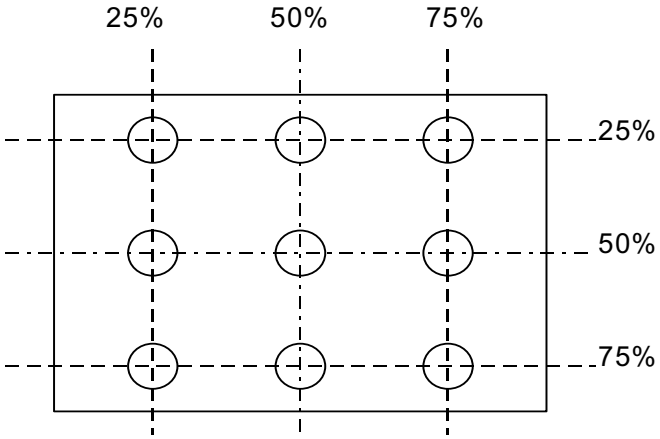
Luminance meter : BM-5A or BM-7 fast(TOPCON)

Measurement distance : 500 mm +/- 50 mm

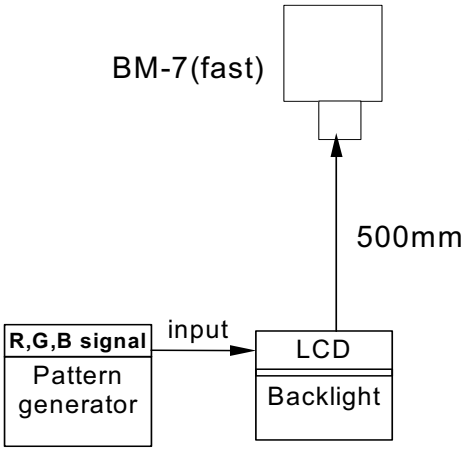
Ambient illumination : < 1 Lux

Measuring direction : Perpendicular to the surface of module

The test pattern is white (Gray Level 63).

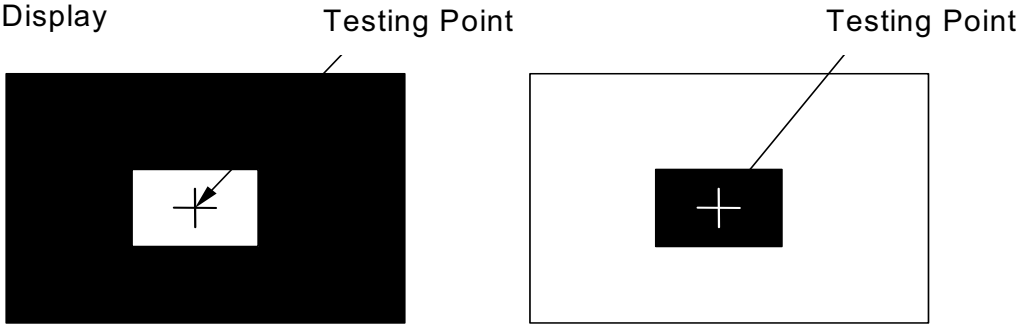


10-2) Testing configuration



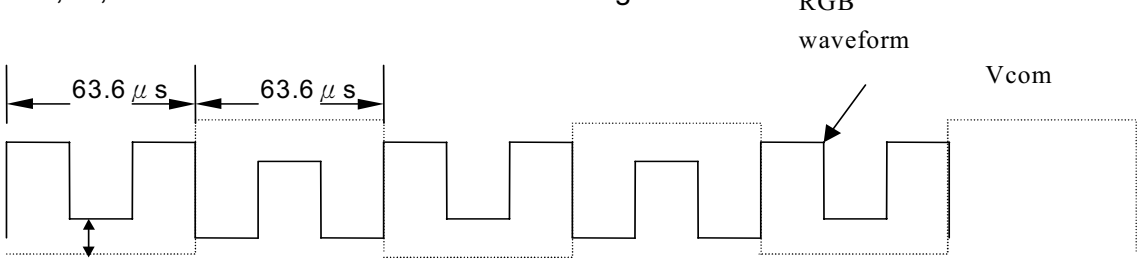
Caution: 1. Environmental illumination ≦ 1 lux
2. Before test CR, Vcom voltage must be adjusted carefully to get the best CR.

- LCD Display



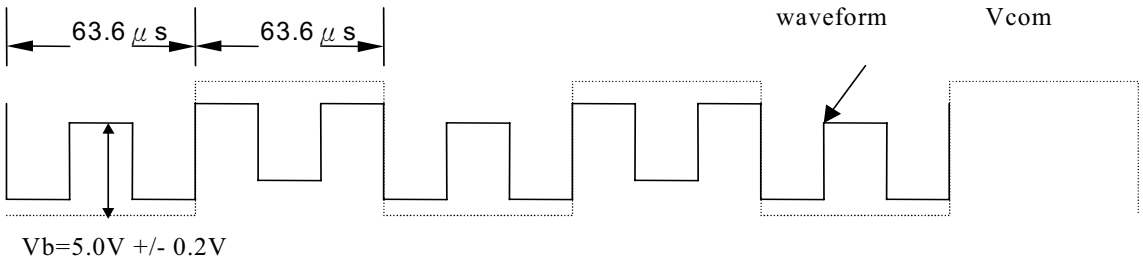
Pattern A Pattern B

- R, G, B Waveform of Pattern A at Testing Point



Vw=1.3V +/- 0.2V

- R, G, B Waveform of Pattern B at Testing Point



Vb=5.0V +/- 0.2V

11. Handling Cautions

11-1) Mounting of module

a) Please power off the module when you connect the input/output connector.

b) Please connect the ground pattern of the inverter circuit surely. If the connection is not perfect, some following problems may happen possibly.

1. The noise from the backlight unit will increase.
2. The output from inverter circuit will be unstable.
3. In some cases a part of module will heat.

c)Polarizer which is made of soft material and susceptible to flaw must be handled carefully.

d)Protective film (Laminator) is applied on surface to protect it against scratches and dirt.

e)Please following the tear off direction as figure11-1 to remove the protective film as slowly as possible, so that electrostatic charge can be minimized.

11-2) Precautions in mounting

a) When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.

b) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.

c) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.

d) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

11-3) Adjusting module

a) Adjusting volumes on the rear face of the module have been set optimally before shipment.

b) Therefore, do not change any adjusted values. If adjusted values are changed, the specifications described may not be satisfied.

11-4) Others

a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.

b) Store the module at a room temperature place.

c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.

d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.

e) Observe all other precautionary requirements in handling general electronic components.

f) Please adjust the voltage of common electrode as material of attachment by 1 module.

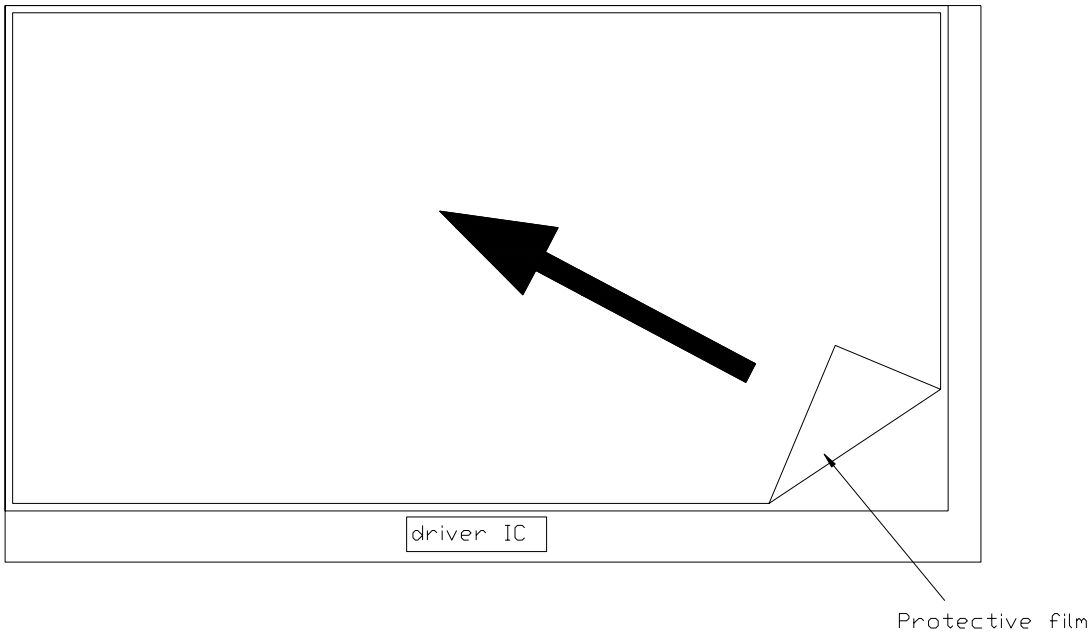


Figure 11-1 the way to peel off protective film

12. Reliability Test

No	Test Item	Test Condition
1	High Temperature Storage Test	Ta = +80℃, 240 hrs
2	Low Temperature Storage Test	Ta = -30℃, 240 hrs
3	High Temperature Operation Test	Ta = +70℃, 240 hrs
4	Low Temperature Operation Test	Ta = -20℃, 240 hrs
5	High Temperature & High Humidity Operation Test	Ta = +60℃, 90%RH, 240 hrs
6	Thermal Cycling Test (non-operating)	-25℃ → +70℃, 200 Cycles 30 min 30 min
7	Vibration Test (non-operating)	Frequency：10 ~ 55 H_Z Amplitude：1.5 mm Sweep time: 11 mins Test Period : 6 Cycles for each direction of X, Y, Z
8	Shock Test (non-operating)	100G, 6ms Direction : ±X, ±Y, ±Z Cycle : 3 times
9	Electrostatic Discharge Test (non-operating)	200pF, 0Ω ±200V 1 time / each terminal

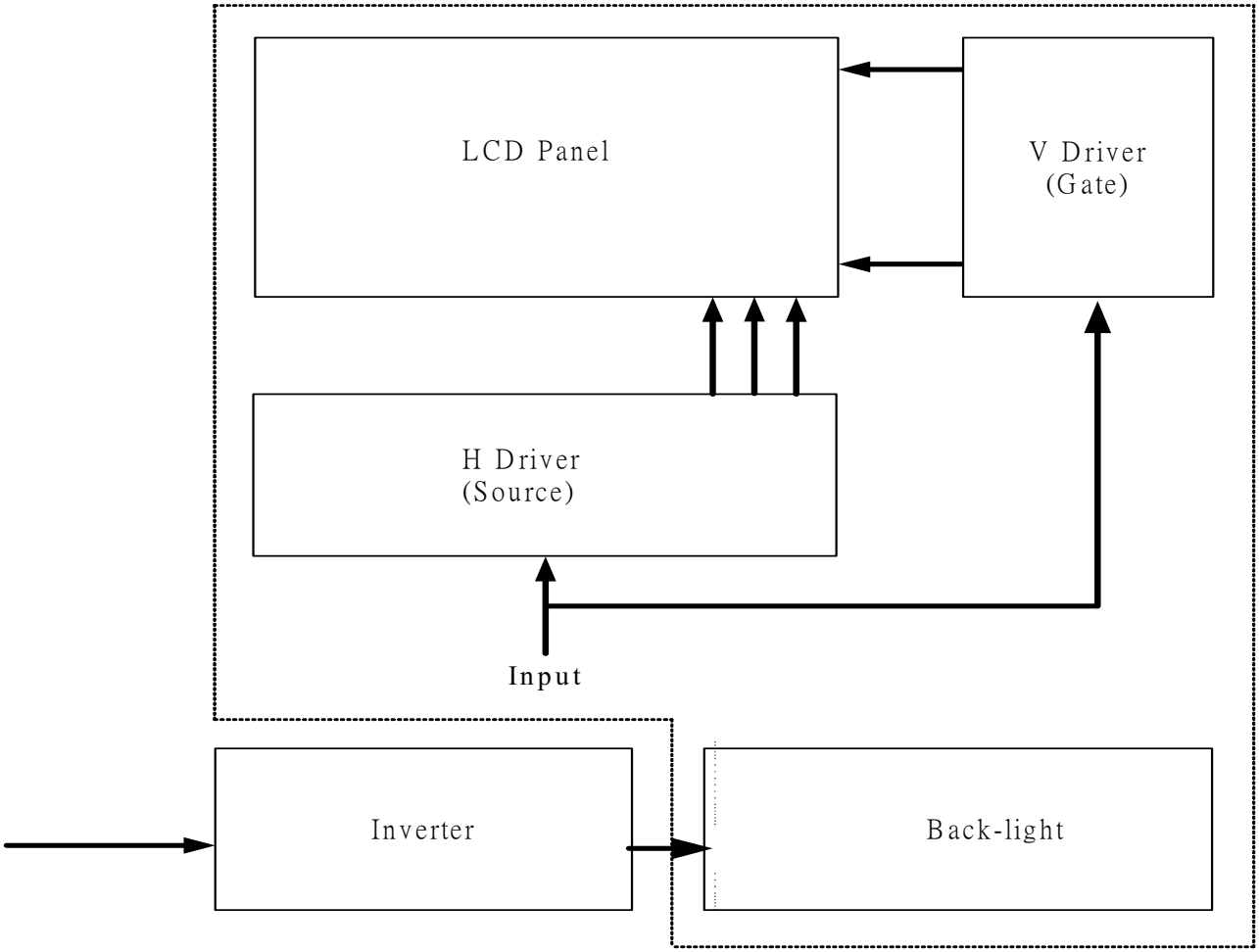
Ta: ambient temperature

[Criteria]

In the standard conditions, there is not display function NG issue occurred. (including :line defect ,no image)

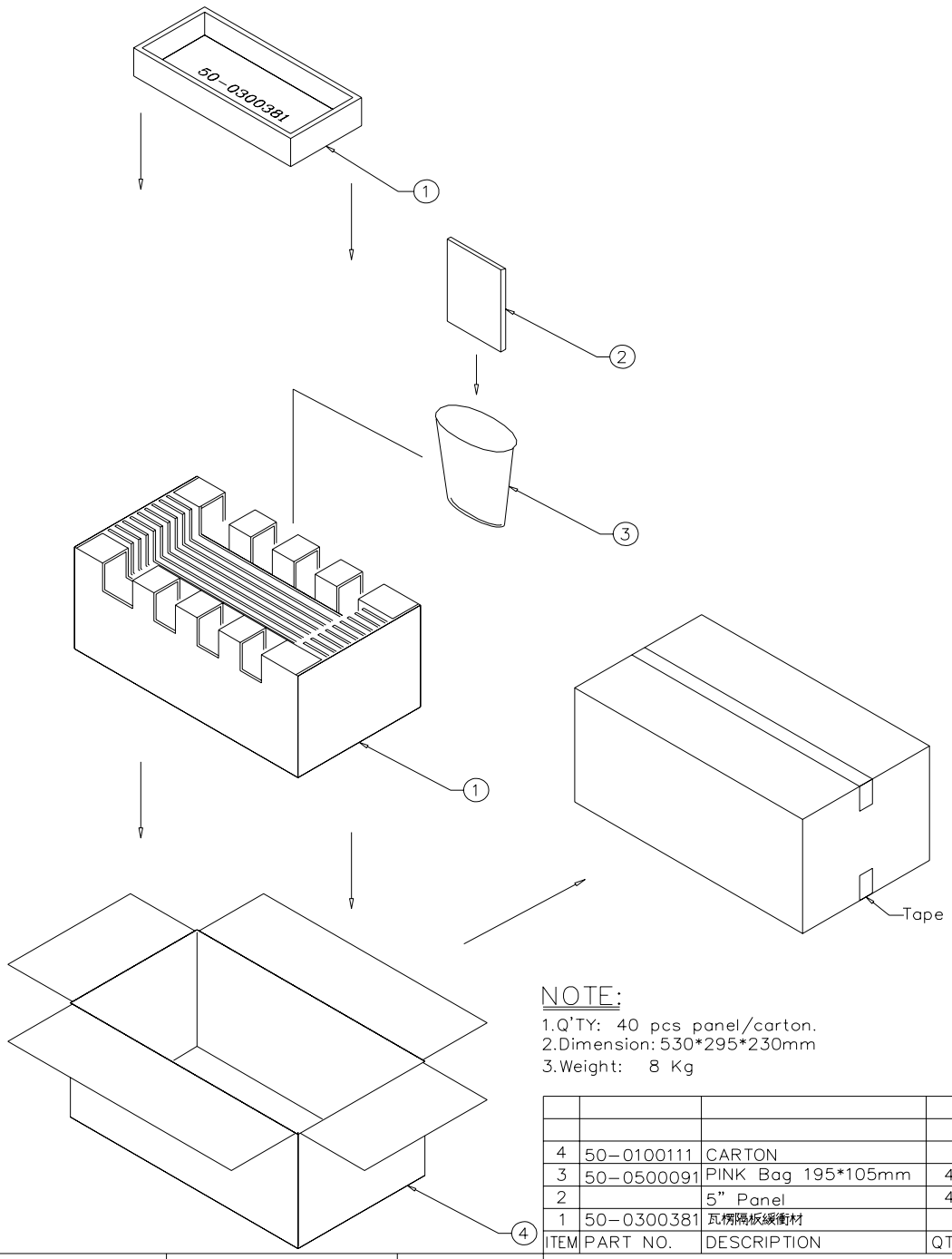
All the cosmetic specification is judged before the reliability stress

13. Block Diagram



14. Packing

ZONE	REV.	DOCUUMENT NO.	DESCRIPTION	DATE	REV.BY



NOTE:
1.Q'TY: 40 pcs panel/carton.
2.Dimension: 530*295*230mm
3.Weight: 8 Kg

ITEM	PART NO.	DESCRIPTION	QTY	REMARK
4	50-0100111	CARTON	1	
3	50-0500091	PINK Bag 195*105mm	40	抗靜電
2		5" Panel	40	
1	50-0300381	瓦楞隔板緩衝材	1	上蓋+ 底座

MTL.SPEC.	UNSPECIFIED TOL'S ANGLE ROUGHNESS	REMARK

元太科技工業股份有限公司
Prime View International Co., Ltd.

APPROVE	Franks	'03.03.17	SCALE	UNIT	SHEET 1 OF 1	DWG.TITLE: 5" Model Packing Draw
CHECK	Franks	'03.03.17				
DRAWN	Jimmyc	'03.03.17	MTL.NO.	DWG FILE:	REV. 01	A4 SIZE