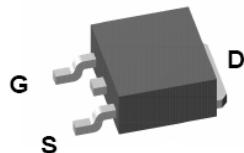


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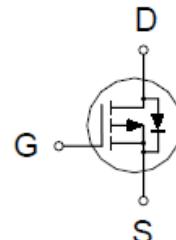
P-Channel Enhancement Mode MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
-20V	115mΩ @ $V_{GS} = -4.5V$	-10A



TO-252



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 12	
Continuous Drain Current $T_C = 25^\circ C$	I_D	-10	A
		-6.2	
Pulsed Drain Current ¹	I_{DM}	-24	
Power Dissipation $T_C = 25^\circ C$	P_D	25	W
		9.6	
Operating Junction & Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta JC}$		5	°C / W
Junction-to-Ambient	$R_{\theta JA}$		110	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

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P-Channel Enhancement Mode MOSFET

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = -250\mu\text{A}$	-20			V
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}, I_D = -250\mu\text{A}$	-0.45	-0.8	-1.2	
Gate-Body Leakage	I_{GSS}	$V_{\text{DS}} = 0\text{V}, V_{\text{GS}} = \pm 12\text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = -16\text{V}, V_{\text{GS}} = 0\text{V}$			-1	μA
		$V_{\text{DS}} = -13.2\text{V}, V_{\text{GS}} = 0\text{V}, T_J = 125^\circ\text{C}$			-10	
On-State Drain Current ¹	$I_{\text{D}(\text{ON})}$	$V_{\text{DS}} = -5\text{V}, V_{\text{GS}} = -4.5\text{V}$	-24			A
Drain-Source On-State Resistance ¹	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}} = -2.5\text{V}, I_D = -2\text{A}$		124	180	$\text{m}\Omega$
		$V_{\text{GS}} = -4.5\text{V}, I_D = -3\text{A}$		93	115	
Forward Transconductance ¹	g_{fs}	$V_{\text{DS}} = -5\text{V}, I_D = -3\text{A}$		4.4		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = -10\text{V}, f = 1\text{MHz}$		369		pF
Output Capacitance	C_{oss}			78		
Reverse Transfer Capacitance	C_{rss}			67		
Total Gate Charge ²	Q_g	$V_{\text{DS}} = 0.5V_{(\text{BR})\text{DSS}}, V_{\text{GS}} = -4.5\text{V}, I_D = -3\text{A}$		5.1		nC
Gate-Source Charge ²	Q_{gs}			1		
Gate-Drain Charge ²	Q_{gd}			2		
Turn-On Delay Time ²	$t_{\text{d}(\text{on})}$	$V_{\text{DD}} = -10\text{V}, I_D \approx -1\text{A}, V_{\text{GS}} = -5\text{V}, R_G = 6\Omega$		25		nS
Rise Time ²	t_r			60		
Turn-Off Delay Time ²	$t_{\text{d}(\text{off})}$			70		
Fall Time ²	t_f			60		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_J = 25^\circ\text{C}$)						
Continuous Current	I_S				-10	A
Pulsed Current ³	I_{SM}				-24	
Forward Voltage ¹	V_{SD}	$I_F = -10\text{A}, V_{\text{GS}} = 0\text{V}$			-1.2	V

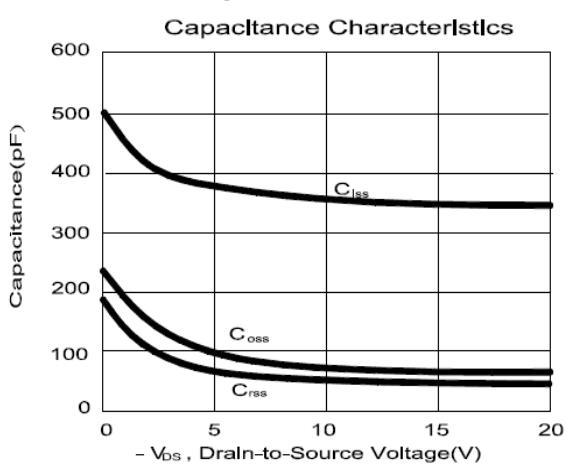
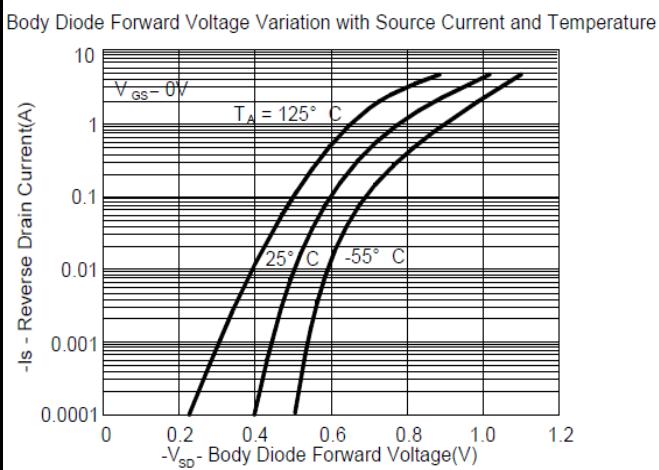
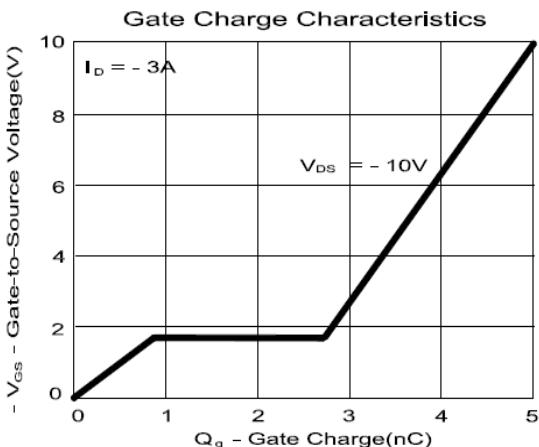
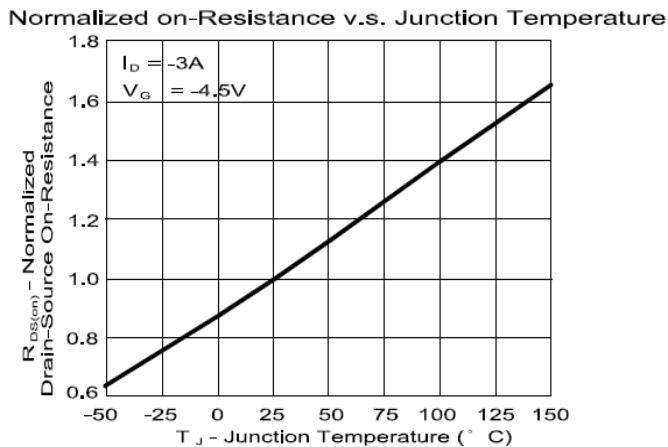
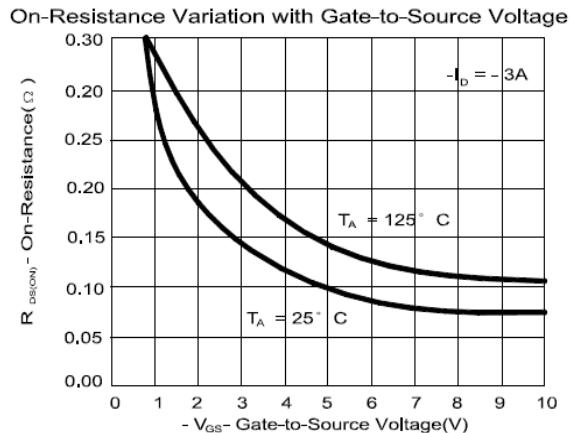
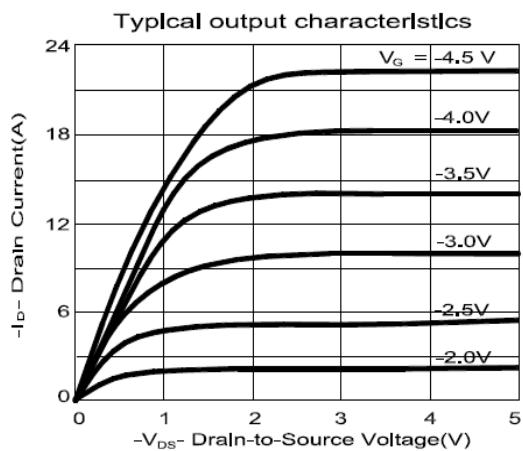
¹Pulse test : Pulse Width $\leq 300\ \mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

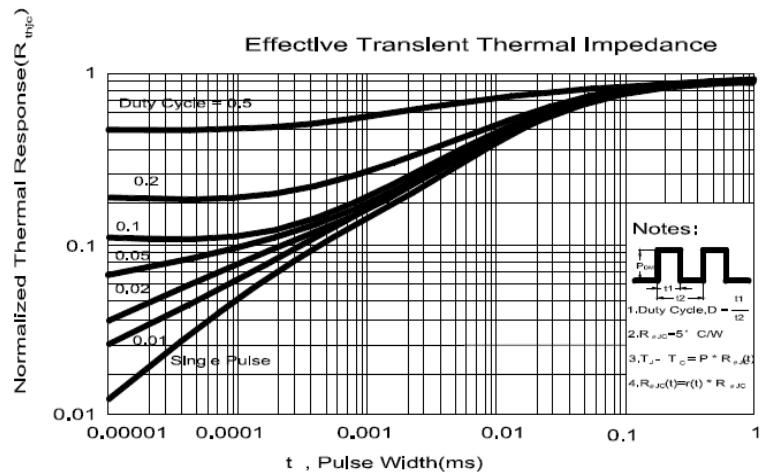
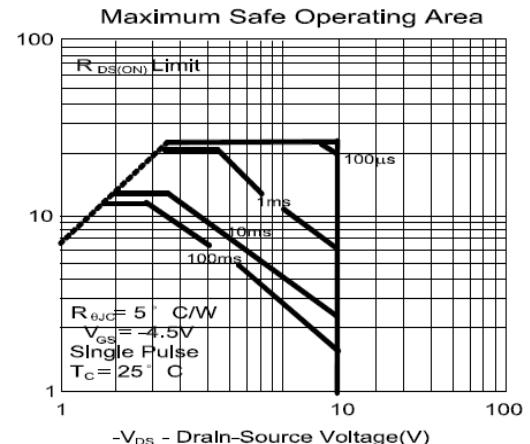
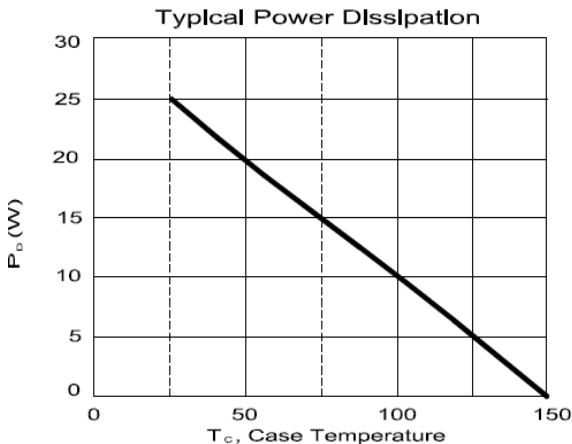
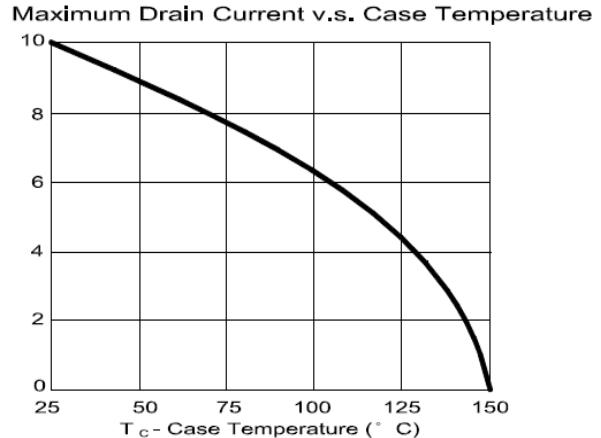
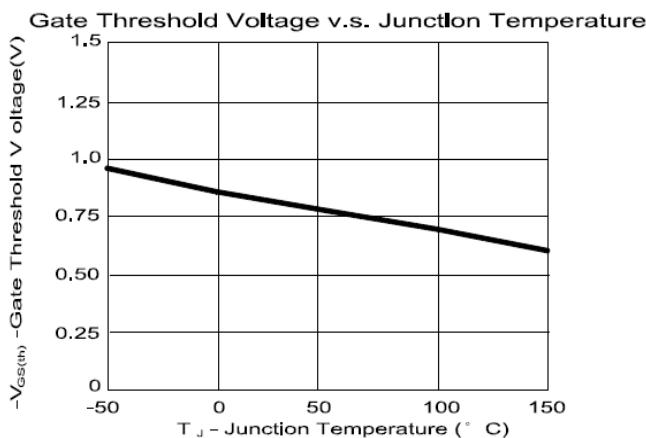
PA102FDG

P-Channel Enhancement Mode MOSFET



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PA102FDG

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Package Dimension

TO-252 (DPAK) MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	8.9	10	10.41	J	4.8		5.64
B	2.1	2.2	2.5	K	0.15		1.49
C	0.4	0.5	0.61	L	0.4	0.76	0.91
D	0.82	1.2	1.5	M	4.2	4.58	5
E	0.35	0.5	0.65	S	4.57	5.1	5.52
F	0		0.2	T	3.81	4.75	5.24
G	5.3	6.1	6.3	U	1.4		1.78
H	0.5		1.7	V	0.55	1.25	1.7
I	6.3	6.5	6.8				

