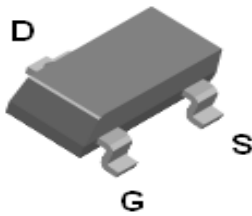


# PA102FMA

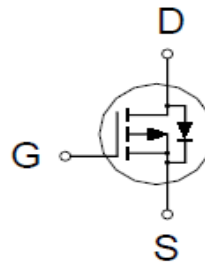
## P-Channel Logic Level Enhancement Mode MOSFET

### PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	$I_D$
-20V	118m $\Omega$ @ $V_{GS} = 4.5V$	-2A



SOT-23(S)



### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25\text{ }^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Drain-Source Voltage	$V_{DS}$	-20	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	V
Continuous Drain Current	$I_D$	$T_A = 25\text{ }^\circ\text{C}$	-2
		$T_A = 70\text{ }^\circ\text{C}$	-1.7
Pulsed Drain Current <sup>1</sup>	$I_{DM}$	-9	A
Power Dissipation	$P_D$	$T_A = 25\text{ }^\circ\text{C}$	0.9
		$T_A = 70\text{ }^\circ\text{C}$	0.6
Operating Junction & Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

### THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient <sup>2</sup>	$R_{\theta JA}$		130	$^\circ\text{C} / \text{W}$

<sup>1</sup>Pulse width limited by maximum junction temperature.

<sup>2</sup>The value of  $R_{\theta JA}$  is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A = 25^\circ\text{C}$ .

# PA102FMA

## P-Channel Logic Level Enhancement Mode MOSFET

### ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25 °C, Unless Otherwise Noted)

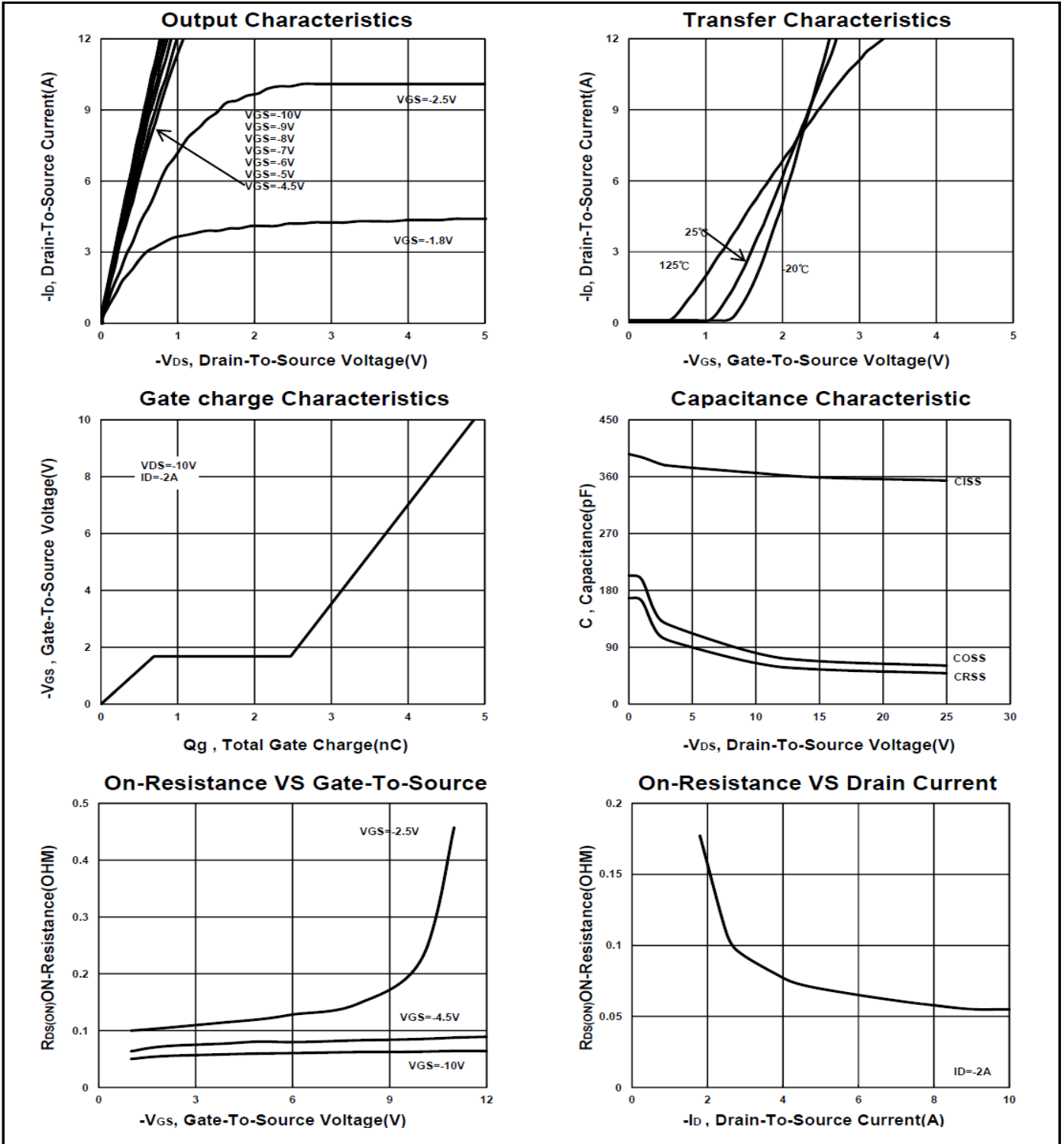
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA	-20			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA	-0.3	-0.75	-1.2	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±12V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -16V, V <sub>GS</sub> = 0V			-1	μA
		V <sub>DS</sub> = -16V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125 °C			-10	
Drain-Source On-State Resistance <sup>1</sup>	R <sub>DS(ON)</sub>	V <sub>GS</sub> = -2.5V, I <sub>D</sub> = -1A		124	215	mΩ
		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -2A		87	118	
		V <sub>GS</sub> = -10V, I <sub>D</sub> = -2A		68	85	
Forward Transconductance <sup>1</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -5V, I <sub>D</sub> = -2A		7.5		S
<b>DYNAMIC</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0V, V <sub>DS</sub> = -10V, f = 1MHz		364		pF
Output Capacitance	C <sub>oss</sub>			88		
Reverse Transfer Capacitance	C <sub>rss</sub>			72		
Total Gate Charge <sup>2</sup>	Q <sub>g</sub>	V <sub>DS</sub> = -10V, V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -2A		5		nC
Gate-Source Charge <sup>2</sup>	Q <sub>gs</sub>			0.7		
Gate-Drain Charge <sup>2</sup>	Q <sub>gd</sub>			2.1		
Turn-On Delay Time <sup>2</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = -10V, I <sub>D</sub> ≅ -1A, V <sub>GS</sub> = -4.5V, R <sub>G</sub> = 6Ω		24		nS
Rise Time <sup>2</sup>	t <sub>r</sub>			24		
Turn-Off Delay Time <sup>2</sup>	t <sub>d(off)</sub>			35		
Fall Time <sup>2</sup>	t <sub>f</sub>			17		
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T<sub>J</sub> = 25 °C)</b>						
Continuous Current	I <sub>S</sub>				0.75	A
Forward Voltage <sup>1</sup>	V <sub>SD</sub>	I <sub>F</sub> = -2A, V <sub>GS</sub> = 0V			1.2	V
Reverse Recovery Time	t <sub>rr</sub>	V <sub>GS</sub> = 0V, di <sub>S</sub> /dt = 100A / μS		11		nS
Reverse Recovery Charge	Q <sub>rr</sub>			2.2		nC

<sup>1</sup>Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

<sup>2</sup>Independent of operating temperature.

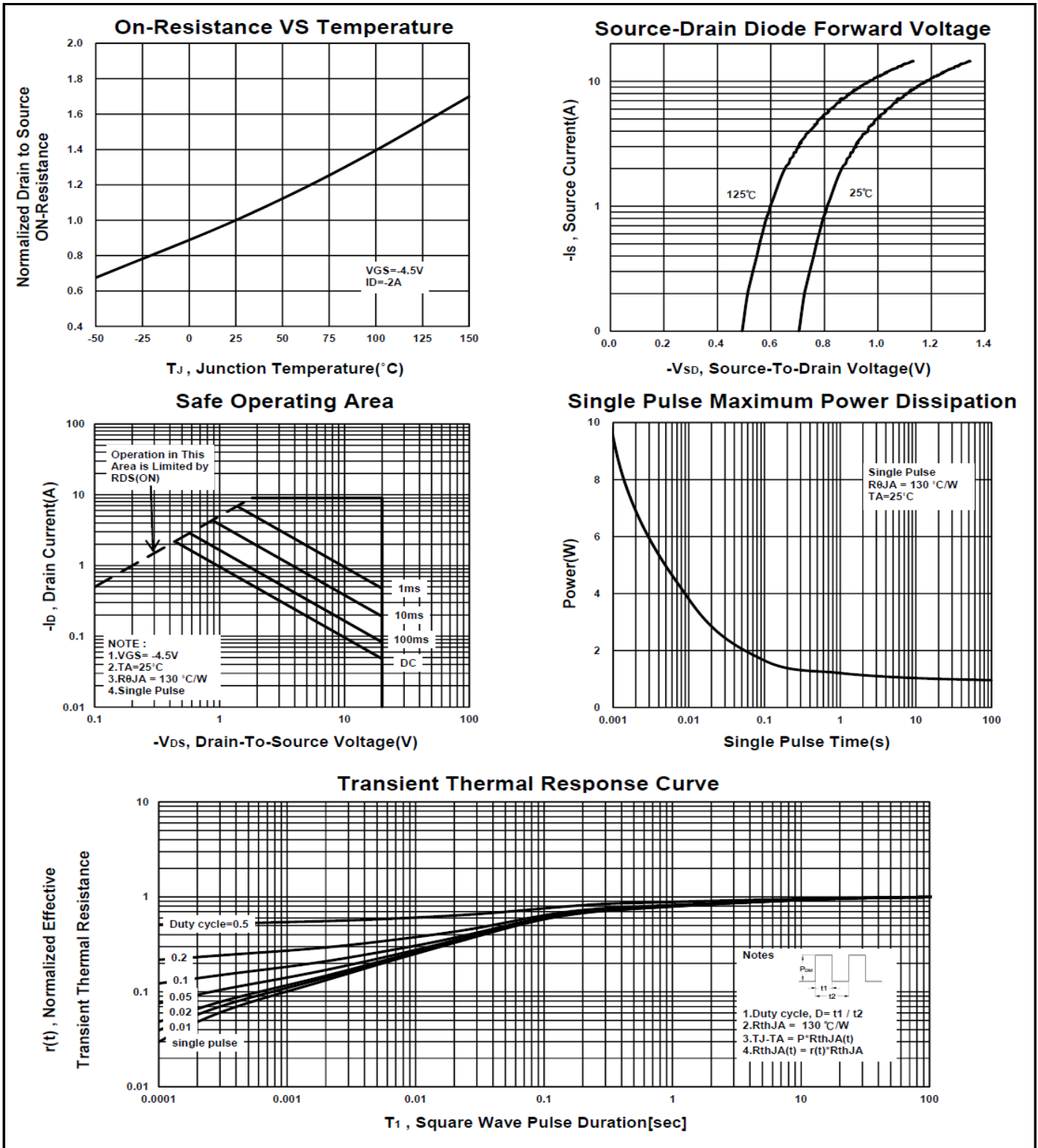
# PA102FMA

## P-Channel Logic Level Enhancement Mode MOSFET



# PA102FMA

## P-Channel Logic Level Enhancement Mode MOSFET



# PA102FMA

## P-Channel Logic Level Enhancement Mode MOSFET

### Package Dimension

### SOT-23 (S) MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	0.9		1	H	0.08		0.2
B	2.25		2.85	I	0.15		0.6
C	1.2		1.4				
D	2.8		3.04				
E	0.89		1.2				
F	0		0.1				
G	0.3		0.5				

