Introduction
This is a reference note for Protek Analog's PA1418. The document includes data for the IC, recommended external components, and other pertinent information.

Please read all instructions and recommendations before beginning to design any product that is to include this device. This document contains a checklist to reference before powering up completed circuit and troubleshooting procedures outlining causes and countermeasures for issues arising in the application of the IC.

Contact information is included if this document is insufficient to answer any problems or questions that may arise.

Contents

1. Overview:

The PA1418 is a Radio Transmitter that can send audio signals from personal computers, game consoles or independent devices to any type of audio equipment with a built in FM receiver.
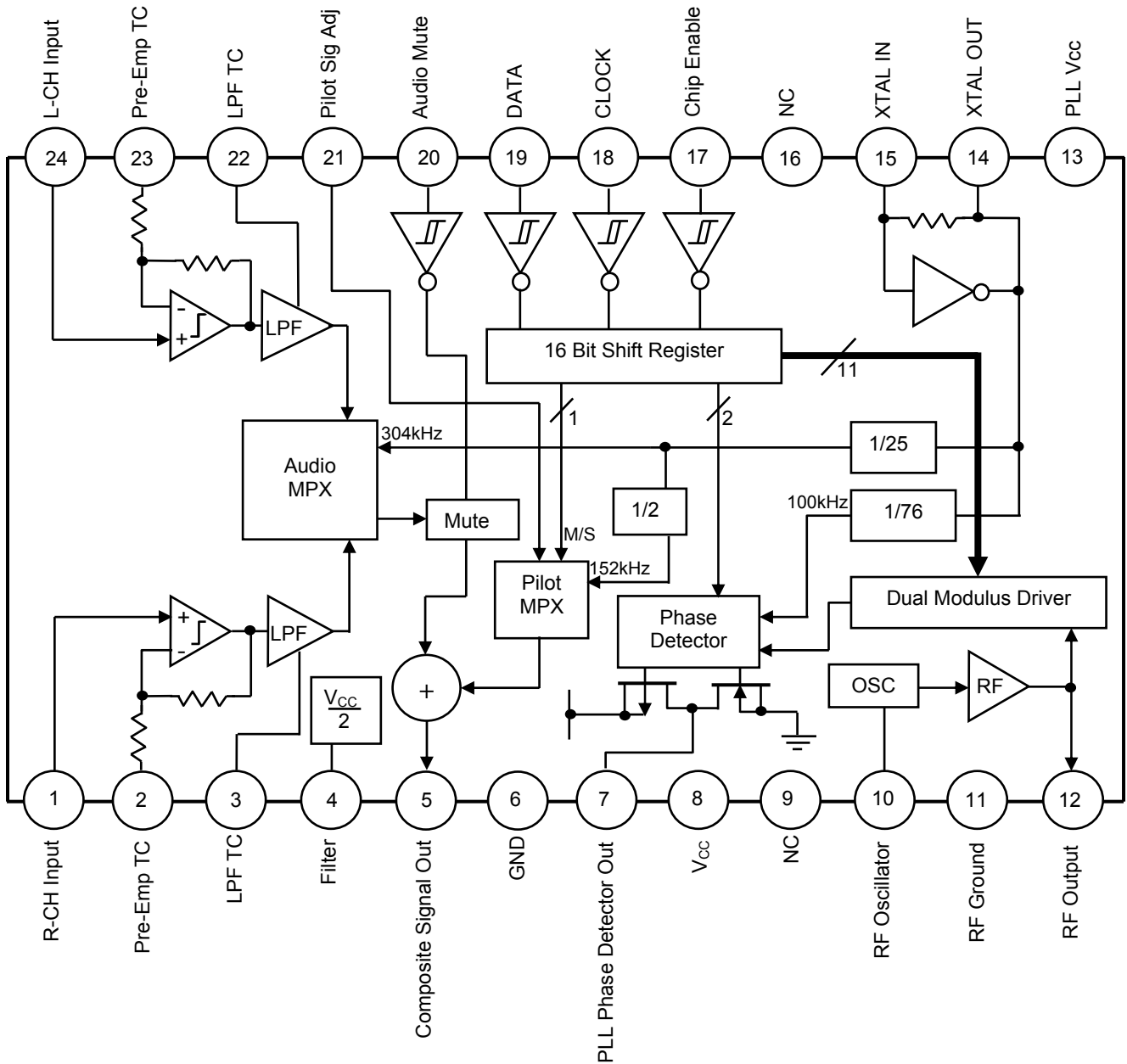The IC consists of a Pre-Emphasis circuit that improves Signal to Noise Ratio (S/N), a Limiter circuit that prevents over-modulation and a low Pass filter (LPF) circuit that limits the maximum modulation frequency. The Stereo modulation circuit generates stereo composite signals through a FM transmitter circuit with Phase-Locked Loop (PLL) frequency synthesizers.

1. 1. Features

1. Improved Audio Quality due to integrated Pre-emphasis, limiter and Low-pass filter circuits.
2. Pilot tone FM stereo modulation circuit is integrated.
3. An incorporated PLL frequency synthesizer ensures a stable FM transmission frequency.
4. Device utilizes a serial data control method to set the frequency via a microcontroller.
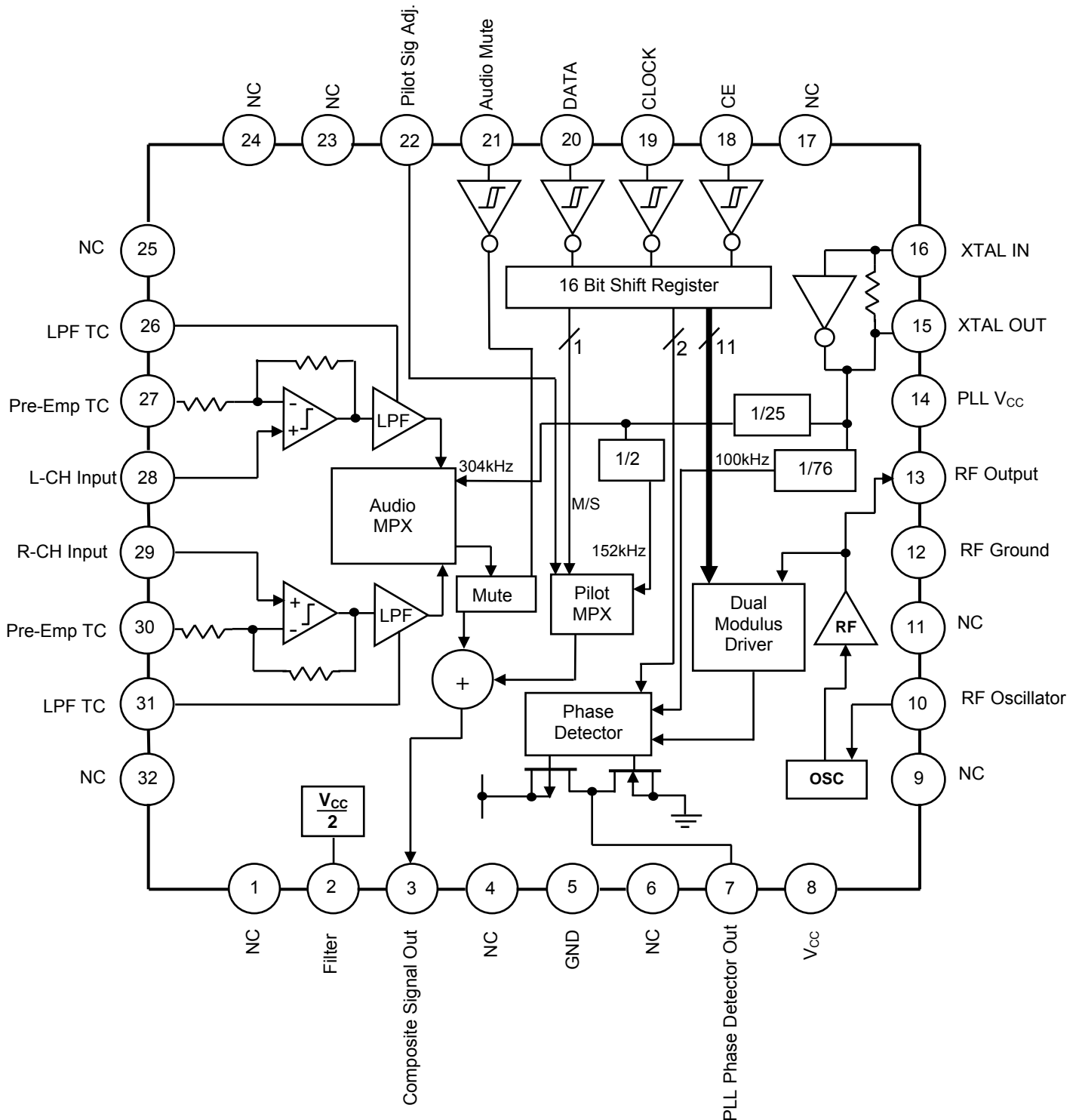5. Integrated mute option.

ANALOG PRODUCT DIVISION

1. 2. Block Diagram:

24 TSSOP Package

Top pins (left to right): 24 L-CH Input, 23 Pre-Emp TC, 22 LPF TC, 21 Pilot Sig Adj, 20 Audio Mute, 19 DATA, 18 CLOCK, 17 Chip Enable, 16 NC, 15 XTAL IN, 14 XTAL OUT, 13 PLL Vcc

Bottom pins (left to right): 1 R-CH Input, 2 Pre-Emp TC, 3 LPF TC, 4 Filter, 5 Composite Signal Out, 6 GND, 7 PLL Phase Detector Out, 8 Vcc, 9 NC, 10 RF Oscillator, 11 RF Ground, 12 RF Output

Internal blocks: LPF, Audio MPX, Mute, $\frac{V_{CC}}{2}$, Pilot MPX, Phase Detector, 16 Bit Shift Register, 1/2, 1/25, 1/76, Dual Modulus Driver, OSC, RF. Labels: 304kHz, 152kHz, 100kHz, M/S, /1, /2, /11.

1.2. Block Diagram:

32 QFN Package

1. 3. Maximum Operating Range

(Ta = 25°C, In test circuit)(Pin numbers reference the 24 TSOP package)

Parameter	Symbol	Limits	Unit	Conditions
Supply Voltage	V_{CC}	+7.0	V	Pin 8, 13.
Data Input voltage	V_{IN-D}	- 0.3 to Vcc + 0.3	V	Pin 17,18,19,20.
Phase comparator output voltage	V_{OUT-P}	- 0.3 to Vcc + 0.3	V	Pin 7.
Power dissipation	P_D	630	mW	(*Note 1*)
Storage Temperature	T_{stg}	-55 to +125	ºC	

(Note 1) when operation temperature exceeds Ta= to 25ºC power is derated at 6.3mW per 1ºC

1.4. Recommended Operating Range

(Ta = 25°C,)

| Parameter	Symbol	Limits	Unit	Conditions
Operating Supply Voltage	V_{CC}	3.6 to 5.0	V	Pin 8, 13.
Operating Temperature	T_{OPR}	-40 to +85	ºC	
Audio Input level	V_{IN}-A	Up to 10	dBV	Pin 1, 24
Audio Input Frequency Band	f_{IN}-A	20 to 15k	Hz	Pin 1, 24
Pre-emphasis time constant set up range	t_{PRE}	to 155	μS	Pin 2, 23
Transmission Frequency	f_{TX}	70 to 120	MHz	Pin 10, 12
Control Terminal "H" level input voltage	V_{IH}	0.8Vcc to Vcc	V	Pin 17, 18, 19, 20.
Control Terminal "H" level input voltage	V_{IL}	GND to 0.2Vcc	V	Pin 17, 18, 19, 20.

Notes

i. **Operating conditions**.
    a. Do not exceed the maximum rating for this device even momentarily; reliability and functionality of the device could be compromised. If special design considerations permit the circuit to exceed the listed tolerance, please utilize a fuse or other methods to protect component from damage.
    b. The electrical characteristics described at Ta = 25°C cannot be guaranteed if this operating temperature is not maintained. Please contact the engineers at Protek Analog if you have any questions or concerns.

ii. **Storage and Transportation.**
    a. Store the product in a dry place at room temperature to prevent oxidation of the device terminals. (Humidity = 75% or less, Temperature = 0-30°C)
    b. Please use static protection containers when storing or transporting devices.
    c. Be careful not to expose ICs to water or electrically conducting fluids at any time and avoid toxic gasses or dust.
    d. During transportation, please insulate the device from any discharge capacitors on boards.
    e. Avoid mechanical vibration and physical shock to devices during transportation or storage.

iii. **Cautions during Installation.**
  a. Some device packages contain NC terminals, please do not use these free pads for relays, or allow the other pins to make contact with these NC terminals. Problems such as unwanted oscillations may occur.
  b. Caution: If a heat sink is cut or damaged and the device is deformed the induced thermal stress can cause a failure or limit the life of the device.
  c. When mounting device on a board please be careful to align the device in the correct direction, both the 32 QFN and 24 TSSOP packages have dots placed in the same corner of the package corresponding to pin 1. Powering on the device with the pins misaligned can ruin the device.

32 QFN   24 TSSOP
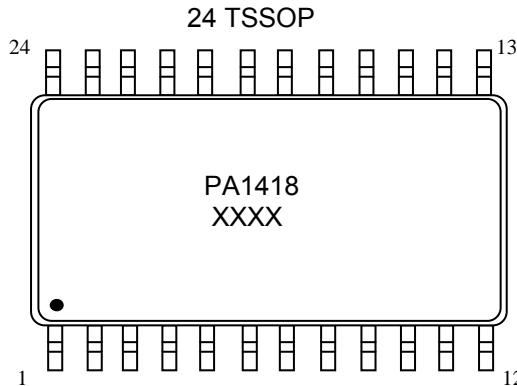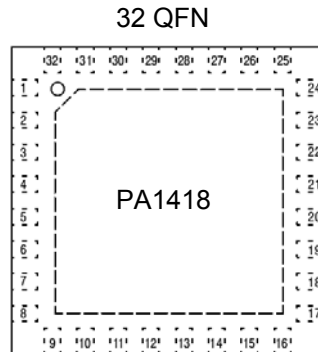
  d. Install the device gently on its PCB level with the plane of the board to reduce stress on pins and contacts.
  e. Before soldering device, be sure that the soldering iron properly grounded and that it is not leaking power into the tip. Discharge from the iron can cause failure of the device when placed in contact with the pins.
  f. Verify that all assembly stations and their perspective assembly techs are properly grounded as released static charge can have an adverse effect on the device. Likewise, pay close attention to the humidity and production methods to reduce static buildup.

iv. **Cautions during testing and inspection.**
  a. Be sure to inspect soldering for accuracy before applying power to the device, bridged pins can cause serious damage.
  b. Please use a current limiter circuit on the power supply, high currents can go into the device and ruin it.
  c. Be careful that the device or board is in the designated position before starting measurement inspection or possible high currents can damage product.
  d. Ensure that the ground will not generate a surge current.

v. **Heat Design**
  a. The operational characteristics of this device are affected by temperature. Excessive heat can cause the performance and life expectancy of the product to reduce dramatically, in Extreme cases destroying the device outright.
  b. The IC is designed for balanced temperature at normal operation; if however, external components or lack of proper ventilation cause excessive heat than additional heat sinks can be utilized to cool the device.
  c. If additional heat sinks are implemented, please ensure that they are properly bonded to device.

  If you have any questions about thermal design or any other topics in an application please contact the applications team at Protek Analog.

2. Operation: (Pin numbers reference 24 TSSOP package)

The PA1418, FM stereo transmitter IC made by ProTek Analog includes all the processing circuitry required for stereo FM transmission and also the crystal control section, which provides precise frequency locking
As shown, the PA1418 includes two separate audio processing sections, for the left and right channels. The left-channel audio signal is applied to pin 24 of the chip, while the right channel signal is applied to pin 1. These audio signals are then applied to a pre-emphasis circuit, which boosts those frequencies above a 50ms time constant (i.e., those frequencies above 3.183 kHz) prior to transmission

Pre-emphasis is used to improve the signal-to-noise ratio of the received FM signal. It works by using a complementary de-emphasis circuit in the receiver to attenuate the boosted treble frequencies after demodulation, restoring the frequency response is restored to normal. At the same time, this also significantly reduces the 'hiss" sound that would otherwise be evident in the signal

The amount of pre-emphasis is set by the value of the capacitors connected to pins 2 & 23, (Signal limiting is also provided within the pre-emphasis section). This involves attenuating signals above a certain threshold to prevent overloading succeeding stages also preventing over-modulation and reduces distortion. The pre-emphasized signals for the left and right channels are then processed through two low-pass filter (LPF) stages, designed at15kHz. This roll-off is necessary to restrict the bandwidth of the FM signal and is the same frequency limit used by commercial broadcast FM transmitters.

The outputs from the left and right LPF channels are in turn applied to a multiplex (MPX) block. This is used to effectively produce sum (left + right) and difference (left - right) signals which are then modulated onto a 38 kHz carrier. The carrier is then suppressed (or removed) to provide a double-sideband suppressed carrier (DSBSC) signal. It is then mixed in a summing (+) block with a 19 kHz pilot tone to give a composite signal output (with full stereo encoding) at pin 5.

The phase and level of the 19 kHz pilot tone are set using a resistor and a capacitor at pin 21.The 38 kHz multiplex signal and 19 kHz pilot tone are derived by dividing down the 7.6MHz crystal oscillator located at pins 14 & 15. The 7.6MHz crystal frequency is divided by 25 to provide a 304 kHz signal. This 304 kHz signal is used by the audio multiplexer and an 8-bit DAC to generate the composite signal with the subcarriers (38 kHz). The 76MHz frequency is also divided by 50 to generate a 152 kHz frequency. This signal is used by the pilot signal into the composite audio.

In addition, the 1.9MHz signal is divided by 76 to give a 100 kHz signal. This signal is then applied to the phase detector, which also monitors the program counter output. This program counter is actually a programmable dual modulus divider, which outputs a divided down value of the RF signal.

The division ratio is set by programming the counter with a 6 and 5 bit number. More information on the working of the dual modulus divider is given in section I of "Explanation of External Parts"

The phase detector output produces an error signal to control the voltage applied to a varicap diode and forms part of the RF oscillator at pin 10. Its frequency of oscillation is determined by the value of the inductance and the total parallel capacitance.
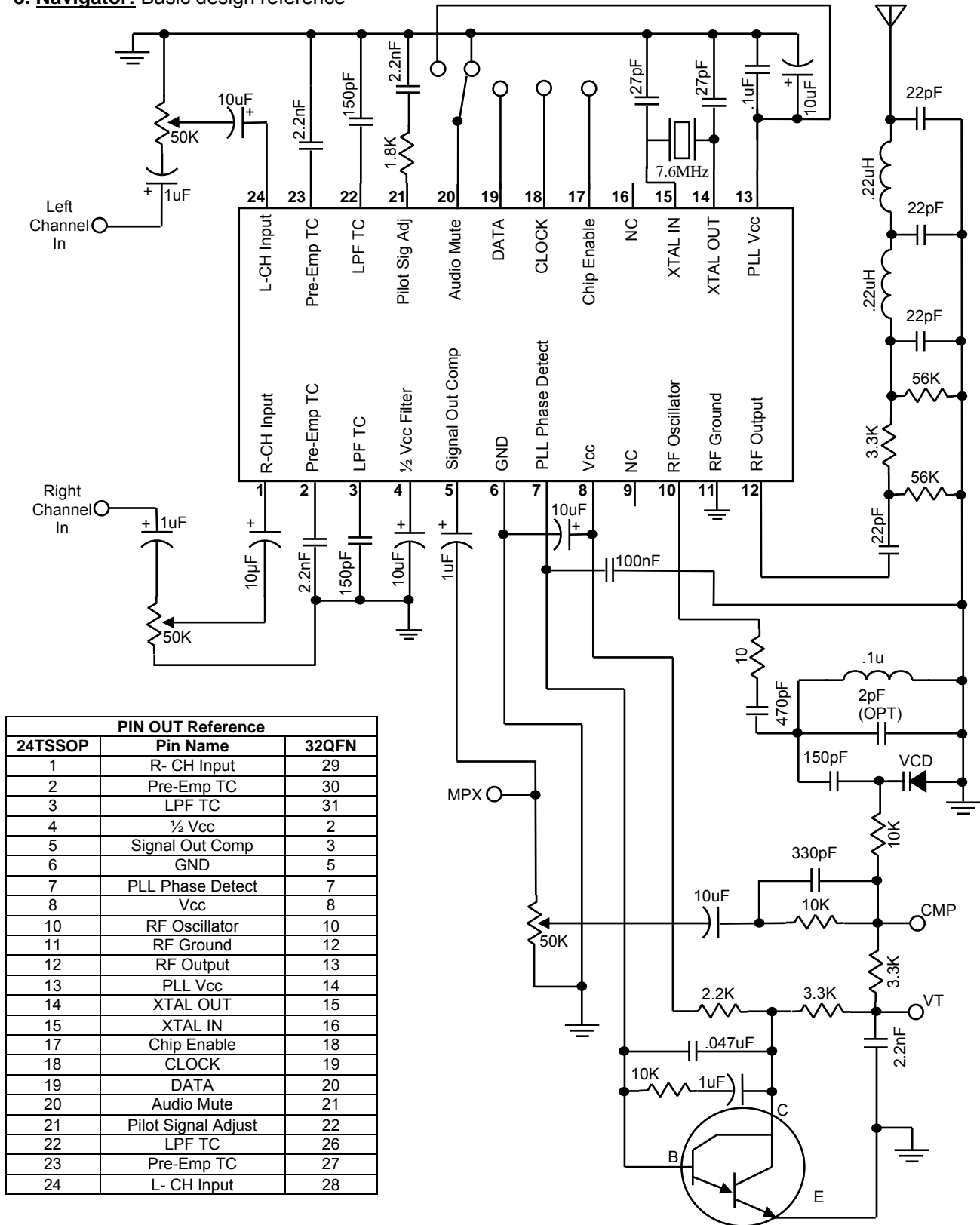
Since the varicap diode forms part of this capacitance, we can alter the RF oscillator frequency by varying its value. In operation, the varicap diode's capacitance varies in proportion to the DC voltage applied to it by the output of the PLL phase detector. The phase detector adjusts the varicap voltage so that the divided RF oscillator frequency is 100 kHz at the program counter output. If the RF frequency drifts high, the frequency output from the programmable divider rises and the phase detector will "see" an error between this and the 100 kHz signal. As a result, the phase detector reduces the DC voltage applied to the varicap diode, thereby increasing its capacitance. And this in turn decreases the oscillator frequency to bring it back into "lock".

Conversely, if the RF frequency drifts low, the programmable divider output will be lower than 100 kHz. This means that the phase detector now increases the applied DC voltage to the varicap to decrease its capacitance and raise the RF frequency. As a result, this PLL feedback arrangement ensures that the programmable divider output remains fixed at 100 kHz and thus ensures stability of the RF oscillator.

By changing the programmable divider we can change the RF frequency. So, for example, if we set the divider to 1079, the RF oscillator must operate at 107.9MHz for the programmable divider output to remain at 100 kHz.

The RF frequency is modulated by the voltage applied to the varicap diode using the composite signal output at pin 5.The average frequency of the RF oscillator remains fixed, as set by the programmable divider. As a result, the transmitted FM signal varies either side of the carrier frequency according to the composite signal level - i.e., it is frequency modulated.

3. Navigator: Basic design reference

PIN OUT Reference		
24TSSOP	**Pin Name**	**32QFN**
1	R- CH Input	29
2	Pre-Emp TC	30
3	LPF TC	31
4	½ Vcc	2
5	Signal Out Comp	3
6	GND	5
7	PLL Phase Detect	7
8	Vcc	8
10	RF Oscillator	10
11	RF Ground	12
12	RF Output	13
13	PLL Vcc	14
14	XTAL OUT	15
15	XTAL IN	16
17	Chip Enable	18
18	CLOCK	19
19	DATA	20
20	Audio Mute	21
21	Pilot Signal Adjust	22
22	LPF TC	26
23	Pre-Emp TC	27
24	L- CH Input	28

4. <u>Explanation of External Parts:</u> (Use TSSOP Package for referencing pin locations)

4.1. Pre-Emphasis (Pins 2, 23)

The IC's internal bias is set to ½ Vcc at pins 1 and 24 therefore coupling capacitors (C_1) must be used between these pins and the audio signal. The positive polarity of the coupling capacitors must be set to the higher DC potential whether that is the input signal from the Audio source or the Left and Right channel inputs. The low range frequency cut-off is determined by the input impedance values of pins 1 and 24 and the value of the external coupling capacitors. If the value is too low the lower frequency ranges can be cut, but if the value becomes too large a pronounced pop-up noise and a longer start up time will result.

The Input cut-off frequency can be calculated by: $f_{CL} = \dfrac{1}{2\pi 43k\Omega \cdot C1}$

The Pre-Emphasis Time constant is determined by the value of the external capacitors (C_2) at pins 2 and 23 and the IC's internal resistance of 22.7kΩ.

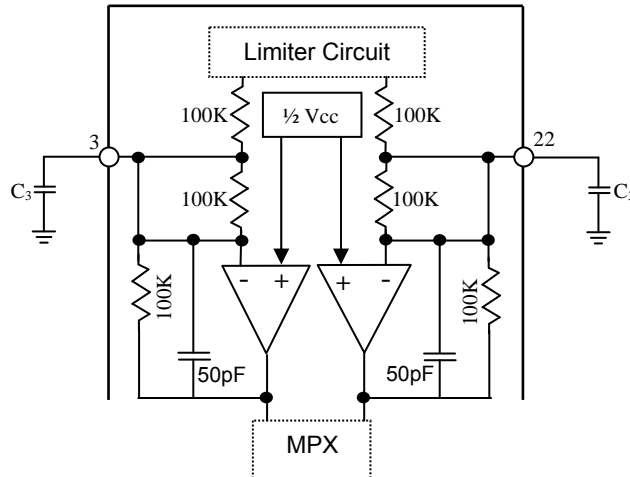The Time Constant can be calculated by: $\tau = 22.7k\Omega * C^{2}$ $\tau < 155\mu\sec$
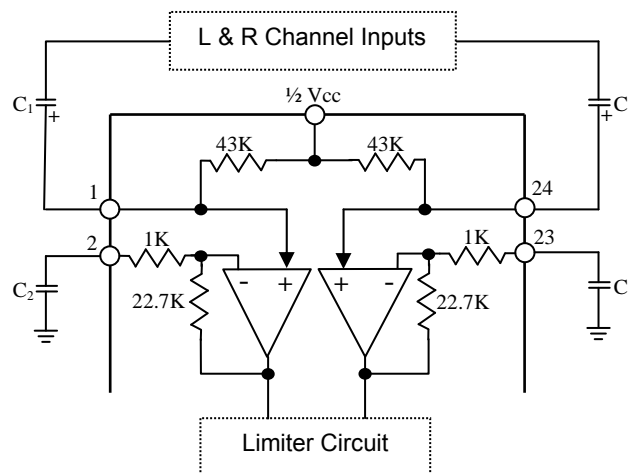
4.2. Limiter (Internal)
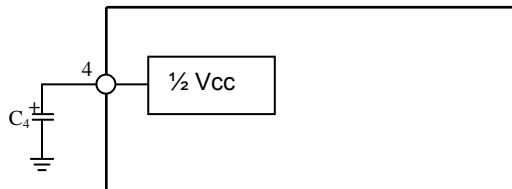
The Limiter Circuit:
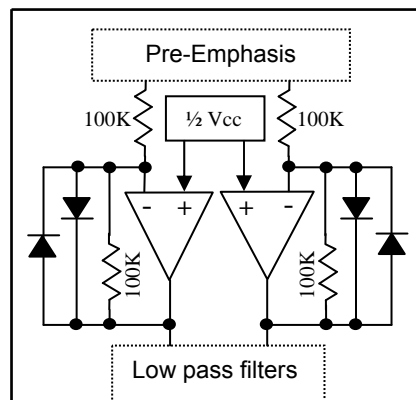
4.3. Low Pass Filter (Pins 3 and 22)

Both pin 3 and pin 22 require 150pF capacitors (C_3) connected to ground to complete the LPF circuit.

4.4. Half Vcc Filter (pin 4)

A 10µF capacitor (C4) is required for proper filtering. A lower value will add distortion while a higher value will slow the start up time.

4.5. Composite Signal Adjust (pin 5)

The modulation rate is adjusted using the composite signal output (pin 5) and the external FM modulator. To make an adjustment, alter the load resistance at pin 5 by changing the value of R_1. The total load on pin 5 should not exceed 50kΩ; lesser values will add unnecessary distortion.

$$f_{CL} = \frac{1}{2\pi R_1 C_5}$$
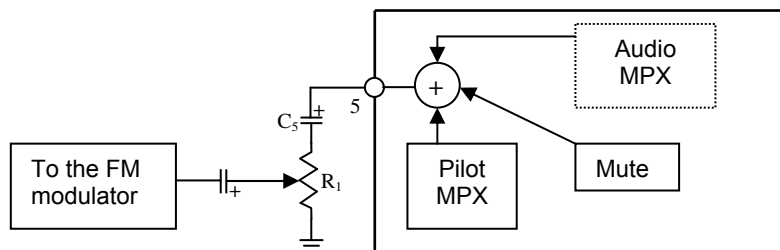
By design, the IC is set so that the composite output L + R = 85% and Pilot = 15% when 400Hz and -20dBV of sine wave is input to pins 1 and 24. The pilot modulation rate is set to 15% to prevent the amplitude from lowering and the modulation rate from dropping far below 10% when the phase of the pilot signal is adjusted. If it is necessary to adjust the pilot modulation precisely, insert a resistor first in between pin 19 and capacitor to lower the modulation rate. Then adjust R_1 while measuring the FM modulation rate at pin 11 until it reaches 100% with a modulation analyzer.

4.6. RF Oscillator (pin 10)

The RF Oscillator is a modified Clapp oscillator, which consists of bipolar transistors. The features of this circuit are such that the oscillating condition is not affected even if the impedance of the parallel resonant (LC) circuit is changed. The oscillation is stabilized against internal transistor changes because the feedback capacitor inside the IC is much larger than the capacitance of the transistor. The RF Oscillator is an important part of the PLL circuit and should be verified in the application. Undesirable noise may result from running oscillations at the limits of the range or from external factors. The scale of the distortions are directly proportional the frequency so extra care is needed when using the upper ranges of the oscillator. It is also important to be sure the Oscillator's components are properly secured; vibrations can cause undesired modulation if not mechanically sound.
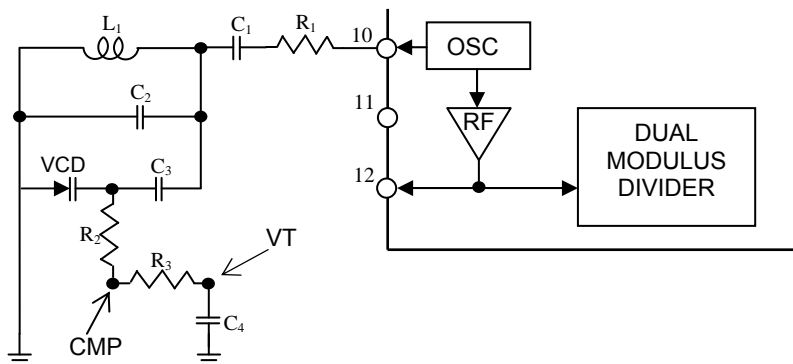
The padding Capacitor C_3 in series with the Variable Capacitance Diode VCD is used to adjust the oscillating frequency range. The choice of C_3 depends on the characteristics of the VCD. C_3 can vary from 10pF to 150pF depending on surrounding components. If C_3 is set closer to 100pF then the VCD has a large impact on the LC resonant circuit. When C_3 is set with a low capacitance, the variable range of the control voltage to the VCD becomes wider, thereby making the oscillator excessively sensitive. This can cause the modulation rate to fluctuate in an exaggerated fashion in relation to the transmission frequency.

The Inductance of the coil L_1 is set so that the reactance X_L may be around 50-100

$$\text{If } f_{TX} = 77.5 \text{ MHz then, } L_1 = \frac{X_L}{2\pi f_{TX}}$$

The capacitor C2 is connected in parallel with L1 and is used to set the range of the oscillator frequency. The larger the C_{MIN} capacitor value, the smaller the variable range will become.

$$\text{If } f_{MIN} = 76 \text{ MHz then, } C_{TOTmin} = \frac{1}{\omega^2 L_1} = 42.6\text{pF}$$

$$\text{If } f_{MAX} = 79 \text{ MHz then, } C_{TOTmax} = \frac{1}{\omega^2 L_1} = 39.4\text{pF}$$

C_{TOT} is the combination of the inline capacitance of VCD and C_3 with C_2. Choose a VCD that had a linear c-v relationship of $0 \leq V_{IN} \leq 5.0$. In this schematic the part number used was Zetex ZMV832ACT that has a capacitance range of 30pF @ V_{IN} = 0V to 11pF @ V_{IN} = 5.0V. (please refer to manufacturer's datasheet for detailed information on this part)

The type of capacitor used for C_2 is also of importance because of the need to cancel the temperature characteristics of L_1. A temperature compensating ceramic capacitor is utilized for this purpose. For air-core coil inductors RH (-220±60 ppm/C°) or SH (-330±60 ppm/C°) can be used, for ferrite-core inductors TH (-470±60 ppm/C°) or UJ (-750±60 ppm/C°) are recommended.

The damping resistor R_1 and the coupling capacitor C_1 are used to correct the harmonics of the oscillating circuit. C_2 should be set between 470pF and 47nF. If larger values are utilized, the internal oscillator is greatly affected by the external circuits and may not stabilize. If the value is set low the Q of the oscillating circuit is decreased and the oscillating may stop.

The harmonics are observed by monitoring the antenna terminal with a spectrum analyzer. Please be sure to match the impedance (50Ω or 75Ω) or the results will be misleading.

The damping resistor is used to reduce the harmonics level. Set R_1 between 0Ω and 10Ω. R_1 must be set so that the harmonics comply with the radio laws of the marketed countries.

To confirm the oscillation range of operation,

1. Manually discharge the inductor to stop the oscillation and upon removing the source of the interruption, check to see if the oscillating resumes.
2. Confirm that oscillation can continue when the power supply drops below 3.0V
3. Given that step 1 and 2 passed. Increase the value of R_1 by at least 33% and check to see if the circuit can still oscillate.
4. If the circuit is incapable of passing the first 3 tests, increase the value of C_1 or alter L_1 or the VCD to increase the Q of the circuit.

R_2 is used to increase the impedance after the VCD; to achieve this at least 10KΩ should be employed. R_3 and C_4 act as a low pass filter for the DC voltage at VCD, choose R_3 as 3.3kΩ and C4 as 2.2nF.
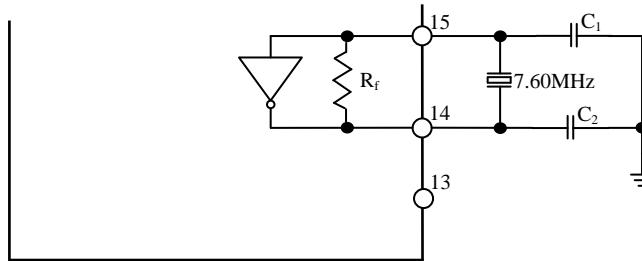
4.7. RF Output (Pin 12)
A BPF must be inserted in-between the RF output and the antenna to suppress undesired RF output harmonics. The output impedance of pin 12 is set to 75Ω.
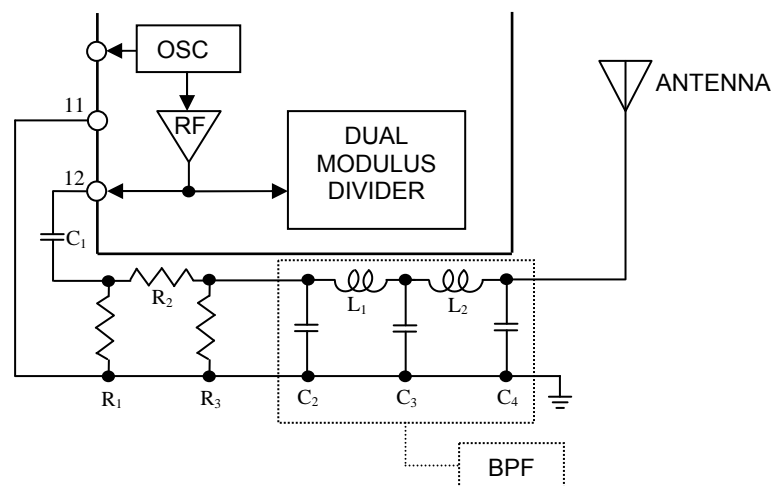
4.8. X'TAL Oscillator (Pin 14, 15)

A 7.60 MHz crystal oscillator is needed between pins 14 and 15 coupled with its 27pF load capacitors (C_1 and C_2) as shown the the folowing drawing.

The crystal needs to be placed as near as possible to the device output pins to minimize stray capacitance. Please no not run any wires or traces near or under the oscillator as it is very suseptable to interference. If possible, place a ground plane directly under the crystal to further insulate it from any nearby signals.

4.9. Serial Data Input (Pin 17, 18, 19)

The V_{IH} level for the inpt voltage at the serial data input is 0.8Vcc to Vcc and the V_{IL} level is GND to 0.2Vcc. Please note that the operating voltage of the microcontroller can be different from the operating voltage of the IC. It is also important to keep in mind that there needs to be a small delay betweeen powering on the IC and inputing the serial data. The initial logic is set as "unfixed" upon startup and some circuits such as the PLL will not function correctly instantaniously.
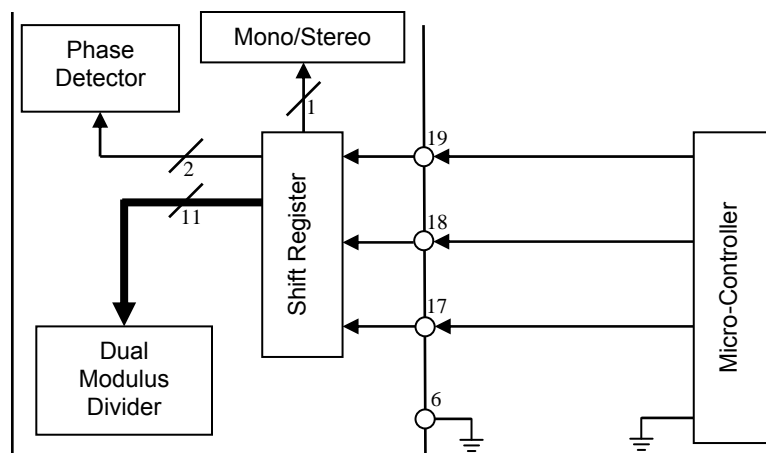
PA1418 – Serial Programming Interface:

The PA1418 has a 3-pin serial programming port. This port consists of pins CE (Chip Enable), CK (Clock) and DA (Data). The timing sequence of these signals is as shown in figure 1. Using these ports a 16-bit word can be fed into the chip to form various division ratios as well as other control bits.
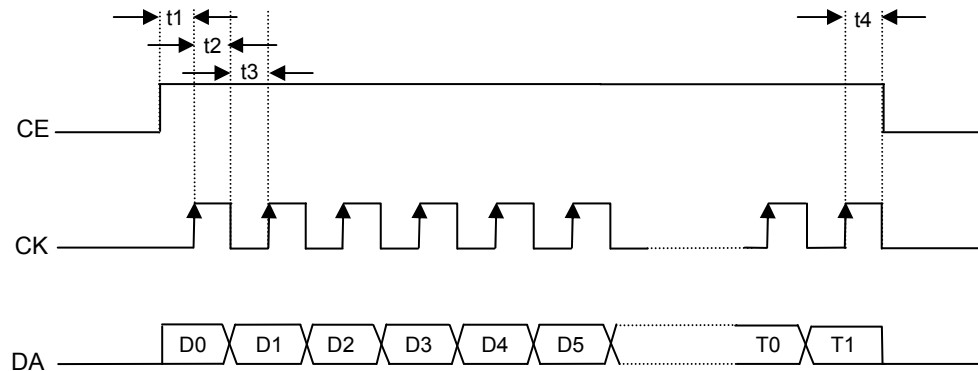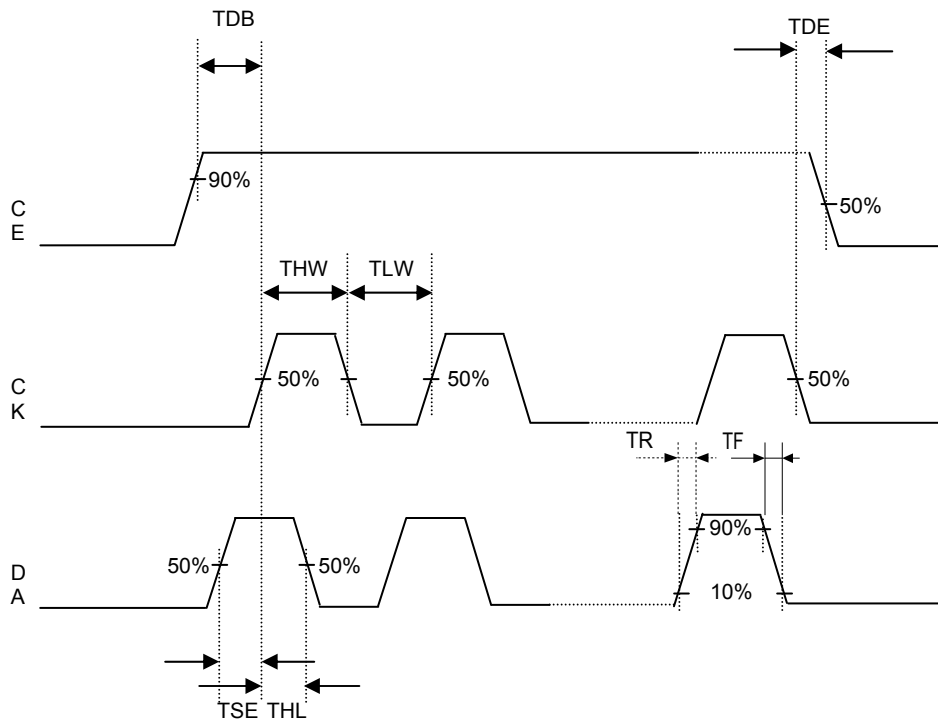
t1, t2, t3, t4 ≤ 1.5µsec

Figure 1: Timing sequence of signals

Setup and Hold Requirements:

The setup and hold requirements of these signals are shown in figure 2:

TDB	TDE	THW	TLW	TR	TF	TSE	THL
≥ 1.5µsec	≥ 0sec	≥ 1.5µsec	≥ 1.5µsec	≤ 300nsec	≤ 300nsec	≥ 100nsec	≥ 100nsec

Figure 2: Setup and Hold requirements of signal

Bit Structure of the 16-bit word:

The bit structure of the 16-bit word is shown in figure 3.
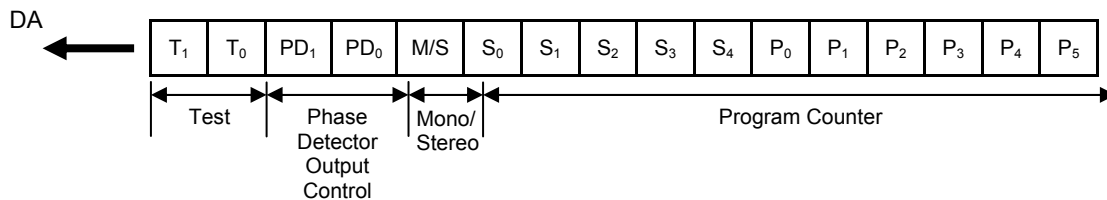
Serial Data Input Configuration

DA ←

T_1	T_0	PD_1	PD_0	M/S	S_0	S_1	S_2	S_3	S_4	P_0	P_1	P_2	P_3	P_4	P_5

Test | Phase Detector Output Control | Mono/ Stereo | Program Counter

Figure 3: Serial data input configuration

Setting up the Program Counter:

Figure 4 shows the contents of the Program Counter.

Program Counter Configuration

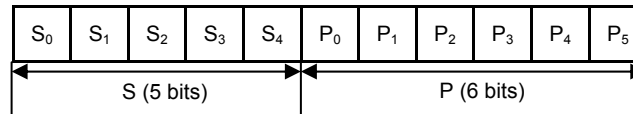| S_0	S_1	S_2	S_3	S_4	P_0	P_1	P_2	P_3	P_4	P_5

S (5 bits) | P (6 bits)

Figure 4: Program Counter Configuration

The Dual Modulus divider works as follows:

$$M = S + P*32 = \frac{f_{RF}}{f_{IN}} = \frac{f_{RF}}{100kHz}$$

Where: **M** is the desired division ratio.
S and **P** are integers such that **S < P**.

Example:
To program for 101.1MHz frequency, perform the following calculations.

$$f_{RF} = 101.1MHz \qquad\qquad M = \frac{101.1MHz}{100kHz} = 1011$$

Calculate P as: $P = \frac{1011}{32} = 31 = 111110_b$

Calculate S as: S= 1011 - 32 ∗ 31 = 19 = 11001_b

To program the chip for normal stereo operation, feed the following bits: (0000 1100 1101 1111)_b

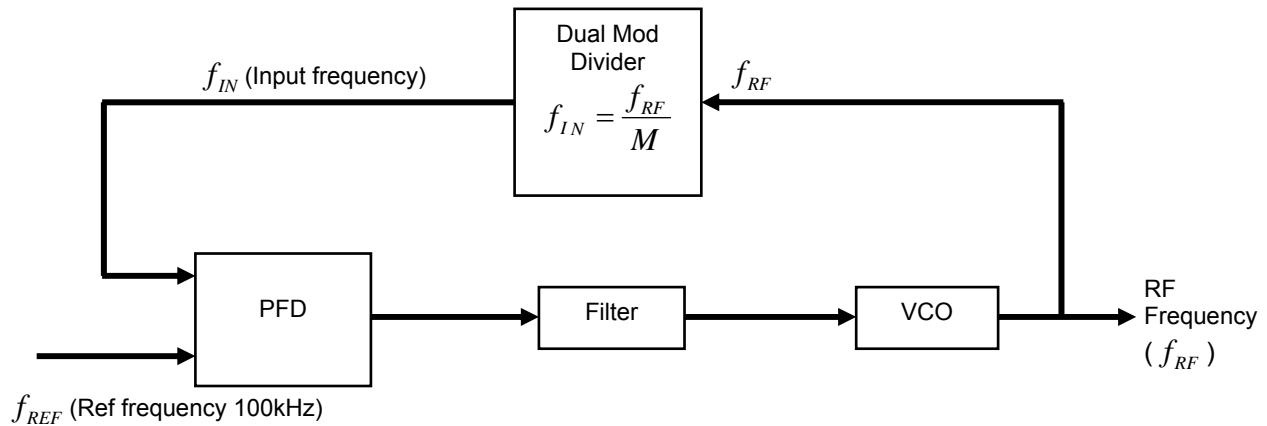$$f_{IN} = \frac{f_{RF}}{M}$$

Figure 5: Block Diagram of PLL. The PFD and Divider are internal to the chip

Please note that due to the limitations of the Dual Modulus Divider, there are frequencies where $S \geq P$, such as 95.9 MHz (where S = 31 and P = 28). If programmed for this frequency or any other frequency where $S \geq P$, the PLL will not lock to the desired frequency and it may produce undesired results like audio noise or jitter.
The following frequencies in the US FM Band may not be programmable by the PA1418: 89.1, 89.3, 89.5, 92.5, 92.7, 95.7, 95.9, 99.1, and 102.3.

Explanation of the remaining controller bits:

In addition to the 11 bit word for the divider, the PA1418 provides an additional 5 bits for controlling the phase detector output and the multiplexer stereo/mono transmission. They are as follows:

Mono/Stereo:

Mono	Status
0	Monaural Operation, L + R, Pilot Off
1	Stereo Operation, L + R + (L-R)sinωt + Psin(ωt/2)

Phase Detector:

PD0	PD1	Charge Pump Output
0	0	Normal Operation
0	1	Forced Low
1	0	Forced High
1	1	High Z–

4.10. PLL Loop Filter

The PA1418 employs a Charge Pump PLL. This means that the PFD output (pin 7) is a current output. An active loop filter is recommended because it has a very small input leakage current. The PA1418 employs a Darlington pair (MPSA13) as the amplifier. The active filter is a low-pass type filter. The block diagram of the PLL is as shown in figure 6.
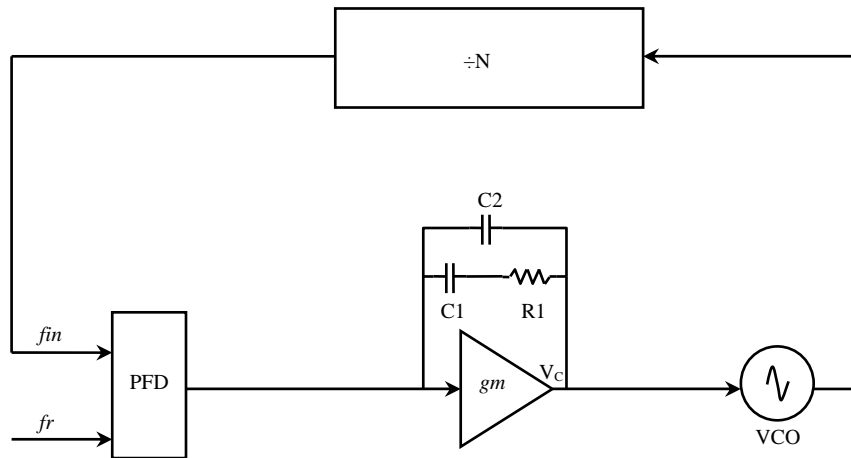

Figure 6: Block Diagram of the Charge Pump PLL

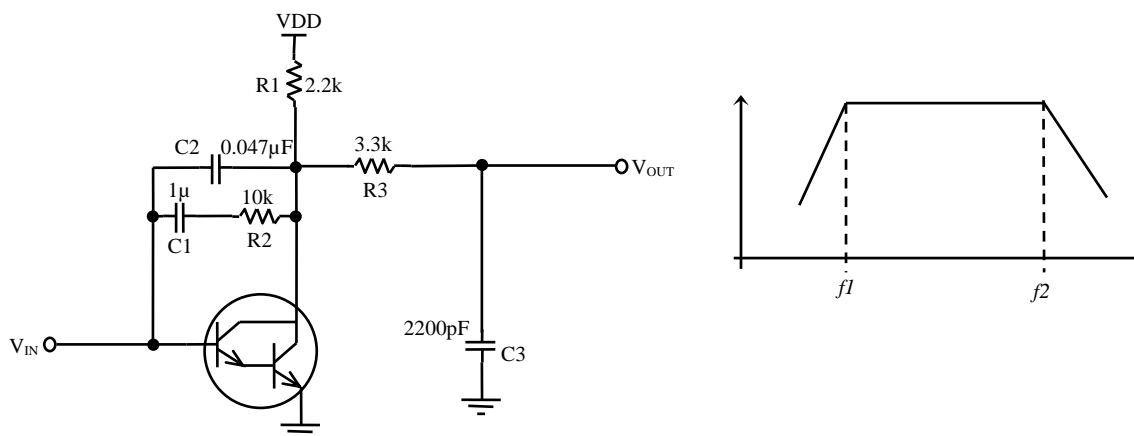The active filter that is used in the PLL, as shown in Figure 7.

Figure 7: Active Loop Filter for PA1418 and its response

Frequencies *f1* and *f2* are obtained as follows:

$$f_1 = \frac{1}{2\pi R_2 \cdot C_1} = 15.9 Hz$$

$$f_2 = \frac{1}{2\pi R_3 \cdot C_3} = 21.9 kHz$$

The PLL directly conducts audio modulation to the VCO. Hence the interrupting frequency *f1* should be set low. The time to lock to the set frequency is dependent on the time constant τ_1 which is calculated as follows:

$$\tau_1 = C_1 \cdot \left(R_2 - \frac{1}{Gm} \right) \text{ where } Gm = gm \cdot R_1$$

This time constant has a trade-off relation with the amplitude and distortion characteristics when the modulation is conducted at a low range frequency (100Hz). In other words, if the frequency lock time is shorter, the distortion ratio in the lower range becomes worse, and if the amplitude characteristics and the distortion ratio are improved, the frequency lock time becomes longer. If R2 value is chosen to be smaller, the gain ($Gm = gm \cdot R_1$) of the amplifier will affect the time constant τ_1 and the loop operation will be unstable. If R1 is set to a higher value to improve the gain of the amplifier, the current through the transistor decreases and the gm results are smaller. This in turn affects the stability of the loop filter.

The capacitor C2 improves the dynamic range of the LPF. C2 is calculated taking into account the stability factor of the LPF circuit. C2 should be calculated from the time constant $\omega_c = \frac{1}{C_2 \cdot R_2}$, with the condition $\omega_c = (5 \sim 10)\omega_n$ where ω_n is the natural angular frequency given by the relation

$$\omega_n = \sqrt{\frac{K_\phi \cdot K_V}{\tau_1}}$$

K_φ is the Phase Detector constant and is given by the expression

$$K_\phi = \frac{I_p}{2\pi} = \frac{20\mu A}{2\pi} = 3.18x10^{-6}$$

K_V is the VCO sensitivity and is calculated as

$$K_V = 2\pi \frac{f_{max} - f_{min}}{V_{max} - V_{min}} = 2\pi \frac{120MHz - 75MHz}{4.0 - 0.6} = 83.15x10^6 \; V/rad/s$$

In this example, ω_n = 1626 rad/s. So ω_c = 16260 rad/s. Choose C_2 = 0.047µF. C_3 and R_3 form a low-pass filter to eliminate the sideband. The ω_c of this filter is much higher than $10\omega_n$ so the loop can be stable.

4.11. Audio Mute (Pin 20)

For the input control of the Mute terminal, the V_{IH} level is 0.8Vcc to Vcc and V_{IL} level is GND to 0.2Vcc. This can be controlled using a microcontroller (Fig 8) or controlled with the IC's Vcc and an alternate switching control. (Fig 9)
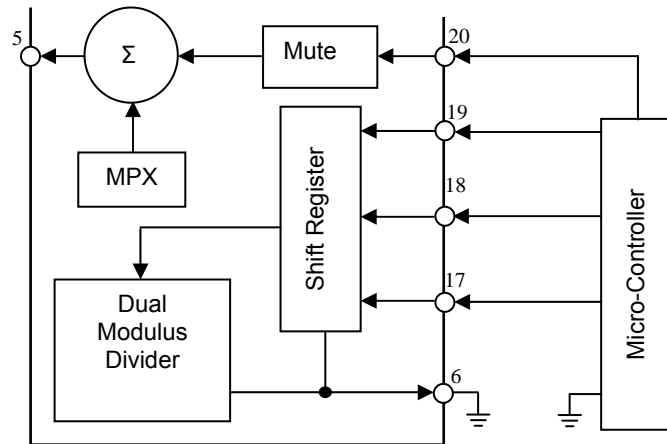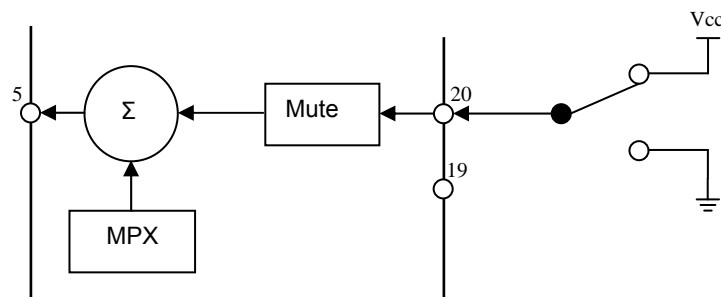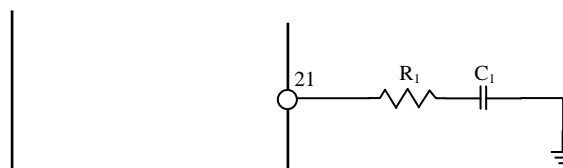

Figure 8: Controlling mute with microcontroller

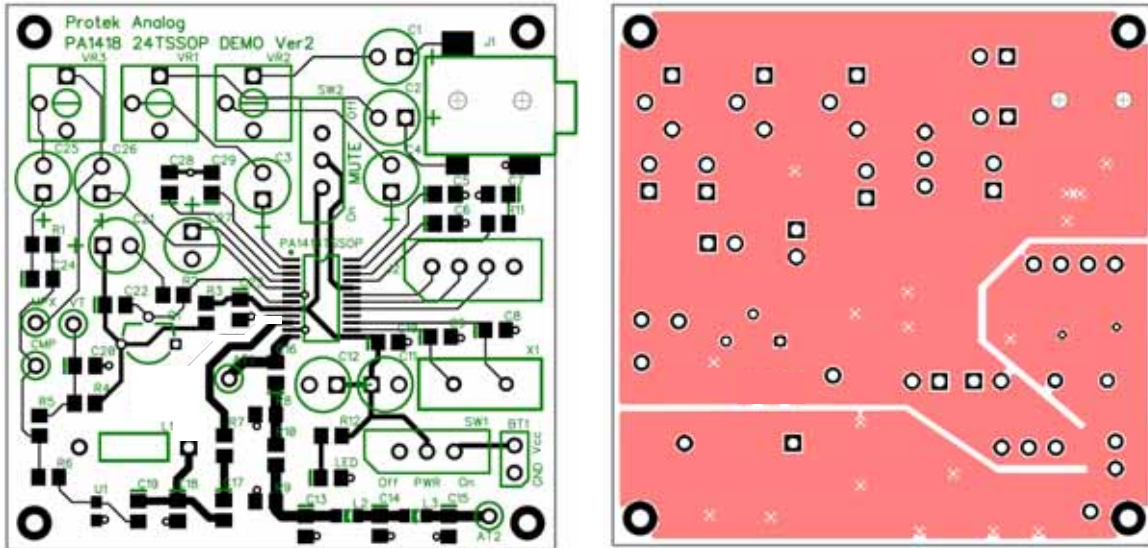*Figure 9: controlling mute with external switch*

5. Pilot Signal Adjust (Pin 21)

The Phase of the pilot signal can be adjusted by changing the RC constant of R_1 and C_1 in-between pin 21 and ground. Recommended settings are 1.8KΩ for R_1 and 2.2nF for C_1.

5. PCB Samples and recommendations:

24 TSSOP Sample demo board:

Recommendations:

- It is important to note that the ground plane has been segragated into 3 semi-isolated sections to help isolate the RF Output, the Input and PLL LPF, and the digital sections. It is detrimental to signal integrity to allow these sections to share ground impedence where it can be otherwise avoided.

- Ideally, the bypass capacitors should be placed as close to the IC as possible and have the needed characteristics to handle the high frequencys of the circuit.

- When possible, using an independent power supply for the digital system is useful to prevent noise from interfering with the other circuit blocks.

- The crystal Oscillator should be placed as close as possible to the IC to minimize stray capacitance. It is also important to keep it clear of other signal traces or power lines that could interfere with it's operation.

- The traces for the RF Oscillator and the RF output should be of suffecient width to reduce stray capacitance. (0.5mm wide minimum)

- It is important that the RF Output should be isolated and not be allowed to cross any other signal paths, nor should it cross through vias or reflective trace corners that can reduce signal strength and intergrity.