PA46

FEATURES

- MONOLITHIC MOS TECHNOLOGY
- PROGRAMMABLE I_Q (5 or 50 mA MAX)
- LOW COST
- HIGH VOLTAGE OPERATION—150V
- HIGH SLEW RATE—27V/μs
- HIGH POWER—5A, 75W DISSIPATION

APPLICATIONS

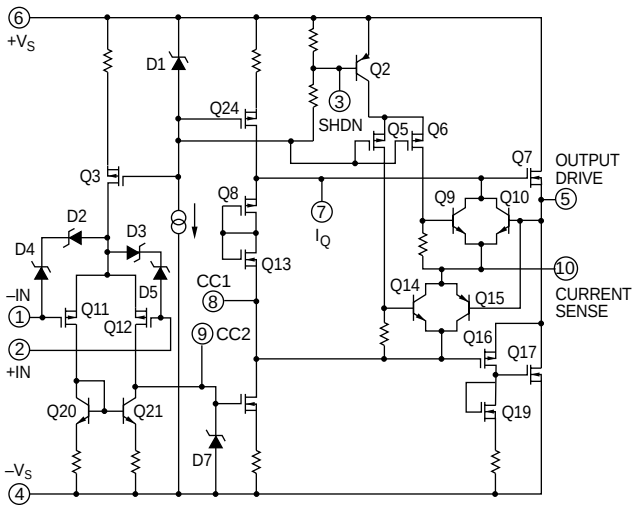
- MAGNETIC DEFLECTION
- PA AUDIO
- MOTOR DRIVE
- NOISE CANCELLATION

DESCRIPTION

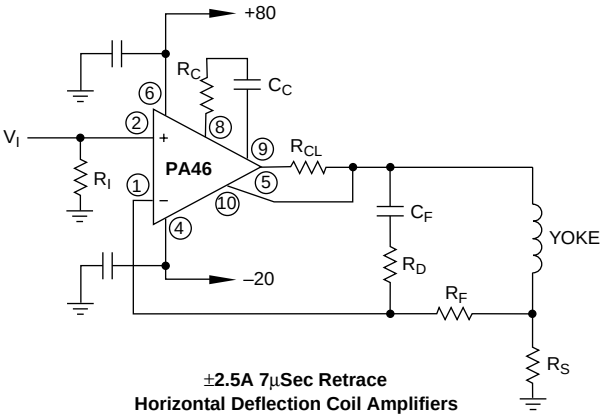
The PA46 is a high power monolithic MOSFET operational amplifier that achieves performance levels unavailable even in many hybrid amplifier designs. Inputs are protected from excessive common mode and differential mode voltages as well as static discharge. The safe operating area (SOA) has no second breakdown limitations and can be observed with all type loads by choosing an appropriate current limiting resistor. External compensation provides the user flexibility in choosing optimum gain and bandwidth for the application. Class C operation with resulting low quiescent current is pin programmable. A shutdown input turns off the output stage.

This circuit utilizes a beryllia oxide (BeO) substrate to minimize thermal resistance. The 10-pin power SIP package is electrically isolated.

EQUIVALENT SCHEMATIC



TYPICAL APPLICATION

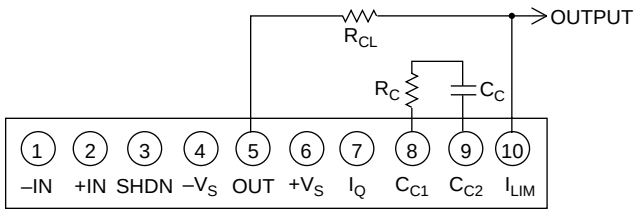


±2.5A 7μSec Retrace
Horizontal Deflection Coil Amplifiers

Horizontal deflection amplifiers require both high speed and low distortion. The speed at which current can be changed in a deflection coil is a function of the voltage available from the op amp. In this application an 80 volt power supply is used for the retrace polarity to provide a 7 μSec retrace time, half of which is required for amplifier slewing. This circuit can perform 15.75 KHz deflection in up to 50μH coils at up to 5A p-p.

EXTERNAL CONNECTIONS

Package: SIP02



C_C is NPO rated for full suppy voltage.

Phase Compensation

Gain	C_C	R_C
≥10	10pF	1KΩ
≥ 1	68pF	1KΩ

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	150V
OUTPUT CURRENT, continuous within SOA	5A
POWER DISSIPATION, continuous @ T_C = 25°C	75W
INPUT VOLTAGE, differential	±16 V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder – 10 sec	220°C
TEMPERATURE, junction	150°C
TEMPERATURE, storage	–65 to +150°C
TEMPERATURE RANGE, powered (case)	–55 to +125°C

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[1]	MIN	TYP	MAX	UNITS
INPUT					
OFFSET VOLTAGE, initial			5	10	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		10	50	µV/°C
OFFSET VOLTAGE, vs supply			8	15	µV/V
OFFSET VOLTAGE, vs time				2	µV √kh
BIAS CURRENT, initial			20	100	pA
BIAS CURRENT, vs supply				2	pA/V
OFFSET CURRENT, initial				200	pA
INPUT IMPEDANCE, DC			10^{11}		Ω
INPUT CAPACITANCE			5		pF
COMMON MODE, voltage range		$\pm V_S$–10			V
COMMON MODE REJECTION, DC		90	106		dB
NOISE, broad band	10kHz BW, R_S = 1KΩ		10		µV RMS
GAIN					
OPEN LOOP at 15Hz		94	106		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	R_L = 500Ω, C_C = 10pF		4.5		MHz
POWER BANDWIDTH	C_C = 10pF, 130V p-p, R_L = 8Ω		66		kHz
PHASE MARGIN	Full temp range, C_C = 68pF, R_L = 10Ω		60		°
OUTPUT					
VOLTAGE SWING	I_O = 5A	$\pm V_S$–10	$\pm V_S$–8		V
CURRENT, continuous		5			A
SETTLING TIME to .1%	10V step, A_V = –10		2		µs
SLEW RATE	C_C = 10pF, R_L = 8Ω		27		V/µs
CAPACITIVE LOAD	A_V = +1, C_C = 68pF	10			nF
RESISTANCE , no load	R_{CL} = 0		150		Ω
POWER SUPPLY					
VOLTAGE[3]	See Note 3	±15	±50	±75	V
CURRENT, quiescent			30	50	mA
CURRENT, quiescent, class C				5	mA
THERMAL[2]					
RESISTANCE, AC junction to case	F > 60Hz			1.3	°C/W
RESISTANCE, DC junction to case	F < 60Hz			1.7	°C/W
RESISTANCE, junction to air	Full temperature range		30		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	°C

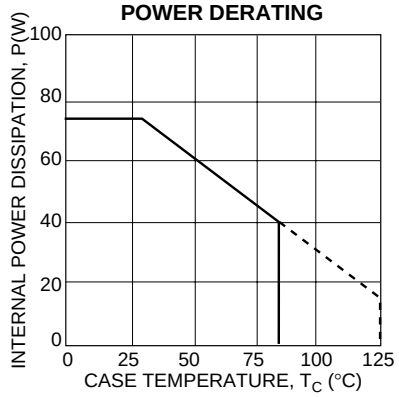
NOTES:
1. Unless otherwise noted T_C = 25°C, C_C = 10pF, R_C = 1KΩ. DC input specifications are ± value given. Power supply voltage is typical rating.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to heatsink data sheet.
3. Derate maximum supply voltage .5 V/°C below case temperature of 25°C. No derating is needed above T_C = 25°C.

CAUTION

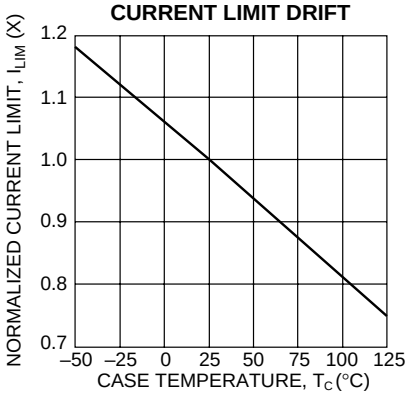
The PA46 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The exposed substrate is beryllia (BeO). Do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

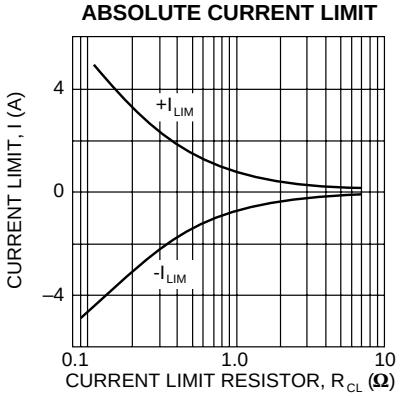
POWER DERATING



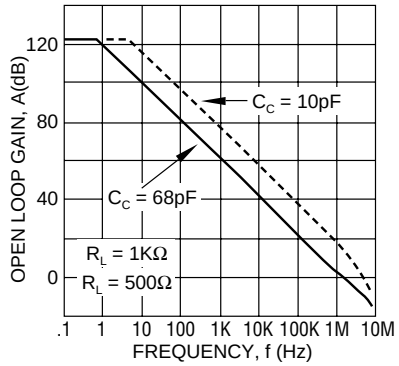
CURRENT LIMIT DRIFT



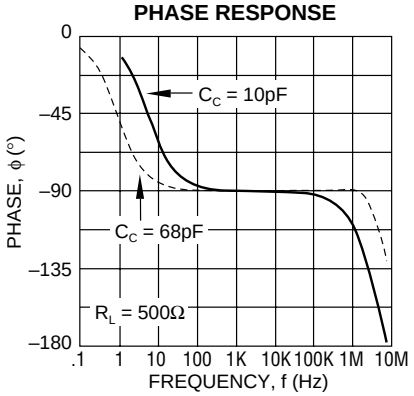
ABSOLUTE CURRENT LIMIT



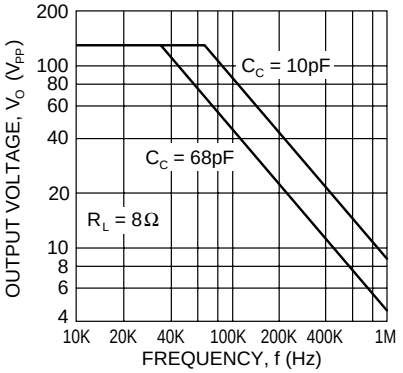
SMALL SIGNAL RESPONSE



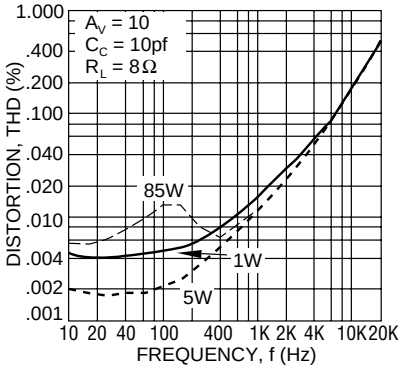
PHASE RESPONSE



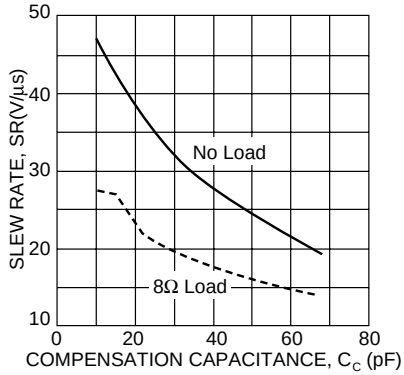
POWER RESPONSE



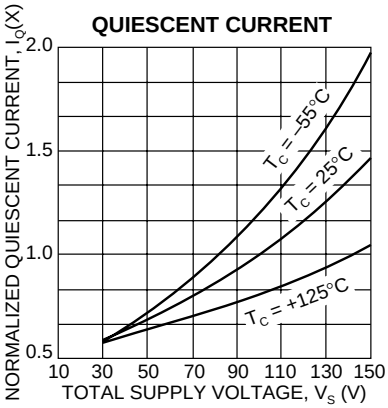
HARMONIC DISTORTION



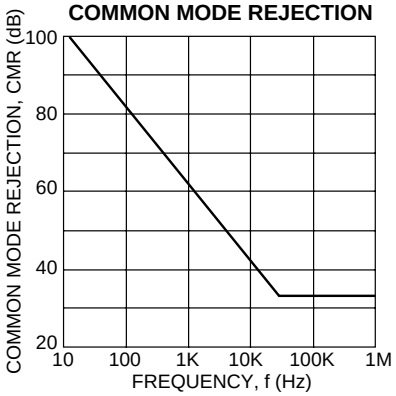
SLEW RATE



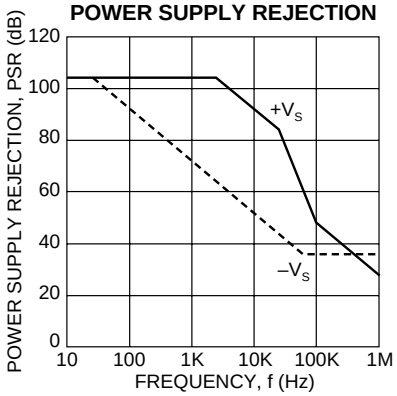
QUIESCENT CURRENT



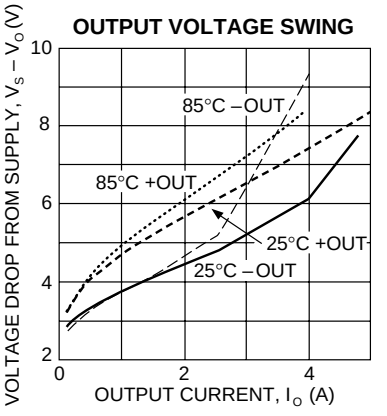
COMMON MODE REJECTION



POWER SUPPLY REJECTION



OUTPUT VOLTAGE SWING



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit and heat sink selection. The "Application Notes" and "Technical Seminar" sections contain a wealth of information on specific types of applications. Package outlines, heat sinks, mounting hardware and other accessories are located in the "Packages and Accessories" section. Evaluation Kits are available for most Apex product models, consult the "Evaluation Kit" section for details. For the most current version of all Apex product data sheets, visit www.apexmicrotech.com.

CURRENT LIMIT

Current limiting is achieved by developing 0.83V on the amplifiers current sense circuit by way of an internal tie to the output drive (pin 5) and an external current sense line (pin 10). A sense resistor R_{CL} is used to relate this sense voltage to a current flowing from output drive.

$$R_{CL} = \frac{0.83 - 0.05 * I_{CL}}{I_{CL}}$$

$$I_{CL} = \frac{0.83}{R_{CL} + 0.05}$$

with a maximum practical value of 16Ω. R_{CL} is added to the typical value of output resistance and affects the total possible swing since it carries the load current. The swing reduction, V_R can be established $V_R = I_{OUT} * R_{CL}$.

INPUT PROTECTION

The PA46 inputs are protected against common mode voltages up to the supply rails, differential voltages up to ±16 volts and static discharge. Differential voltages exceeding 16 volts will be clipped by the protection circuitry. However, if more than a few milliamps of current is available from the input drive source, the protection circuitry could be destroyed. The protection circuitry includes 300 ohm current limiting resistors at each input. This security may be insufficient for severe overdrive of the input. Adding external resistors to the application which limits severe input overdrive current to 1mA, will prevent damage.

STABILITY

The PA46 has sufficient phase margin when compensated for unity gain to be stable with capacitive loads of at least 10nF. However, the low pass circuit created by the sum-point (–in) capacitance and the feedback network may add phase shift and cause instabilities. As a rule, the sum-point load resistance (input and feedback resistors in parallel) should be 1k ohm or less. Alternatively, use a bypass capacitor across the feedback resistor. The time constant of the feedback resistor and bypass capacitor combination should match the time constant of the sum-point resistance and sum-point capacitance.

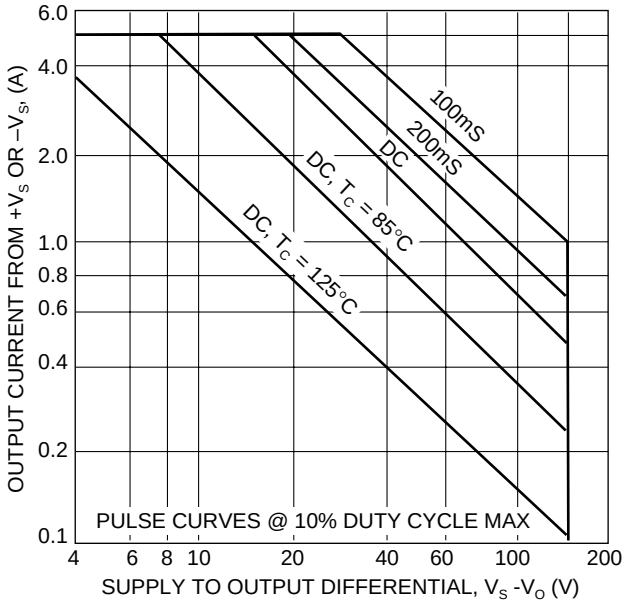
The PA46 is externally compensated and performance can be tailored to the application. The compensation network C_C-R_C must be mounted closely to the amplifier pins 8 and 9 to avoid noise coupling to these high impedance nodes.

SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has limitations from its channel temperature.

NOTE: The output is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

SAFE OPERATING AREA



SHUTDOWN

Pin 3 (SHDN) will shut off the output stage when at least 90µA is pulled from pin 3 to any voltage at least 3 volts less than $+V_s$ (ground, for example).

BIAS CLASS OPTION FOR LOWER QUIESCENT CURRENT

Normally pin 7 (I_Q) is left open. When pin 7 is tied to pin 8 (C_{CI}) the quiescent current in the output stage is disabled. This results in lower quiescent current, but also class C biasing of the output stage.

