5 Channel ESD Protection Array

Features

- Five channels of ESD protection
- ±8 kV contact, ±15 kV air ESD protection per channel (IEC 61000-4-2 standard)
- ±15 kV of ESD protection per channel (HBM)
- Low loading capacitance (3pF typical)
- Low leakage current is ideal for battery-powered devices
- Available in miniature 8-lead MSOP package
- Lead-free version available

Applications

- Consumer electronic products
- Cellular phones
- PDAs
- Notebook computers
- Desktop PCs
- Digital cameras and camcorders
- VGA (video) port protection for desktop and portable PCs

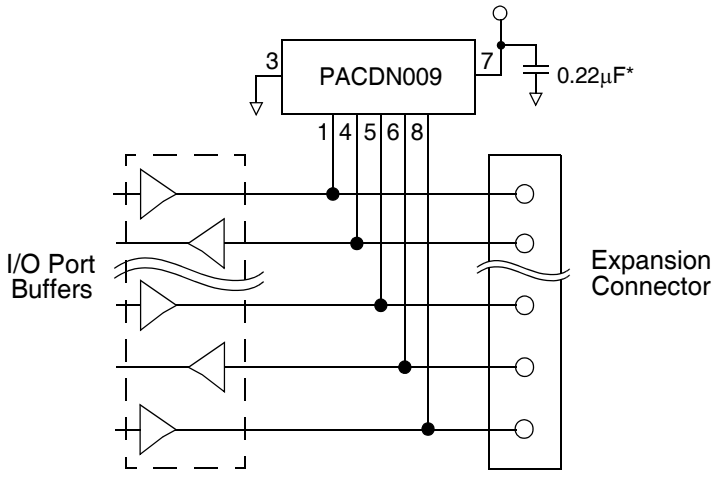
Product Description

The PACDN009 is a diode array designed to provide 5 channels of ESD protection for electronic components or sub-systems. Each channel consists of a pair of diodes which steers an ESD current pulse to either the positive (V_P) or negative (V_N) supply. The PACDN009 protects against ESD pulses up to ±15kV Human Body Model (100 pF capacitor discharging through a 1.5KΩ resistor), and ±8kV contact discharge, per International Standard IEC 61000-4-2.

This device is particularly well-suited for portable electronics (e.g., cellular phones, PDAs, notebook computers) because of its small package footprint, high ESD protection level, and low loading capacitance. It is also suitable for protecting video output lines and I/O ports in computers and peripherals and is ideal for a wide range of consumer electronics products.

The PACDN009 is supplied in an 8-lead MSOP package and is available with optional lead-free finishing.

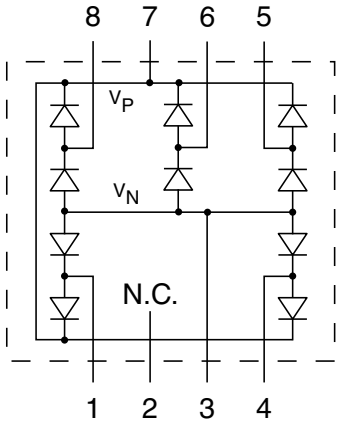
Typical Application Circuit



Handheld/PDA ESD Protection

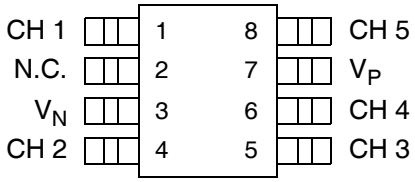
* Capacitor should be placed as close as possible to Pin7

Electrical Schematic



PACKAGE / PINOUT DIAGRAMS

TOP VIEW



PACDN009
8-lead MSOP Package

Note: This drawing is not to scale.

PIN DESCRIPTIONS

PIN	NAME	TYPE	DESCRIPTION
1	CH 1	I/O	ESD Channel
2	N.C.	-	No connect
3	V_N	GND	Negative voltage supply rail or ground reference rail
4	CH 2	I/O	ESD Channel
5	CH 3	I/O	ESD Channel
6	CH 4	I/O	ESD Channel
7	V_P	Supply	Positive voltage supply rail
8	CH 5	I/O	ESD Channel

Ordering Information

PART NUMBERING INFORMATION

		Standard Finish		Lead-free Finish	
Leads	Package	Ordering Part Number[1]	Part Marking	Ordering Part Number[1]	Part Marking
8	MSOP	PACDN009M	D009	PACDN009MR	009R

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	**RATING**	**UNITS**
Supply Voltage (V_P - V_N)	6.0	V
Diode Forward DC Current (Note 1)	20	mA
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C
DC Voltage at any channel input	(V_N - 0.5) to (V_P + 0.5)	V
Package Power Rating MSOP Package	200	mW

Note 1: Only one diode conducting at a time.

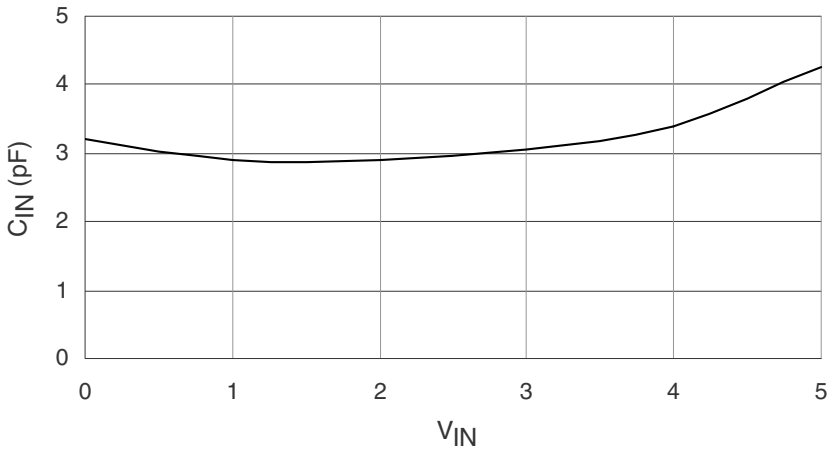
STANDARD OPERATING CONDITIONS		
PARAMETER	**RATING**	**UNITS**
Operating Temperature Range	-40 to +85	°C
Operating Supply Voltage (V_P - V_N)	0 to 5.5	V

ELECTRICAL OPERATING CHARACTERISTICS (SEE NOTE 1)						
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
I_P	Supply Current	(V_P-V_N)=5.5V			10	µA
V_F	Diode Forward Voltage	I_F = 20mA	0.65		0.95	V
V_{ESD}	ESD Protection Peak Discharge Voltage at any channel input, in system a) Human Body Model, MIL-STD-883, Method 3015 b) Contact Discharge per IEC 61000-4-2 c) Air Discharge per IEC 61000-4-2	 Note 3 Notes 2,4 Note 5 Note 5	 ±15 ±8 ±15			 kV kV kV
V_{CL}	Channel Clamp Voltage Positive Transients Negative Transients	@15kV ESD HBM			 V_P + 13.0 V_N - 13.0	 V V
I_{LEAK}	Channel Leakage Current			±0.1	±1.0	µA
C_{IN}	Channel Input Capacitance	@ 1 MHz, V_P=5V, V_N=0V, V_{IN}=2.5V; Note 2 applies		3	5	pF

Note 1: All parameters specified at T_A=25°C unless otherwise noted. V_P = 5V, V_N = 0V unless noted.
Note 2: These parameters guaranteed by design and characterization.
Note 3: From I/O pins to V_P or V_N only. V_P bypassed to V_N with a 0.22µF ceramic capacitor (see Application Information for more details).
Note 4: Human Body Model per MIL-STD-883, Method 3015, $C_{Discharge}$ = 100pF, $R_{Discharge}$ = 1.5KΩ, V_P = 5.0V, V_N grounded.
Note 5: Standard IEC 61000-4-2 with $C_{Discharge}$ = 150pF, $R_{Discharge}$ = 330Ω, V_P = 5.0V, V_N grounded.

Performance Information

Input Capacitance vs. Input Voltage



Typical Variation of C_{IN} vs. V_{IN}

(V_P = 5V, V_N = 0V, 0.1 µF chip capacitor between V_P and V_N)

Application Information

Design Considerations

In order to realize the maximum protection against ESD pulses, care must be taken in the PCB layout to minimize parasitic series inductances on the Supply/ Ground rails as well as the signal trace segment between the signal input (typically a connector) and the ESD protection device. Refer to Figure 1, which illustrates an example of a positive ESD pulse striking an input channel. The parasitic series inductances back to the power supply are represented by L_1 and L_2. The voltage V_{CL} on the line being protected is:

$$V_{CL} = \text{Fwd voltage drop of } D_1 + V_{SUPPLY} + L_1 \times d(I_{ESD}) / dt + L_2 \times d(I_{ESD}) / dt$$

where I_{ESD} is the ESD current pulse, and V_{SUPPLY} is the positive supply voltage.

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC61000-4-2 standard results in a current pulse that rises from zero to 30 Amps in 1ns. Here $d(I_{ESD})/dt$ can be approximated by $\Delta I_{ESD}/\Delta t$, or $30/(1x10^{-9})$. So just 10nH of series inductance (L_1 and L_2 combined) will lead to a 300V increment in V_{CL}!

Similarly for negative ESD pulses, parasitic series inductance from the V_N pin to the ground rail will lead to drastically increased negative voltage on the line being protected.

Another consideration is the output impedance of the power supply for fast transient currents. Most power supplies exhibit a much higher output impedance to fast transient current spikes. In the V_{CL} equation above, the V_{SUPPLY} term, in reality, is given by (V_{DC} + I_{ESD} x R_{OUT}), where V_{DC} and R_{OUT} are the nominal supply DC output voltage and effective output impedance of the power supply respectively. For example, with R_{OUT} equal to 1 ohm, we would see a 10V increment in V_{CL} for a peak I_{ESD} of 10A.

If the inductances and resistance described above are close to zero, the rail-clamp ESD protection diodes will do a good job of protection. However, since this is not possible in practical situations, a bypass capacitor must be used to absorb the very high frequency ESD energy. So for any brand of rail-clamp ESD protection diodes, a bypass capacitor should be connected between the V_P pin of the diodes and the ground plane (V_N pin of the diodes) as shown in the Application Circuit diagram below. A value of 0.22µF is adequate for IEC-61000-4-2 level 4 contact discharge protection (±8kV). Ceramic chip capacitors mounted with short printed circuit board traces are good choices for this application. Electrolytic capacitors should be avoided as they have poor high frequency characteristics. For extra protection, connect a zener diode in parallel with the bypass capacitor to mitigate the effects of the parasitic series inductance inherent in the capacitor. The breakdown voltage of the zener diode should be slightly higher than the maximum supply voltage.

As a general rule, the ESD Protection Array should be located as close as possible to the point of entry of expected electrostatic discharges. The power supply bypass capacitor mentioned above should be as close to the V_P pin of the Protection Array as possible, with minimum PCB trace lengths to the power supply, ground planes and between the signal input and the ESD device to minimize stray series inductance.

Additional Information

See also California Micro Devices Application Notes AP209, “Design Considerations for ESD Protection” and AP219, "ESD Protection for USB 2.0 Systems""

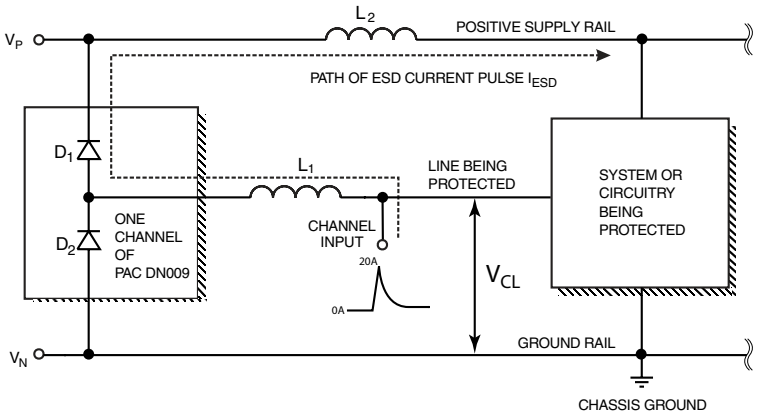


Figure 1. Application of Positive ESD Pulse between Input Channel and Ground

Application Information (cont'd)

Implementation Examples

ESD events are very high-speed pulses with rise times in the range of 1ns or less. To effectively use the PACDN009, the following design guidelines must be observed (as discussed in the application section):

1) The inductance from the V_N and V_P connections of the PACDN009 to ground must be very low. This includes the path through the V_P decoupling capacitor to ground and the path to the power supply (as discussed above).

2) The inductance between the connector pin to be protected and the PACDN009 channel input pin must be kept to a minimum. If there is a large inductance here, the ESD event will find a lower impedance path which will more likely be through the device to be protected. Figure 2 shows the implementation schematic and Figure 3 shows a possible layout for the PACDN009. In figure 3, notice the large VCC and ground areas with multiple via connections to the underlying reference planes and the positioning of the bypass capacitor. Note how the signal lines to be protected flow from the connector to the PACDN009 and then out to the device to be protected (Figure 3). This daisy chaining provides a low impedance path from the connector to the PACDN009 and a higher impedance path from the PACDN009 to the protected device.

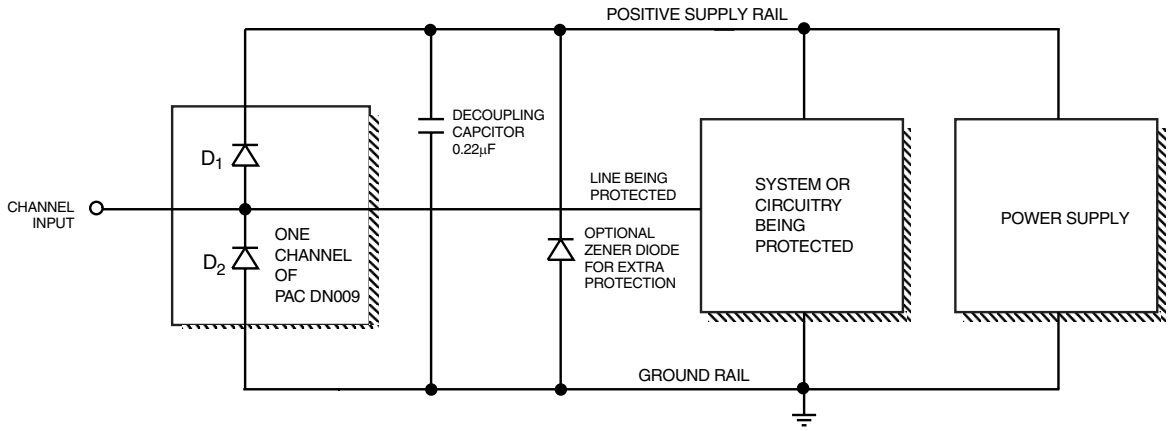


Figure 2. Typical ESD protection implementation

Application Information (cont'd)

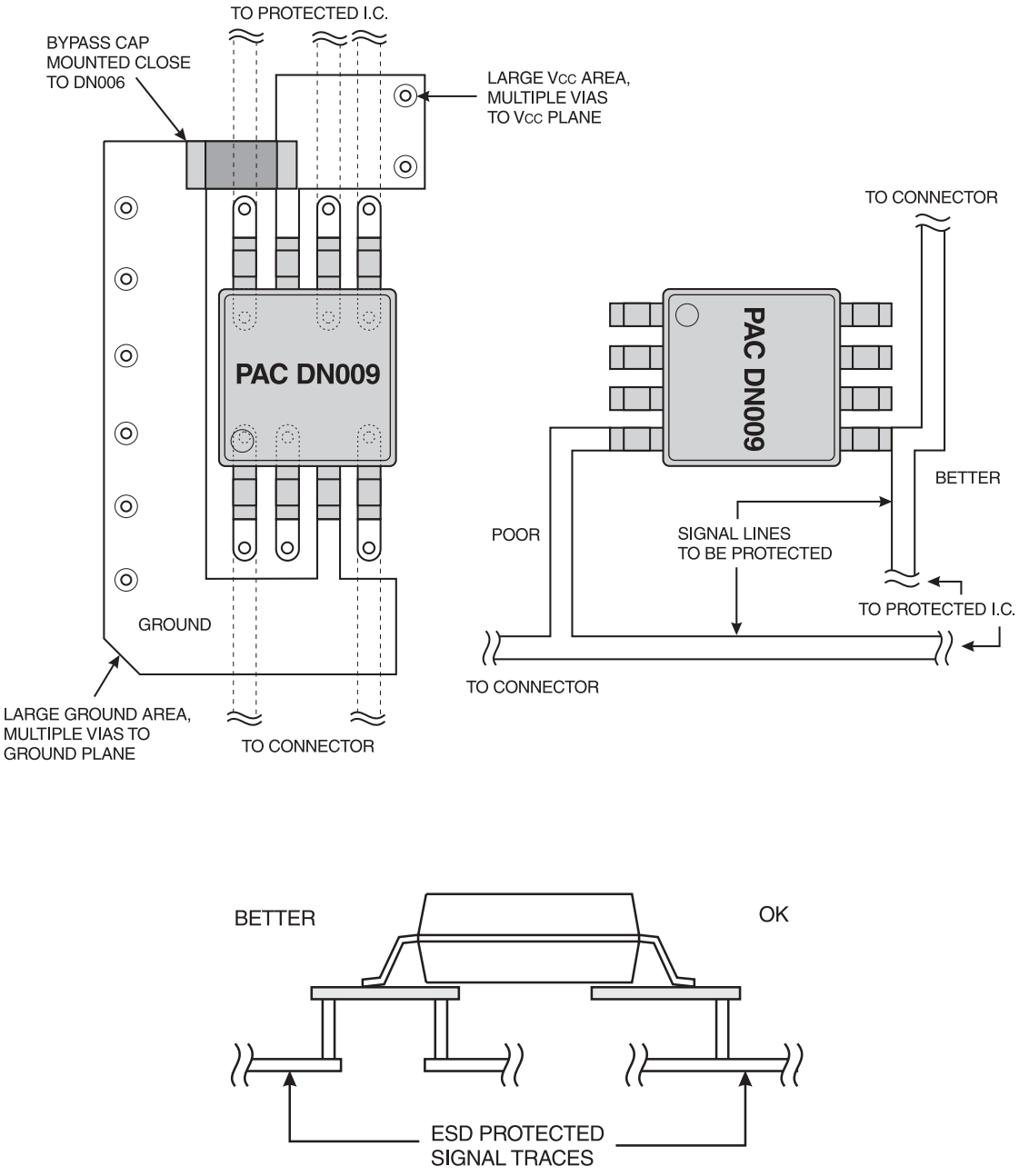


Figure 3. PCB Layout Recomendation

Mechanical Details

MSOP Mechanical Specifications

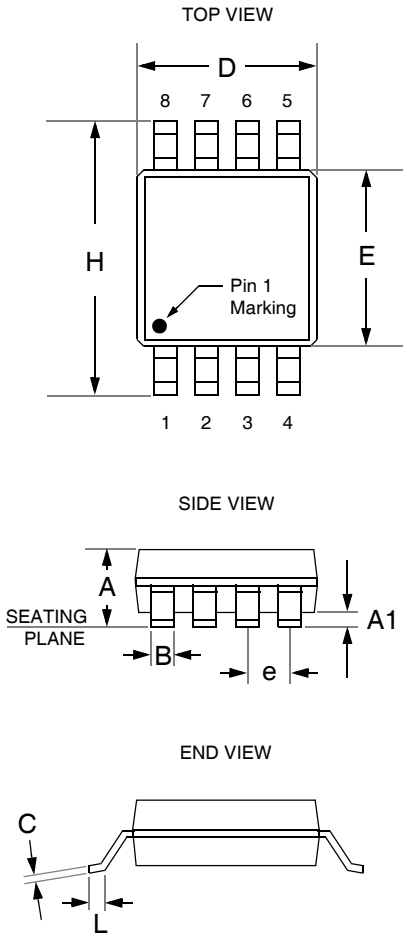
The PACDN009 is supplied in an 8-lead MSOP package. Dimensions are presented below.

For complete information on the MSOP-8 package, see the specific California Micro Devices Package Information document.

PACKAGE DIMENSIONS				
Package	MSOP			
Leads	8			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	0.87	1.17	0.034	0.046
A1	0.05	0.25	0.002	0.010
B	0.30 (typ)		0.012 (typ)	
C	0.18		0.007	
D	2.90	3.10	0.114	0.122
E	2.90	3.10	0.114	0.122
e	0.65 BSC		0.025 BSC	
H	4.78	4.98	0.188	0.196
L	0.52	0.54	0.017	0.025
# per tube	80 pieces*			
# per tape and reel	4000 pieces			
Controlling dimension: inches				

* This is an approximate number which may vary.

Mechanical Package Diagrams



Package Dimensions for MSOP-8