VGA PROTECTION AND TERMINATION NETWORK

Features

- 7 channel ESD protection
- 15KV ESD protection (HBM)
- 8KV contact, 15KV air discharge ESD protection per IEC 1000-4-2 (Level 4)
- Low loading capacitance, 4.5pF typical

Application

- ESD protection for VGA (video) port in PCs and notebooks.

Product Description

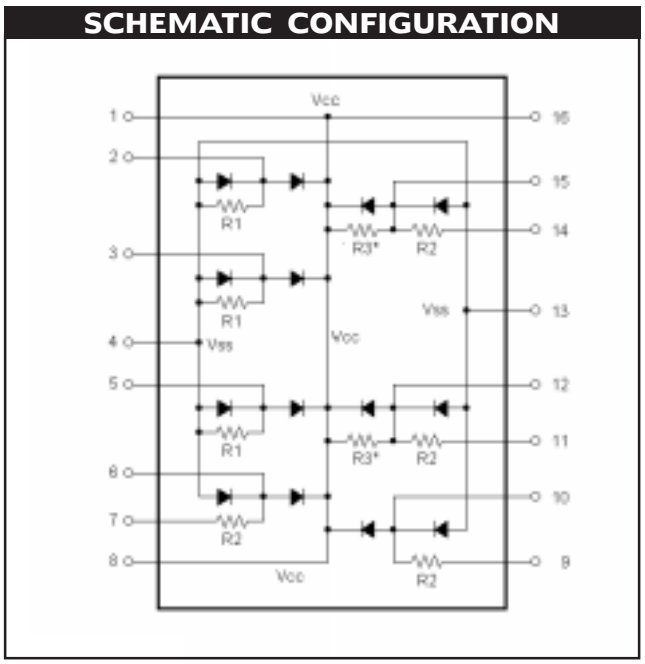
The PAC VGA-100/101 acts as a transmission line terminating and ESD protection device. It provides 75 Ohm parallel terminations for the R, G, B lines and series terminations for the Horizontal and Vertical Sync lines and two monitor ID lines which provide 'Plug and Play' logic signals. In addition, all interface lines provide Level 4 ESD protection per the IEC1000-4-2 contact discharge Specification. The PAC VGA-100 provides internal pull-up resistors for the two monitor ID lines. The PAC VGA-101 omits these internal pull-ups so that different pull-up resistor values can be added externally.

ABSOLUTE MAXIMUM RATINGS

Diode Forward DC Current (Note 1)	20mA
Storage Temperature	-65°C to 150°C
Operating Temperature Range	0°C to 70°C
DC Voltage at any Channel Input	V_N-0.5V to V_P+0.5V

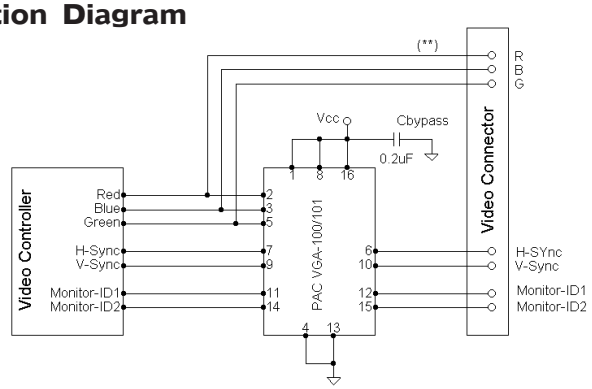
Note 1: Only one diode conducting at a time.

SCHEMATIC CONFIGURATION



R1=75Ω, **R2**=33Ω, **R3**=2.2KΩ **(VGA-100** only)
(*) **R3** Removed **(VGA-101** only)

Typical Connection Diagram



(**) For best ESD protection, minimize trace lengths between PAC VGA-100/101 and the video connector.

STANDARD SPECIFICATIONS			
Parameter	**Min.**	**Typ.**	**Max.**
Operating Supply Voltage (V_P - V_N)			5.5V
R/G/B termination resistor (R1) tolerance			±5%
Series termination resistor (R2) tolerance			±5%
Monitor ID pull-up resistor resistor (R3) tolerance			±10%
Diode Forward Voltage, I_F = 20mA, T = 25°C	0.65V		0.95V
Diode reverse breakdown voltage, T = 25°C			
Top Diode (Cathode to V_P)	17.0V		
Bottom Diode (Anode to V_N)	25.0V		
ESD Protection			
Peak Discharge Voltage at pins 7, 9, 11 and 14			
Human Body Model, Method 3015 (Note 6)	-4KV		+4KV
Peak Discharge Voltage at pins 2, 3, 5, 6, 10, 12, 15			
In-system (Note 2)			
Human Body Model, Method 3015 (Notes 3, 4)	-15KV		+15KV
Contact Discharge per IEC 1000-4-2 (Note 5)	-8KV		+8KV
Channel Clamp Voltage @ 15KV ESD HBM, T = 25°C			
at pins 2, 3, 5, 6, 10, 12, 15. (Notes 3, 4)			
Positive transients			V_P + 13.0V
Negative transients			V_N - 13.0V
Channel Leakage Current, T = 25°C		0.1 µA	1.0 µA
Channel Input Capacitance (Measured @ 1 MHz)			
at pins 2, 3, 5, 6, 10, 12, 15.			
V_P = 5V, V_N = 0V, V_{INPUT} = 2.5V		4.5pF	7pF
Package Power Rating			
QSOP Package			800mW

Note 2: From I/O pins to V_P or V_N only. V_P bypassed to V_N with 0.2 µF ceramic capacitor.
Note 3: Human Body Model per MIL-STD-883, Method 3015, $C_{Discharge}$=100pF, $R_{Discharge}$=1.5KΩ, V_P=5V, V_N=GND.
Note 4: This parameter is guaranteed by characterization.
Note 5: Standard IEC1000-4-2 with $C_{Discharge}$=150pF, and $R_{Discharge}$=330Ω, V_P=5V, V_N=GND.
Note 6: These pins are not connected directly to the video connector, and therefore are not subject to direct ESD strikes.

Application Information: See California Micro Devices' Application Note AP-209 "Design Considerations for ESD Protection"

STANDARD PART ORDERING INFORMATION				
Package		**Ordering Part Number**		
Pins	**Style**	**Tubes**	**Tape & Reel**	**Part Marking**
16	QSOP	PACVGA-100/T	PACVGA-100/R	PACVGA100
16	QSOP	PACVGA-101/T	PACVGA-101/R	PACVGA101