General Description

The PAH8001EI-QG is a high performance and low power CMOS-process optical sensor with Green LED and DSP integrated serving as a Heart Rate Detection (HRD) sensor. It is based on optical technology which measures the variation of human blood movement in the vessel.

Key Features

- Heart rate detection function (HRD)
- Ultra-low power consumption, power saving mode during time of no touch movement
  - LPT sleep1
  - LPT sleep2
- Flexible sleep rate control
- Flexible communication interface
  - I^2C
  - 4-wire SPI
  - 2-wire SPI
- I^2C interface up to 1 Mbit/s
- SPI interface up to 1 Mbit/s
- Hardware reset support
- Hardware power down support
- Integrated chip-on-board LED with wavelength of 525nm

Applications

- Healthcare on wearable device
- Photoplethysmogram waveform

Key Sensor Performance

Parameter	Value
Max. frame rate	3000 fps
Supply voltage	VDDM: 3.0~3.6V VDDIO: 1.62~3.6V Note: suggest customer could consider 3.3V to avoid voltage drop issue.
Power consumption	1.5 mA at Normal mode 160 uA at Sleep1 mode 40 uA at Sleep2 mode 15uA at power down mode Note: including LED current, w/o I/O toggling, package only
Operating temperature (at junction)	-20 to +60 °C
Package	Land Grid Array. Size 3.0 x 4.7 mm with 16 pins

Ordering Information

Part Number	Packing	Description
PAH8001EI-QG	16-Pin LGA	CMOS HRD optical sensor

PixArt Imaging Inc. E-mail:fae_service@pixart.com.tw

Pin Configuration

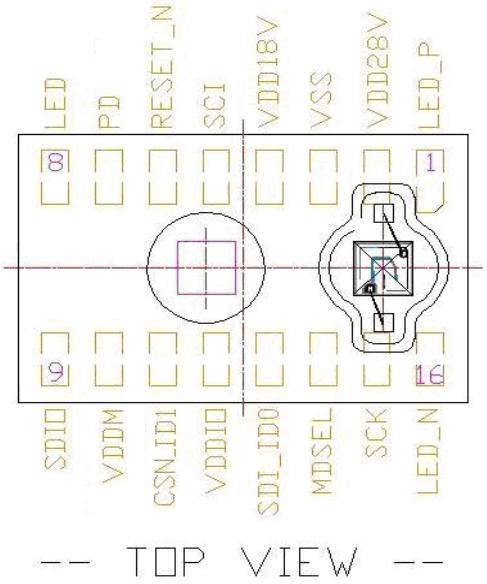

Figure 2. Pin Configuration

Pin No.	Name	Type	Description
1	LED_P		LED Anode Provide VDDM supply voltage
2	VDD28V	PWR	Analog circuit power regulator output Must connect 0.1uF capacitor to GND
3	VSS		GND
4	VDD18V	PWR	Analog and digital circuit power regulator output Must connect 0.1uF capacitor to GND
5	SCI	OUT	Touch on/off INT (Active high)
6	RESET_N	IN	Hardware control to enter reset mode Level High: leave reset mode Level Low: enter reset mode Set to high when not used
7	PD	IN	PD: Hardware control to enter power down mode Build-in 1M ohm pull-down resistor Level High: enter power down mode Level Low: leave power down mode Set to low when not used
8	LED		LED driver connection Must connect to LED_N
9	SDIO	IN/OUT	4-wire SPI: data output pin 2-wire SPI: data in-out pin I2C: data in-out pin
10	VDDM	PWR	Power supply (3.0v~3.6v) for internal power regulator
11	CSN_ID1	IN	4-wire SPI: chip select, active low I2C: address set ID1(Tri state IO)
12	VDDIO	PWR	I/O power supply. VDDIO: 1.62V~3.6V
13	SDI_ID0	IN	4-wire SPI: data input pin I2C: address set ID0(Tri state IO)
14	MDSEL	IN	Tri state IO For select 2-wire SPI/ 4-wire SPI/ I2C mode I2C: Pull down 4-wire SPI: Floating 2-wire SPI: Pull high(Tied to VDDIO)
15	SCK	IN	2-wire SPI/ 4-wire SPI/ I2C: clock pin
16	LED_N		LED Cathode Must connect to LED

Package Outline Dimension

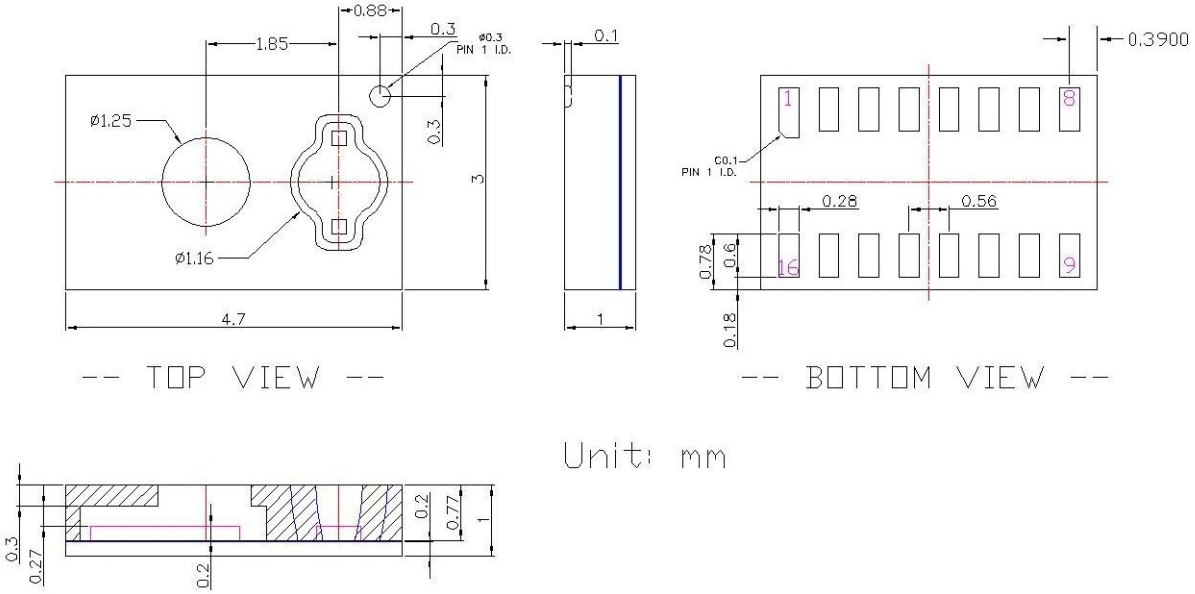

Figure 3. Package Outline Drawing

Reference Application Circuit

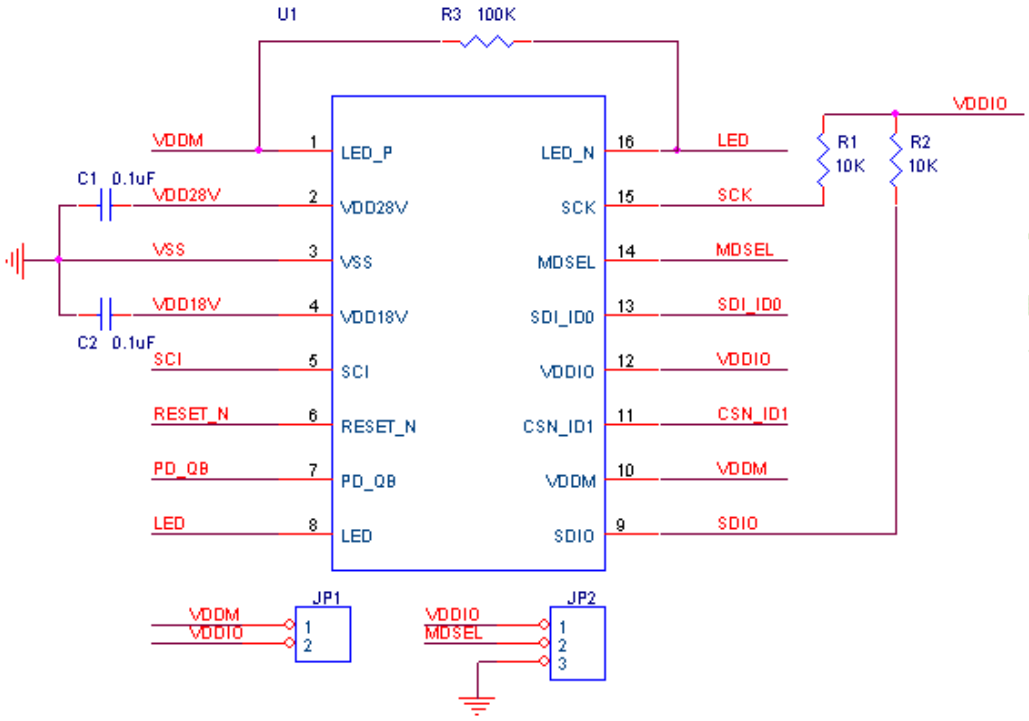

Figure 4. Application Circuit

Design Notes:

1. VDDM & VDDIO: 3.0V~3.6V (3.3V System) --> JP1 Short
2. VDDM: 3.0V~3.6V, VDDIO: 1.62V~1.98V (1.8V System) --> JP1 Open
3. R1, R2 10K for I2C Only
4. VDD28V, VDD18V must be connected 0.1uF capacitor to GND
5. SCI can connect to MCU HW INT as Touch INT for power saving (Active high)
6. VDDM and VDDIO power noise need to under 100mV
7. MDSEL of JP2 tied to VDDIO for 2SPI, floating for 4SPI, and tied to GND for I2C
8. ID0 and ID1 can directly bond to VDDIO or GND based on your I2C ID selection
9. LED pin must be pulled high 100K resistor to VDDM for internal circuit voltage reference

PCB Layout Guide

1. 0.1uF Capacitors of VDD18V and VDD28V must be closed to 8001.
2. If SDI_ID0 and CSN_ID1 (I2C ID selection) are floating, please don't close to any clock trace.
3. Trace width of VDDM/VDDIO/VDD28V/VDD18V/LED_P/LED_N/LED must be at least 8 mil.