PAL16RA8

20-pin Asynchronous TTL Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 30 ns maximum propagation delay and 20 MHz f_{MAX}
- Individually programmable asynchronous clock, preset, reset, and enable
- Registered or combinatorial outputs
- Programmable polarity
- Programmable replacement for high-speed TTL logic
- TTL-level register preload for testability
- Easy design with PALASM® software
- Programmable on standard PAL® device programmers
- 20-pin DIP and 20-pin PLCC packages save space

GENERAL DESCRIPTION

The PAL16RA8 offers asynchronous clocking for each of the eight flip-flops in the device. The eight macrocells feature programmable clock, preset, reset, and enable, and all can operate asynchronously to other macrocells in the same device. The PAL16RA8 also has flip-flop bypass, allowing any combination of registered and combinatorial outputs.

The PAL16RA8 utilizes Advanced Micro Devices' advanced junction-isolated bipolar process and fuse-link technology. The devices provide user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

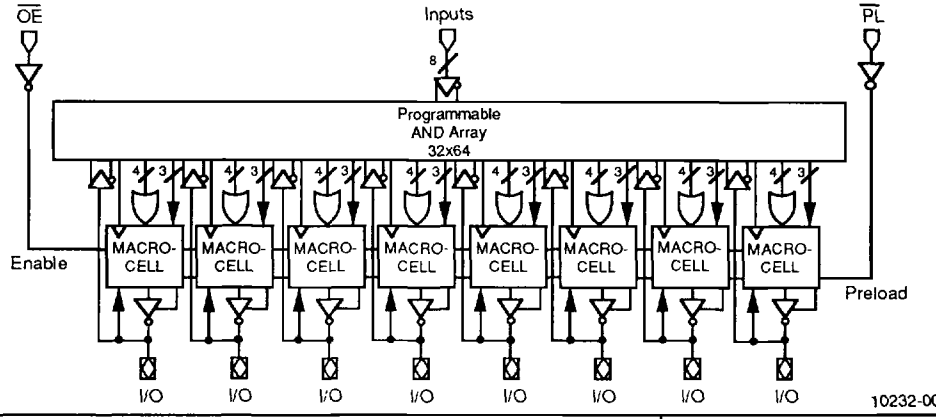
The PAL16RA8 allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

Product terms with all fuses opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state. Registers consist of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock. Unused input pins should be tied to V_{CC} or GND.

The entire PAL device family is supported by the PALASM software package. The PAL family is programmed on conventional PAL device programmers.

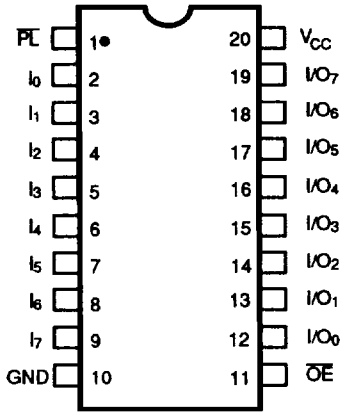
BLOCK DIAGRAM



Publication # 10232 Rev. B Amendment /0
Issue Date: January 1990

CONNECTION DIAGRAMS

DIP



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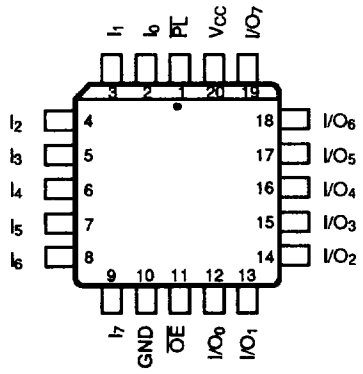
PLCC



Note:
Pin 1 is marked for orientation.

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2

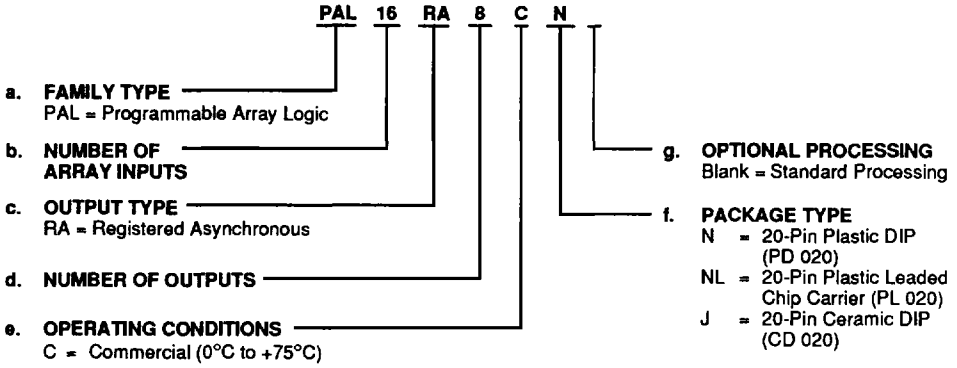
PIN DESIGNATIONS

GND	Ground
I	Input
I/O	Input/Output
$\overline{OE}$	Output Enable
$\overline{PL}$	Preload
V_{CC}	Supply Voltage

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. **Family Type**
b. **Number of Array Inputs**
c. **Output Type**
d. **Number of Outputs**
e. **Operating Conditions**
f. **Package Type**
g. **Optional Processing**



Valid Combinations	
PAL16RA8	CN, CNL, CJ

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with MMI logo.

FUNCTIONAL DESCRIPTION

The PAL16RA8 has eight dedicated input lines and eight programmable I/O macrocells. The Registered Asynchronous (RA) macrocell is shown in Figure 1. Pin 1 serves as global register preload and pin 11 serves as global output enable. Programmable output polarity is available to provide user-programmable output polarity for each individual macrocell.

The programmable functions in the PAL16RA8 are automatically configured from the user's design specification, which can be in a number of formats. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to a programmer, configures the device according to the user's desired function.

Programmable Preset and Reset

In each macrocell, two product lines are dedicated to asynchronous preset and asynchronous reset. If the preset product line is HIGH, the Q output of the register becomes logic 1. If the reset product line is HIGH, the Q output of the register becomes a logic 0. The operation of the programmable preset and reset overrides the clock.

Combinatorial/Registered Outputs

If both the preset and reset product lines are HIGH, the flip-flop is bypassed (Bypass Mode) and the output becomes combinatorial. Otherwise, the output is from the register (Registered Mode). Each output can be configured to be combinatorial or registered.

Programmable Clock

The clock input to each flop-flop comes from the programmable array, allowing any flip-flop to be clocked independently if desired.

Three-State Outputs

The devices provide a product term dedicated to local output control. There is also a global output control pin. The output is enabled if both the global output control pin is LOW and the local output control product term is HIGH. If the global output control pin is HIGH, all outputs will be disabled. If the local output control product term is LOW, then that output will be disabled.

Security Fuse

A security fuse is also provided to prevent unauthorized copying of PAL device patterns. Once the fuse is programmed, the circuitry enabling verification is permanently disabled, and the array will read as if every array fuse is programmed. With verification not operating, it is impossible to simply copy the PAL device pattern on a PAL device programmer.

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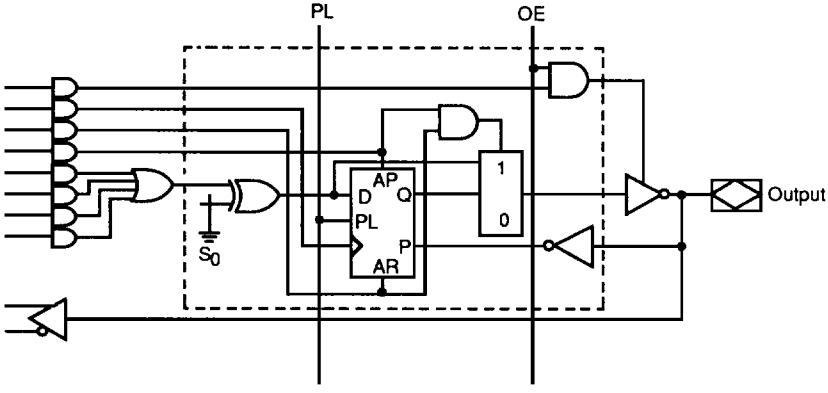

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Figure 1. PAL16RA8 Macrocell

Programmable Polarity

The outputs can be programmed either active-LOW or active-HIGH. This is represented by the Exclusive-OR gate shown in the PAL16RA8 logic diagram. When the output polarity fuse is programmed, the lower input to the Exclusive-OR gate is HIGH, so the output is active-HIGH. Similarly when the output polarity fuse is intact, the output is active-LOW. The programmable output polarity feature allows the user a higher degree of flexibility when writing equations.

Programming

The PAL16RA8 can be programmed on standard logic programmers. Programmers approved by Advanced Micro Devices are listed in the Programmer Reference Guide.

Register Preload

The register on the PAL16RA8 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery. Register preload is controlled by a TTL-level signal, making it a convenient board-level initialization function.

Quality and Testability

The PAL16RA8 offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The PAL16RA8 is fabricated with AMD's junction-isolated process, utilizing TiW fuses.

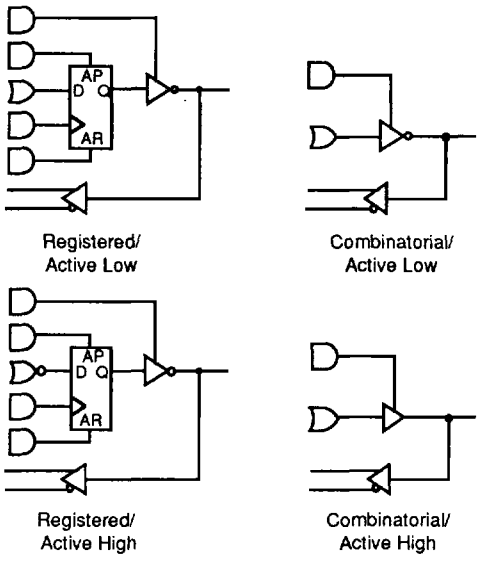

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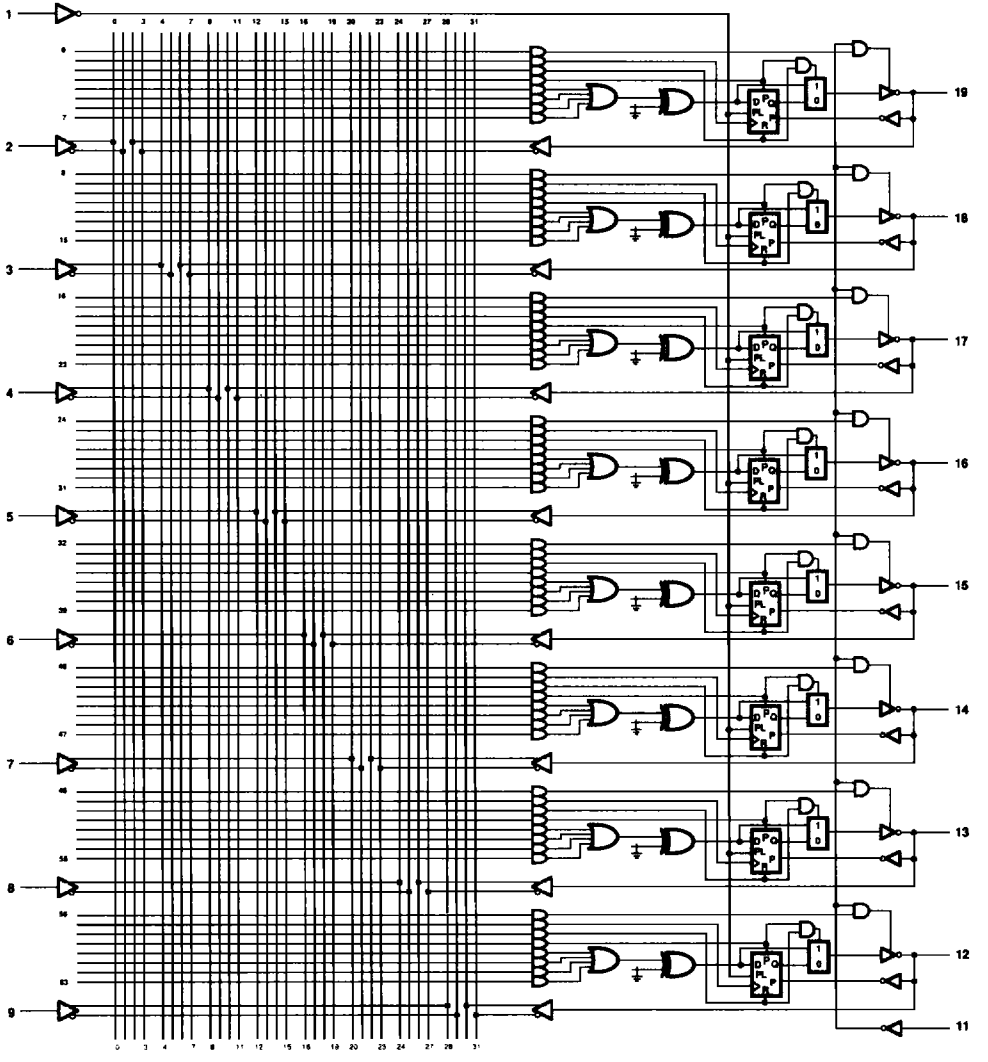
Figure 2. Macrocell Configurations

LOGIC DIAGRAM

PAL16RA8



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ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−1.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 8 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = −18 mA, V_{CC} = Min.		−1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		−250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	−30	−130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		170	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

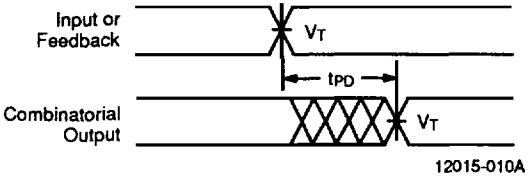
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description			Min. (Note 2)	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output	Active Low			30	ns
		Active High			35	ns
t_S	Setup Time from Input or Feedback to Clock			20		ns
t_H	Hold Time	Active Low		10		ns
		Active High		0		ns
t_{CO}	Clock to Output or Feedback			10	30	ns
t_{AP}	Asynchronous Preset to Registered Output				35	ns
t_{APW}	Asynchronous Preset Width			20		ns
t_{AR}	Asynchronous Reset to Registered Output				40	ns
t_{ARW}	Asynchronous Reset Width			20		ns
t_{WL}	Clock Width	LOW		20		ns
t_{WH}		HIGH		20		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	20		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	25		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				20	ns
t_{EA}	Input to Output Enable Using Product Term Control				30	ns
t_{ER}	Input to Output Disable Using Product Term Control				30	ns

Notes:

1. See Switching Test Circuit for test conditions.
2. Output delay minimums are measured under best-case conditions.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

SWITCHING WAVEFORMS



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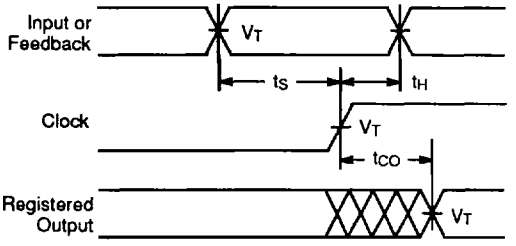
Combinatorial Output



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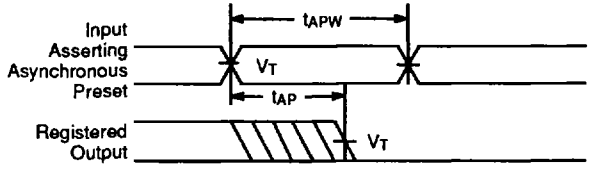
Registered Output



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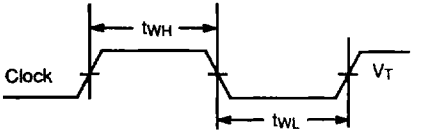
Asynchronous Preset



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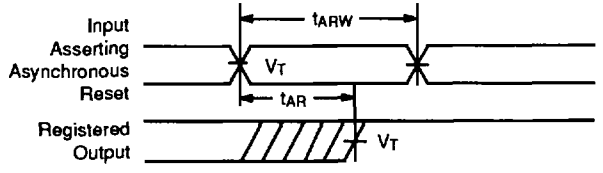
Clock Width



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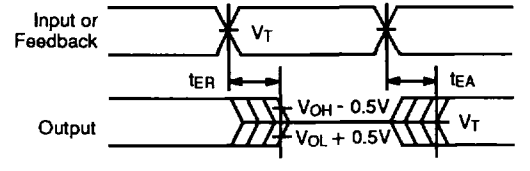
Asynchronous Reset



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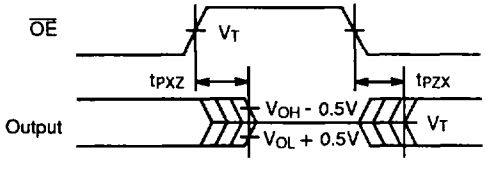
Input to Output Disable/Enable



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$\overline{OE}$ to Output Disable/Enable

Notes:

1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2–5 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

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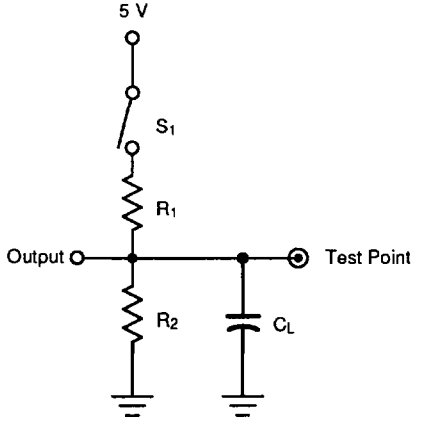
SWITCHING TEST CIRCUIT



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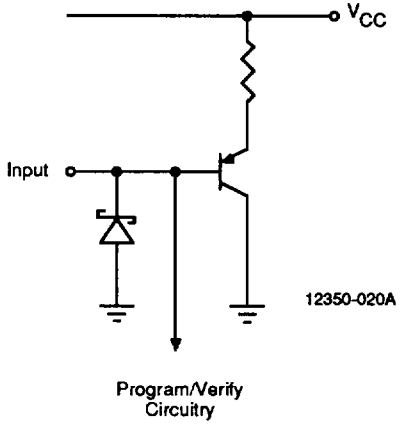
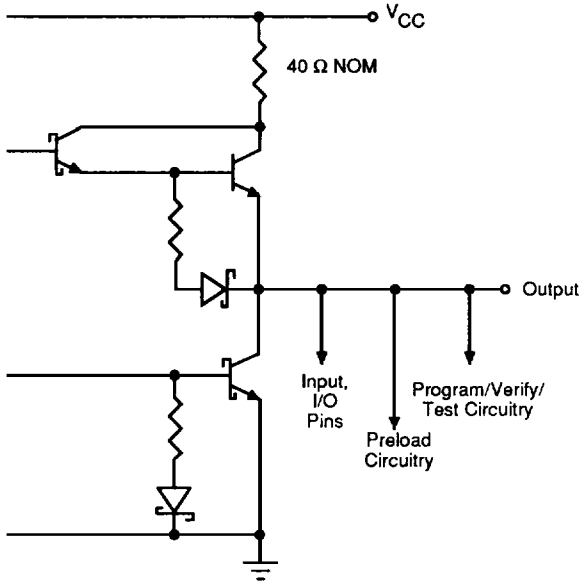
Specification	S_1	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	50 pF	560 Ω	1.1 kΩ	1.5 V
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

INPUT/OUTPUT EQUIVALENT SCHEMATICS

Typical Input



Typical Output

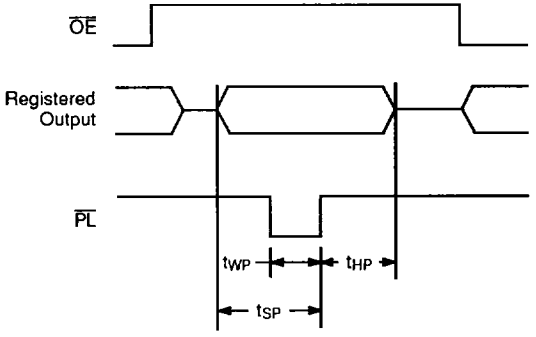


OUTPUT REGISTER PRELOAD

The preload function allows the register to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for preloading follows.

1. Set $\overline{OE}$ to V_{IHP} to disable output registers.
2. Apply either V_{IHP} or V_{ILP} to all registered outputs. Leave combinatorial outputs floating.
3. Pulse $\overline{PL}$ from V_{IHP} to V_{ILP} to V_{IHP}.
4. Remove V_{ILP}/V_{IHP} from all registered output pins.
5. Lower $\overline{OE}$ to V_{ILP} to enable the output registers.
6. Verify V_{OL}/V_{OH} at all registered output pins. Note that because of the output inverter, a register that has been preloaded HIGH will provide a LOW at the output.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{ILP}	Low-level input voltage	0	0	0.5	V
V_{IHP}	High-level input voltage	2.4	5.0	5.5	V
t_{SP}	Preload setup time	25			ns
t_{WP}	Preload pulse width	35			ns
t_{HP}	Preload hold time	25			ns



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Output Register Preload Waveform