



# PAL20R8 Family

## 24-pin TTL Programmable Array Logic

### DISTINCTIVE CHARACTERISTICS

- As fast as 7.5 ns maximum propagation delay
- Popular 24-pin architectures: 20L8, 20R8, 20R6, 20R4
- Programmable replacement for high-speed TTL logic
- Power-up reset for initialization
- Easy design with PALASM<sup>®</sup> software
- Programmable on standard PAL<sup>®</sup> device programmers
- 24-pin SKINNYDIP<sup>®</sup> and 28-pin PLCC packages save space

### GENERAL DESCRIPTION

The PAL20R8 Family (PAL20L8, PAL20R8, PAL20R6, PAL20R4) is AMD's standard 24-pin PAL device family. The devices provide user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

The family allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

In addition, the PAL device provides the following options:

- Variable input/output pin ratio
- Programmable three-state outputs
- Registers with feedback

Product terms with all connections opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state. Registers consist of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock. Unused input pins should be tied to V<sub>cc</sub> or GND.

The entire PAL device family is supported by the PALASM software package. The PAL family is programmed on conventional PAL device programmers with appropriate personality and socket adapter modules. See the Programmer Reference Guide for approved programmers. Once the PAL device is programmed and verified an additional connection may be opened to prevent pattern readout. This feature secures proprietary circuits.



### PRODUCT SELECTOR GUIDE

DEVICE	DEDICATED INPUTS	OUTPUTS	PRODUCT TERMS/ OUTPUT	FEEDBACK	ENABLE
PAL20L8	14	6 comb. 2 comb.	7 7	I/O -	prog. prog.
PAL20R8	12	8 reg.	8	reg.	pin
PAL20R6	12	6 reg. 2 comb.	8 7	reg. I/O	pin prog.
PAL20R4	12	4 reg. 4 comb.	8 7	reg. I/O	pin prog.

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## PERFORMANCE OPTIONS

		(Commercial)	
Speed ( $t_{PD}$ , ns)	35	A-2	
	25	B-2	A
	15		B
	10		-10
	7.5		-7
		105	210
		Power ( $I_{CC}$ , mA)	

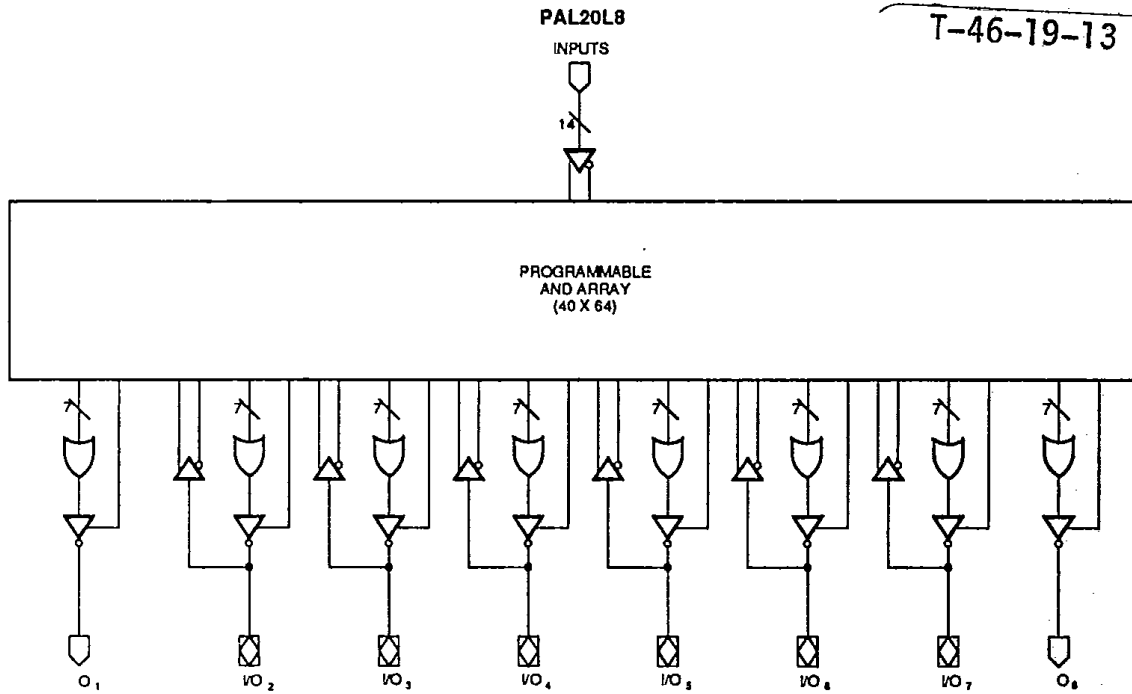
### Note:

For low power and high speed, the EE CMOS PALCE20V8 can directly replace the PAL20R8 Family.

## OPERATING RANGES

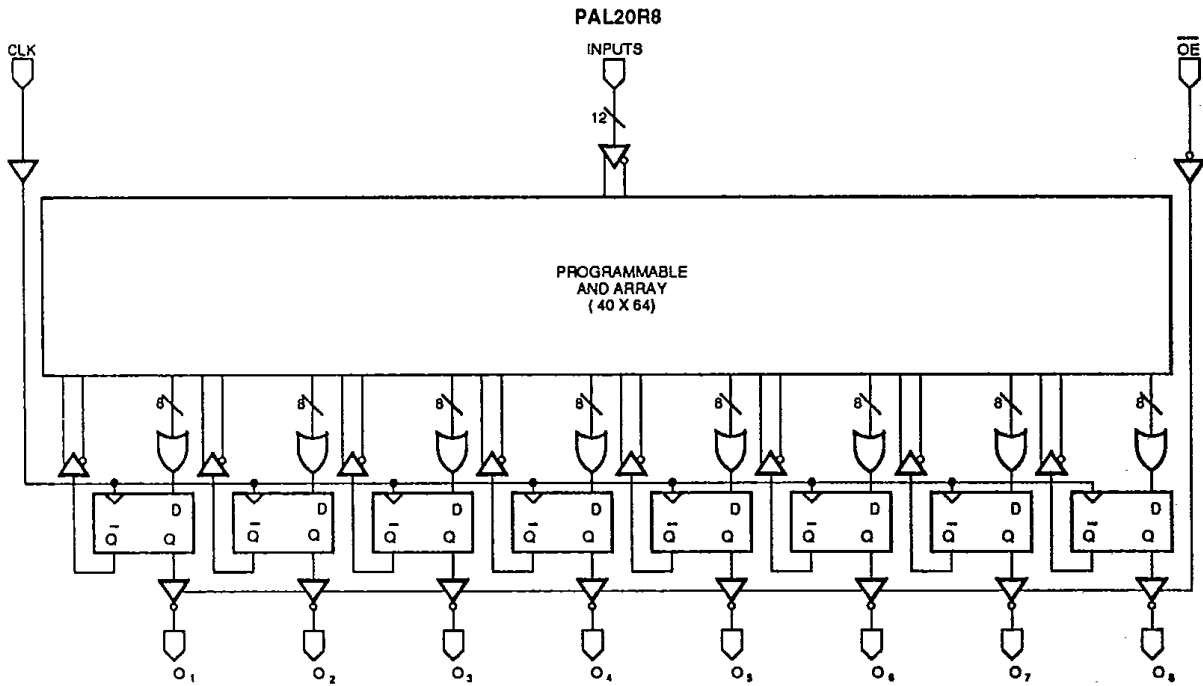
Commercial	Military
-7	-12
-10	-15
B (15 ns)	B (20 ns)
B-2 (25 ns)	
A (25 ns)	A (30 ns)
A-2 (35 ns)	A-2 (50 ns)

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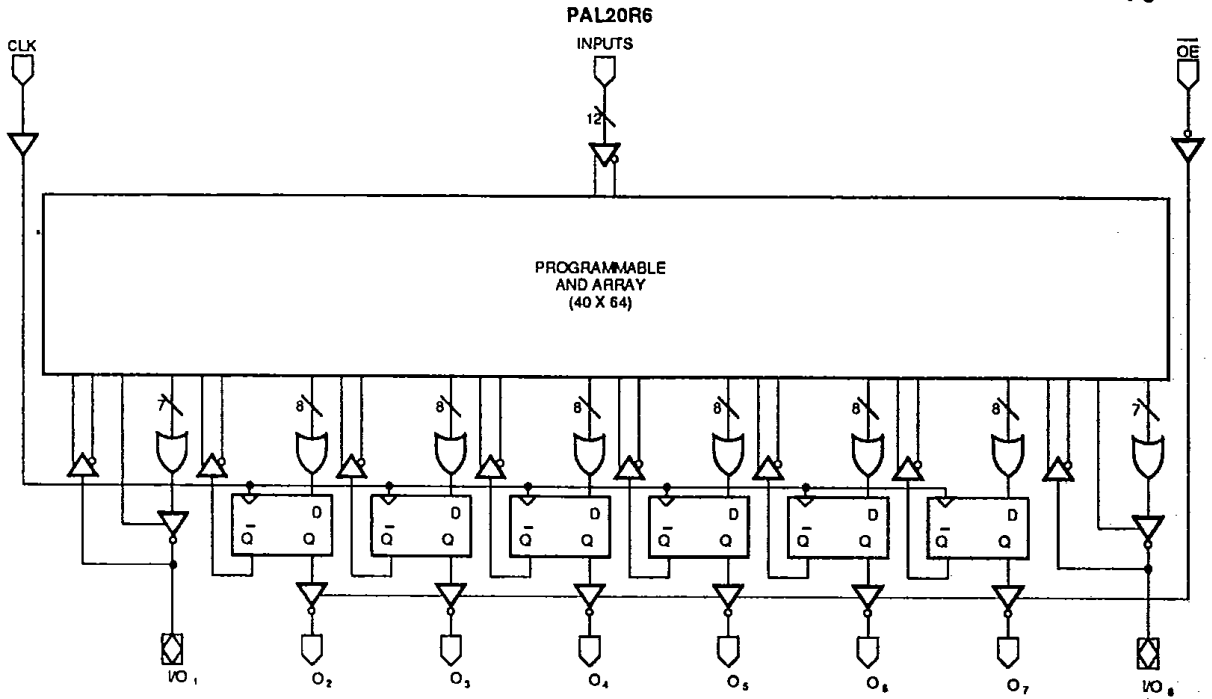


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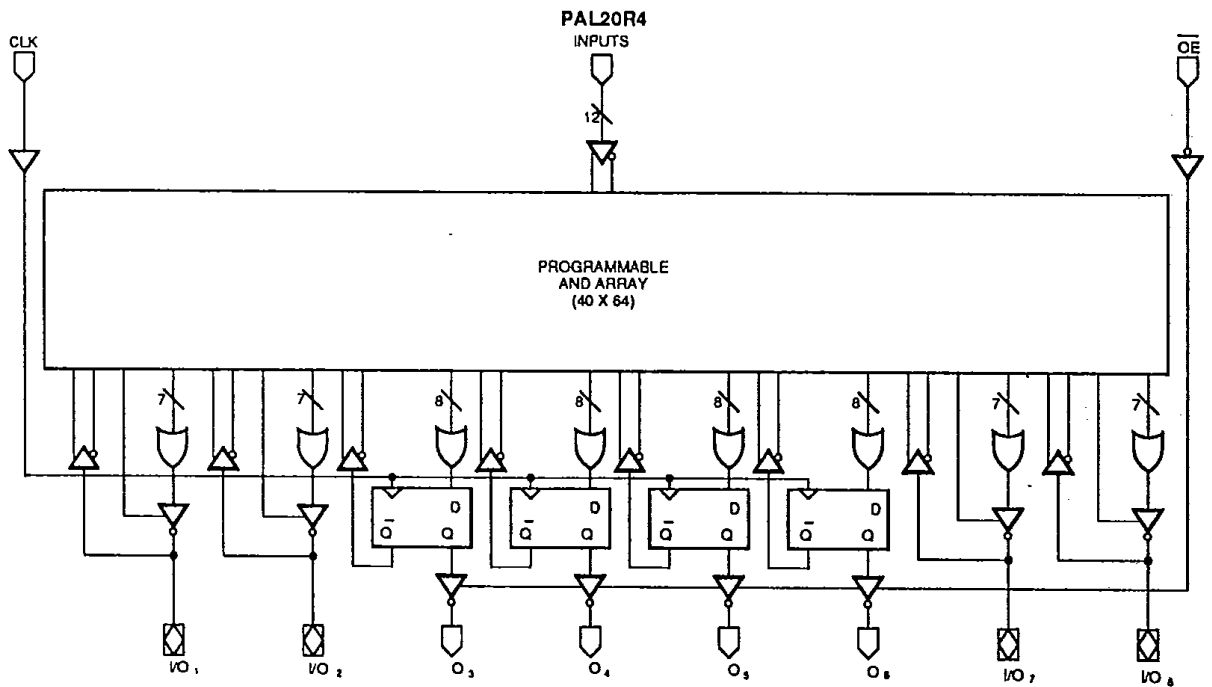
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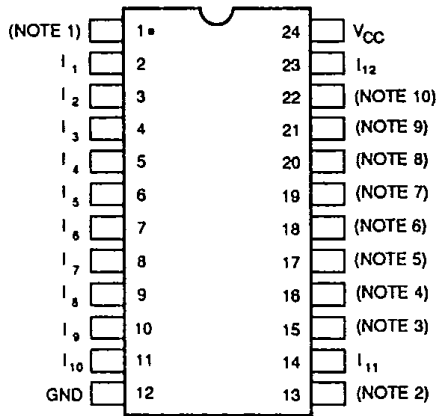
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Top View

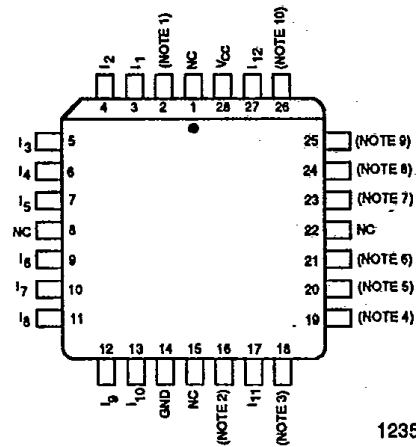
SKINNYDIP/FLATPACK



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PLCC/LCC

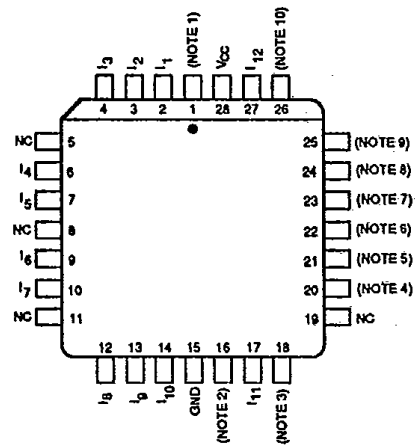
JEDEC: Applies to -7(-12 mil), -10(-15 mil),  
B-2 Series Only



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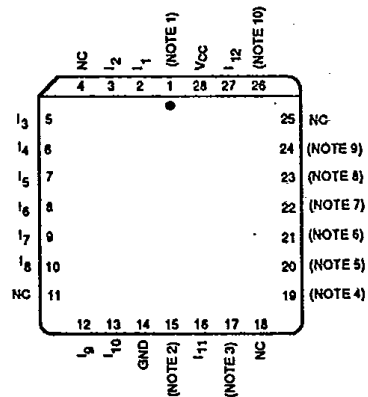
PLCC

Applies to B, A, A-2 Series Only



LCC

Applies to B, A, A-2 Series Only



Note	20L8	20R8	20R6	20R4
1	I <sub>0</sub>	CLK	CLK	CLK
2	I <sub>13</sub>	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
3	O <sub>1</sub>	O <sub>1</sub>	I/O <sub>1</sub>	I/O <sub>1</sub>
4	I/O <sub>2</sub>	O <sub>2</sub>	O <sub>2</sub>	I/O <sub>2</sub>
5	I/O <sub>3</sub>	O <sub>3</sub>	O <sub>3</sub>	O <sub>3</sub>
6	I/O <sub>4</sub>	O <sub>4</sub>	O <sub>4</sub>	O <sub>4</sub>
7	I/O <sub>5</sub>	O <sub>5</sub>	O <sub>5</sub>	O <sub>5</sub>
8	I/O <sub>6</sub>	O <sub>6</sub>	O <sub>6</sub>	O <sub>6</sub>
9	I/O <sub>7</sub>	O <sub>7</sub>	O <sub>7</sub>	I/O <sub>7</sub>
10	O <sub>8</sub>	O <sub>8</sub>	I/O <sub>8</sub>	I/O <sub>8</sub>

PIN DESIGNATIONS

- CLK Clock
- GND Ground
- I Input
- I/O Input/Output
- NC No Connect
- O Output
- $\overline{OE}$  Output Enable
- V<sub>CC</sub> Supply Voltage

Note:  
Pin 1 is marked for orientation.



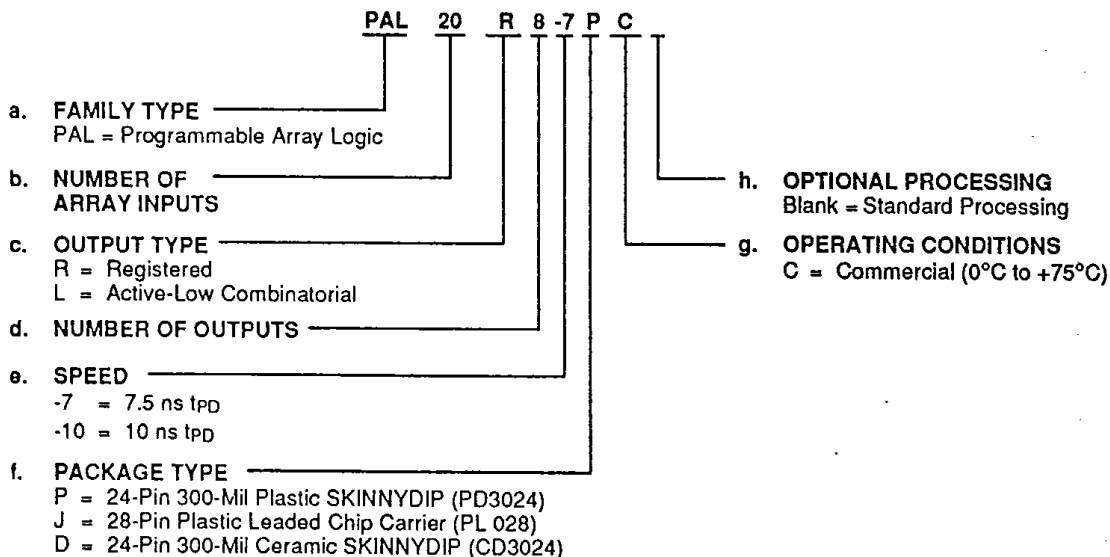
# ORDERING INFORMATION

## Commercial Products (AMD Marking Only)

T-46-19-13

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

- a. Family Type
- b. Number of Array Inputs
- c. Output Type
- d. Number of Outputs
- e. Speed
- f. Package Type
- g. Operating Conditions
- h. Optional Processing



Valid Combinations		
PAL20L8	-7, -10	PC, JC, DC
PAL20R8		
PAL20R6		
PAL20R4		

### Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with AMD logo.

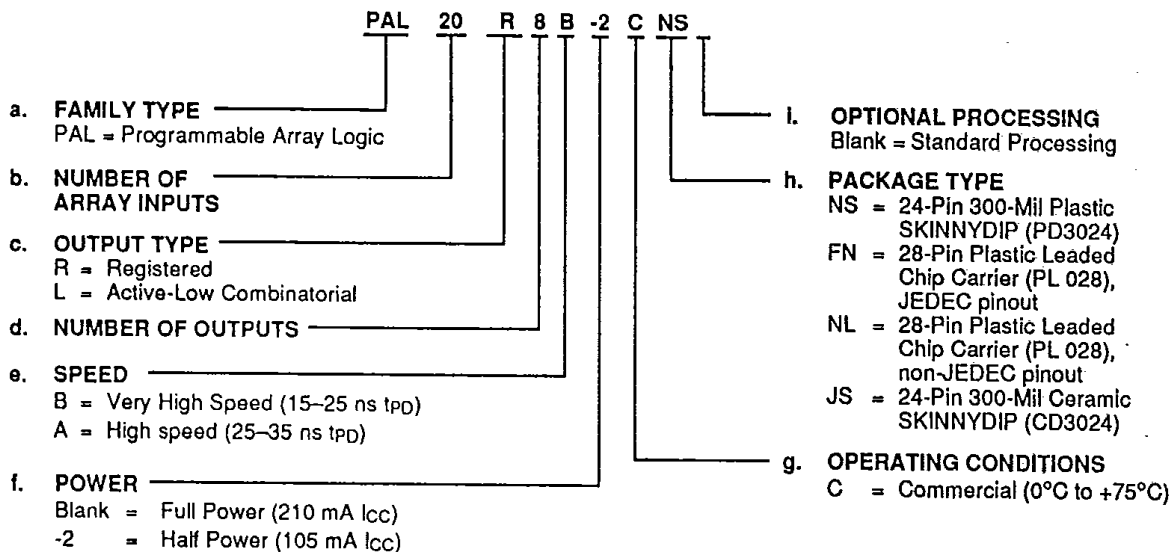
# ORDERING INFORMATION

## Commercial Products (MMI Marking Only)

T-46-19-13

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

- a. Family Type
- b. Number of Array Inputs
- c. Output Type
- d. Number of Outputs
- e. Speed
- f. Power
- g. Operating Conditions
- h. Package Type
- i. Optional Processing



Valid Combinations		
PAL20L8,	B-2	CNS, CFN, CJS
PAL20R8,		
PAL20R6,	B, A,	CNS, CNL, CJS
PAL20R4	A-2	

### Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with MMI logo.

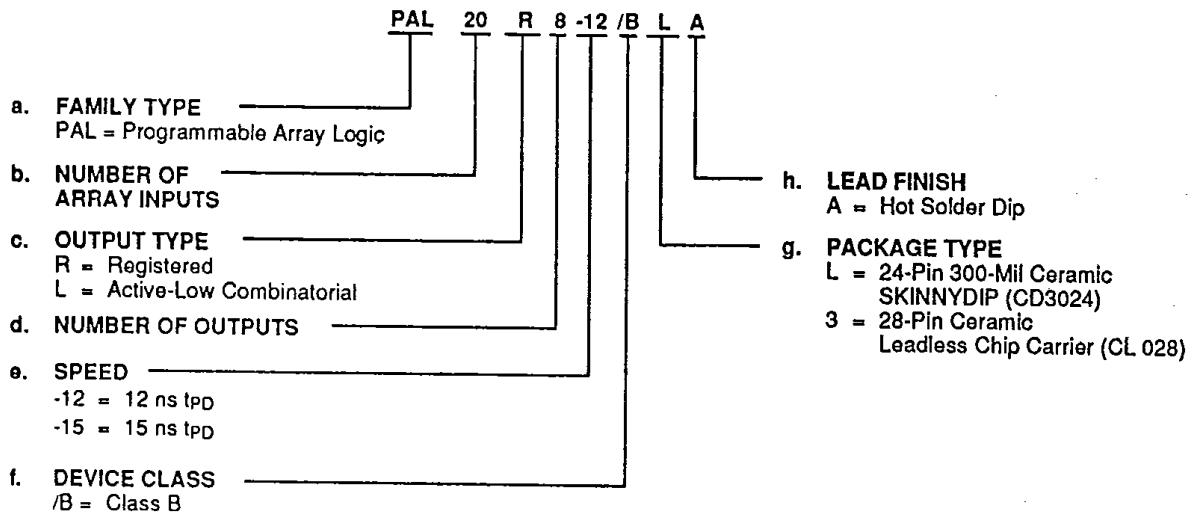
# ORDERING INFORMATION

## APL Products (AMD Marking Only)

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AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:

- a. Family Type
- b. Number of Array Inputs
- c. Output Type
- d. Number of Outputs
- e. Speed
- f. Device Class
- g. Package Type
- h. Lead Finish



Valid Combinations		
PAL20L8	-12, -15	/BLA, /B3A
PAL20R8		
PAL20R6		
PAL20R4		

### Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note: Marked with AMD logo.

### Group A Tests

Group A Tests consist of Subgroups: 1, 2, 3, 7, 8, 9, 10, 11.

### Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Methods 1015, Conditions A through E. Test conditions are selected at AMD's option.

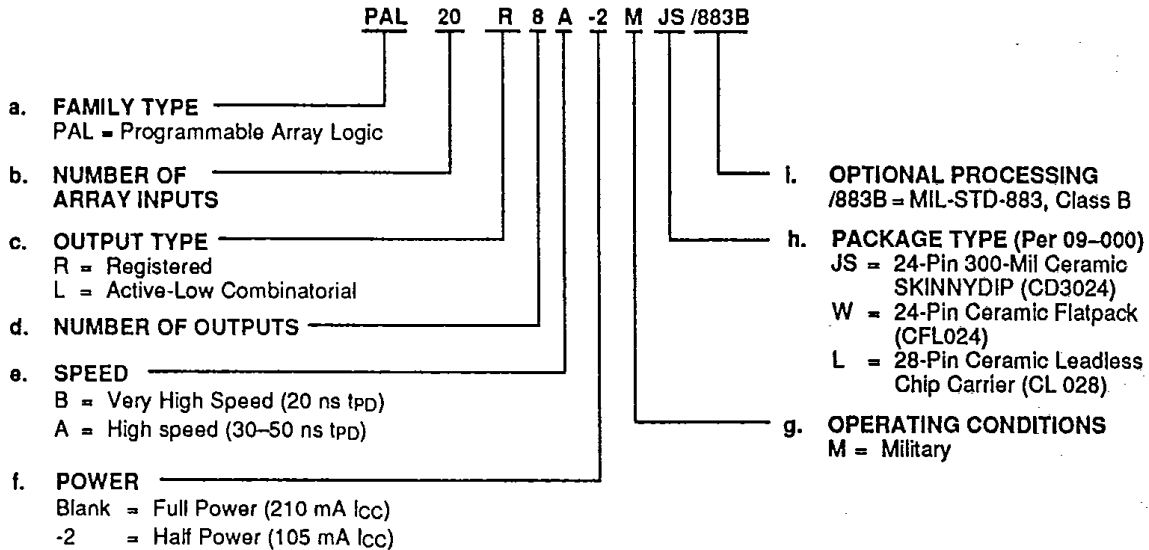


**ORDERING INFORMATION**  
**APL Products (MMI Marking Only)**

T-46-19-13

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:

- a. Family Type
- b. Number of Array Inputs
- c. Output Type
- d. Number of Outputs
- e. Speed
- f. Power
- g. Operating Conditions
- h. Package Type
- i. Optional Processing



Valid Combinations		
PAL20L8		MJS/883B,
PAL20R8	B, A,	MW/883B,
PAL20R6	A-2	ML/883B
PAL20R4		

**Valid Combinations**

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with MMI logo.

**Group A Tests**

Group A Tests consist of Subgroups: 1, 2, 3, 7, 8, 9, 10, 11.

**Military Burn-In**

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Methods 1015, Conditions A through E. Test conditions are selected at AMD's option.

## FUNCTIONAL DESCRIPTION

### Standard 24-pin PAL Family

The standard 24-pin PAL family is comprised of four different devices, including both registered and combinatorial devices. All parts are produced with a fuse link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Information on approved programmers can be found in the Programmer Reference Guide. Extra test words are pre-programmed during manufacturing to ensure extremely high field programming yields, and provide extra test paths to achieve excellent parametric correlation.

### Variable Input/Output Pin Ratio

The registered devices have twelve dedicated input lines, and each combinatorial output is an I/O pin. The PAL20L8 has fourteen dedicated input lines, and only six of the eight combinatorial outputs are I/O pins. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V<sub>CC</sub> or GND.

### Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. On combinatorial outputs, a product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled. On registered outputs, an input pin controls the enabling of the three-state outputs.

### Registers with Feedback

Registered outputs are provided for data storage and synchronization. Registers are composed of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock input.

### Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PAL20R8 Family will be HIGH due to the active-low outputs. The V<sub>CC</sub> rise

must be monotonic and the reset delay time is 1000 ns maximum.

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### Register Preload

#### Applies to -7 (-12 Mil), -10 (-15 Mil), Series Only

The register on the listed Series can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

### Security Fuse

After programming and verification, a PAL20R8 Family design can be secured by programming the security fuse. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is unprogrammed. An exception is the -7 (-12 Mil) Series, where the array will read as if every fuse is programmed.

### Pinouts

All members of the PAL20R8 Family have the same SKINNYDIP pinouts independent of technology, performance, and operating conditions. Because the 24-pin SKINNYDIP requires four no-connects when mapped into the 28-pin PLCC/LCC packages, the PLCC/LCC pinouts can vary.

Two different PLCC pinouts are offered. Newer devices and all future devices will follow the JEDEC electronics committee's standard pinout ("JEDEC pinout") with no-connects on pins 1, 8, 15, and 22. The devices following this pinout are the -7, -10, and B-2 Series. Older devices retain their original pinouts, with no-connects on pins 5, 8, 11, and 19. These include the B, A, and A-2 Series.

PAL20R8 Family devices with the MMI marking indicate the PLCC pinout by the package designator: FN indicates JEDEC, and NL indicates non-JEDEC. Devices with the AMD marking all follow the JEDEC pinout.

Two different LCC pinouts are offered for military products. Newer devices and all future devices will follow the JEDEC pinout with no-connects on pins 1, 8, 15, and 22. These include the -12 and -15 Series. Older devices retain their original pinouts, with no-connects on pins 4, 11, 18, and 25. These include the B, A, and A-2 Series.

Series	Com'l PLCC No-connects	Mil LCC No-connects
-7, -10, B-2	1, 8, 15, 22 (JEDEC)	N/A
-12, -15	N/A	1, 8, 15, 22 (JEDEC)
B, A, A-2	5, 8, 11, 19	4, 11, 18, 25

## Quality and Testability

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The PAL20R8 Family offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

## Technology

The high-speed -7 (-12 Mil) and -10 (-15 Mil) Series are fabricated with AMD's advanced oxide-isolated bipolar process. This process reduces parasitic capacitances and minimum geometries to provide higher performance. The array connections are formed with proven PtSi fuses for the -7 and TiW fuses for the -10. The B, B-2, A, and A-2 Series are fabricated with AMD's junction-isolated process, utilizing TiW fuses.

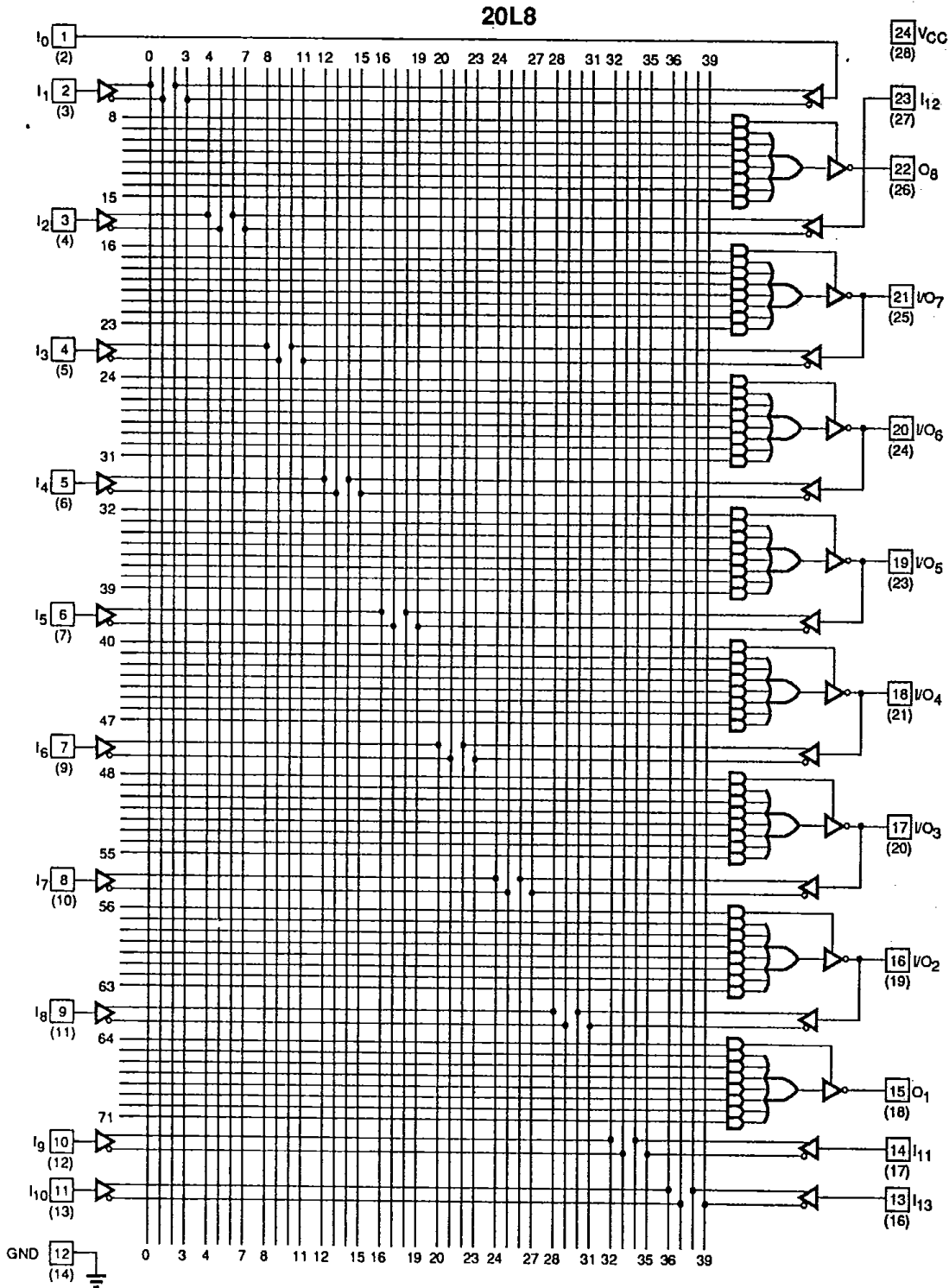


# LOGIC DIAGRAM

## DIP (JEDEC PLCC and LCC) Pinouts

See Connection Diagrams for B, A, A-2 Series PLCC/LCC Pinouts

T-46-19-13



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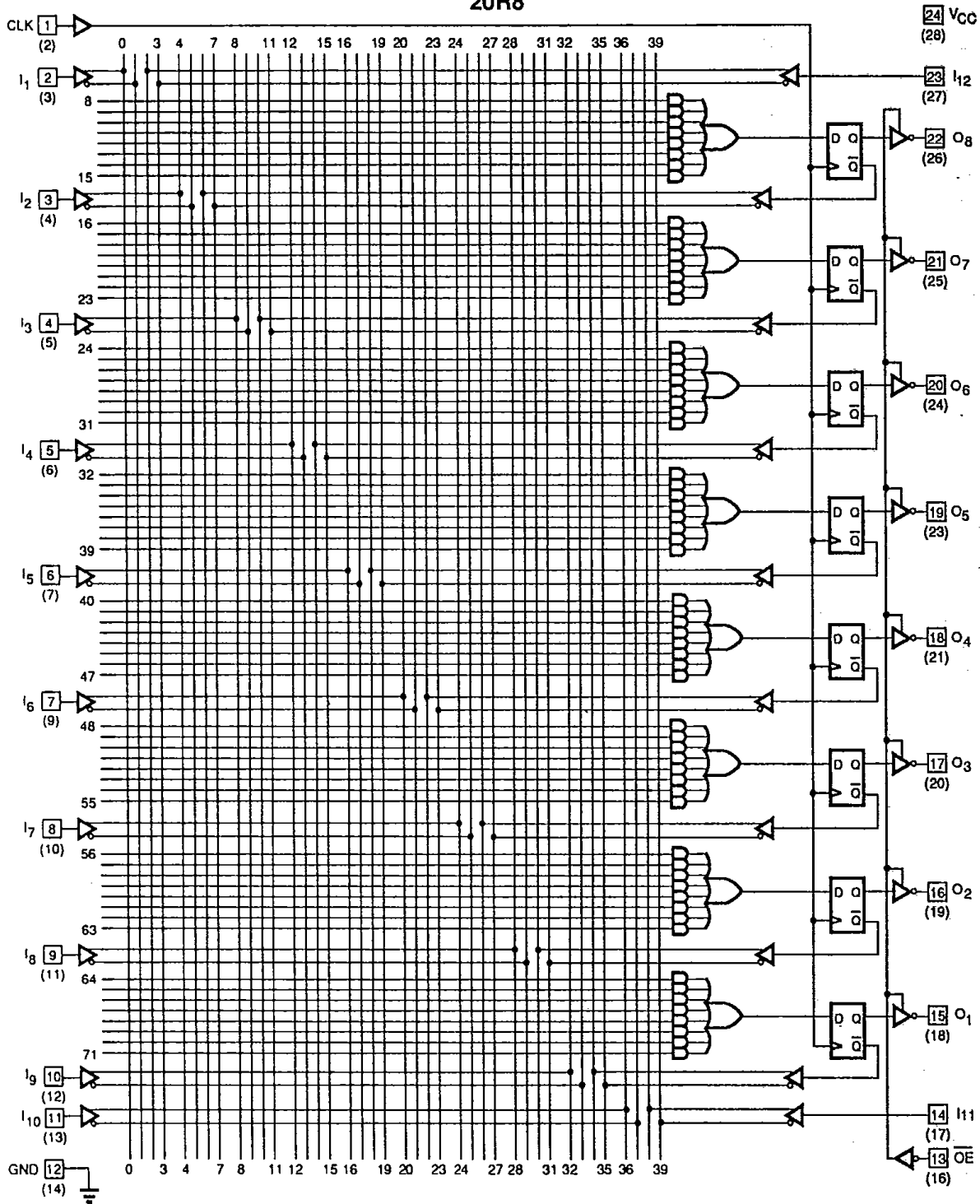
# LOGIC DIAGRAM

## DIP (JEDEC PLCC and LCC) Pinouts

See Connection Diagrams for B, A, A-2 Series PLCC/LCC Pinouts

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### 20R8



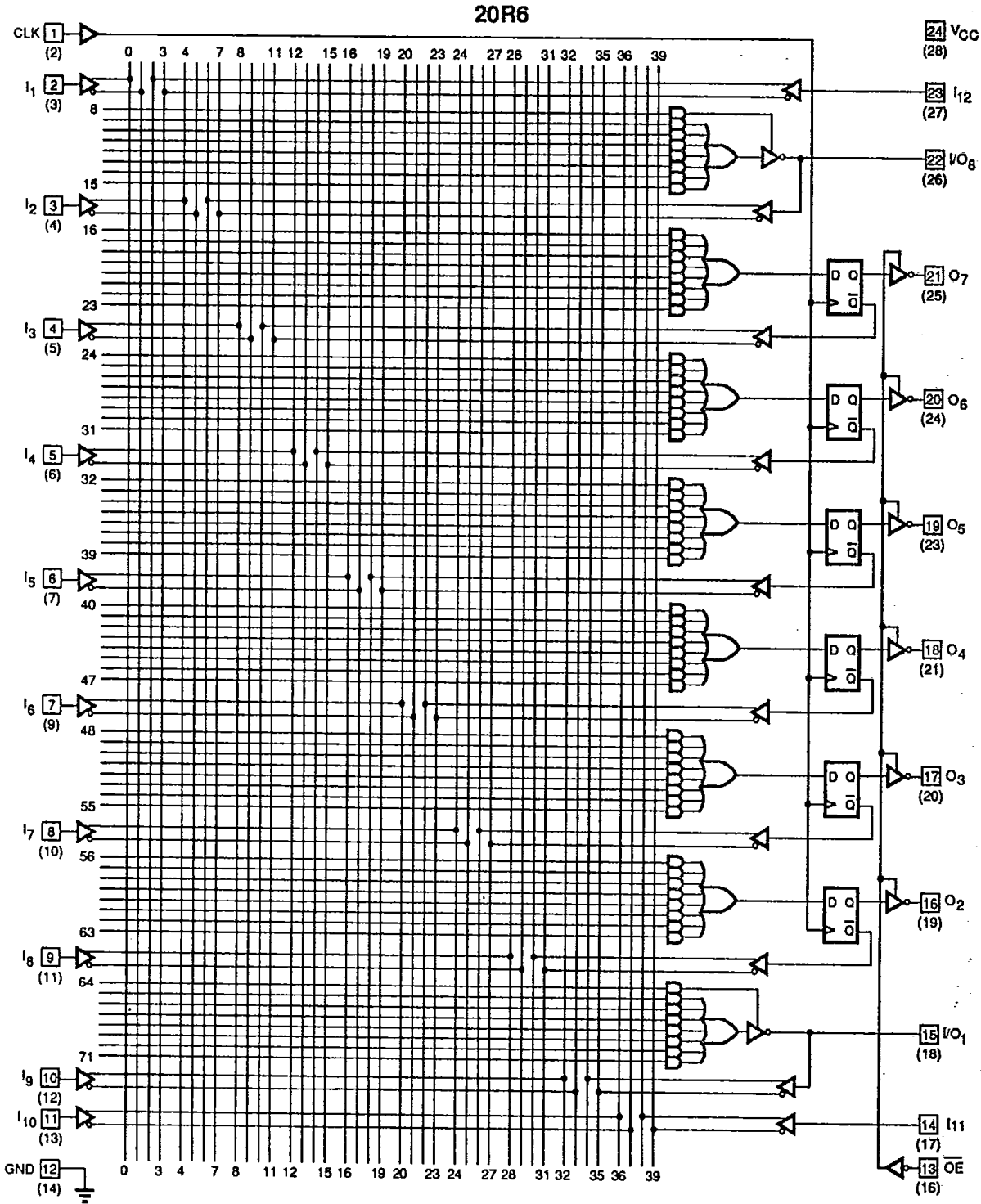
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LOGIC DIAGRAM

DIP (JEDEC PLCC and LCC) Pinouts

See Connection Diagrams for B, A, A-2 Series PLCC/LCC Pinouts

T-46-19-13



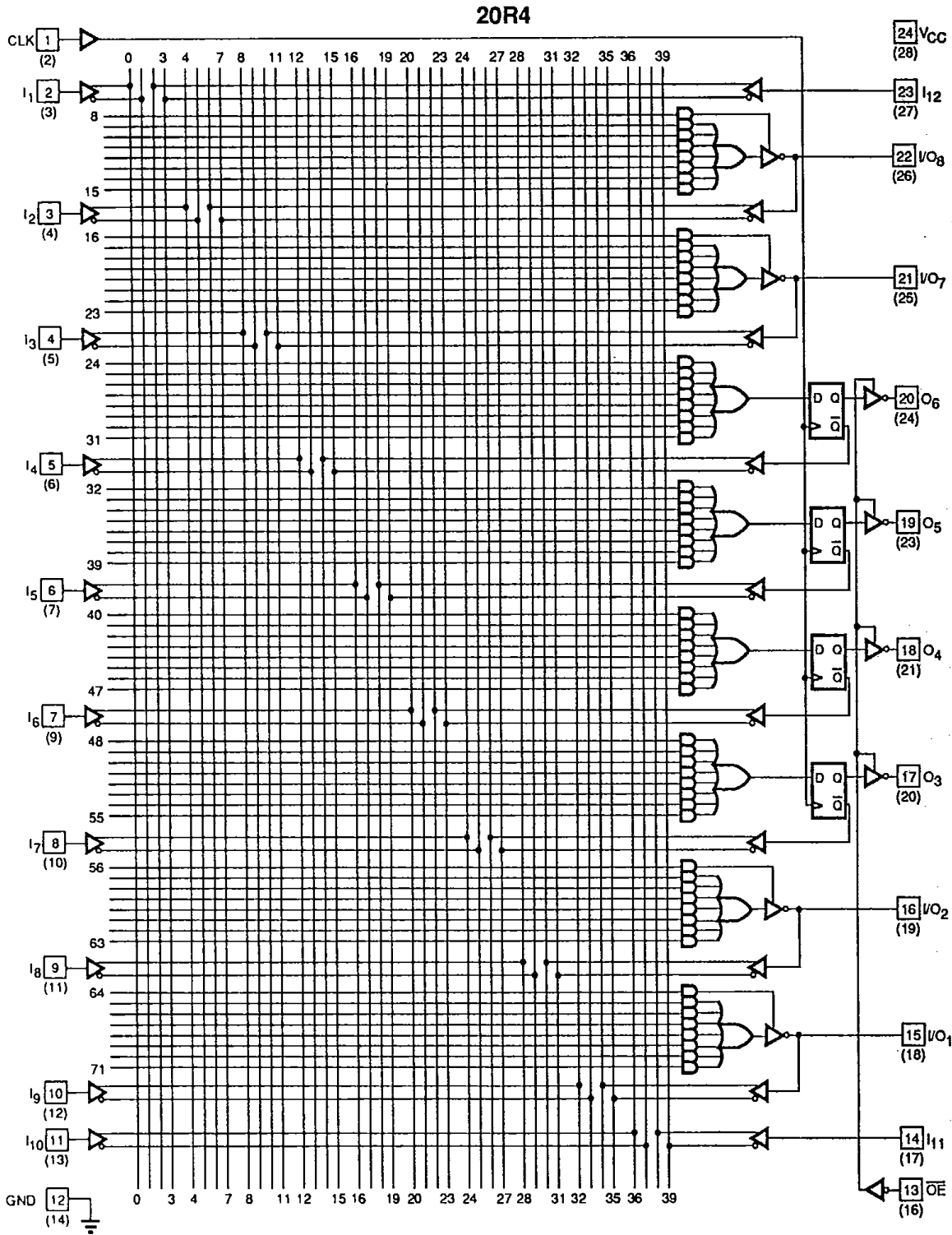
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LOGIC DIAGRAM

DIP (JEDEC PLCC and LCC) Pinouts

See Connection Diagrams for B, A, A-2 Series PLCC/LCC Pinouts

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12350-010A

**ABSOLUTE MAXIMUM RATINGS**

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-1.2 V to $V_{CC} + 0.5$ V
DC Output or I/O Pin Voltage	-0.5 V to $V_{CC} + 0.5$ V
Static Discharge Voltage	2001 V

**OPERATING RANGES****Commercial (C) Devices**

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Ambient Temperature ( $T_A$ ) Operating in Free Air	0°C to +75°C
Supply Voltage ( $V_{CC}$ ) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

**DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified**

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -3.2$ mA $V_{IN} = V_{IH}$ or $V_{IL}$ $V_{CC} = \text{Min.}$	2.4		V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 24$ mA $V_{IN} = V_{IH}$ or $V_{IL}$ $V_{CC} = \text{Min.}$		0.5	V
$V_{IH}$	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
$V_{IL}$	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
$V_I$	Input Clamp Voltage	$I_{IN} = -18$ mA, $V_{CC} = \text{Min.}$		-1.2	V
$I_{IH}$	Input HIGH Current	$V_{IN} = 2.7$ V, $V_{CC} = \text{Max.}$ (Note 2)		25	$\mu$ A
$I_{IL}$	Input LOW Current	$V_{IN} = 0.4$ V, $V_{CC} = \text{Max.}$ (Note 2)		-250	$\mu$ A
$I_I$	Maximum Input Current	$V_{IN} = 5.5$ V, $V_{CC} = \text{Max.}$		1	mA
$I_{OZH}$	Off-State Output Leakage Current HIGH	$V_{OUT} = 2.7$ V, $V_{CC} = \text{Max.}$ $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 2)		100	$\mu$ A
$I_{OL}$	Off-State Output Leakage Current LOW	$V_{OUT} = 0.4$ V, $V_{CC} = \text{Max.}$ $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 2)		-100	$\mu$ A
$I_{SC}$	Output Short-Circuit Current	$V_{OUT} = 0.5$ V, $V_{CC} = \text{Max.}$ (Note 3)	-30	-130	mA
$I_{CC}$	Supply Current	$V_{IN} = 0$ V, Outputs Open ( $I_{OUT} = 0$ mA) $V_{CC} = \text{Max.}$		210	mA

**Notes:**

- These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
- I/O pin leakage is the worst case of  $I_{IL}$  and  $I_{OL}$  (or  $I_{IH}$  and  $I_{OZH}$ ).
- Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second.  $V_{OUT} = 0.5$  V has been chosen to avoid test problems caused by tester ground degradation.



## CAPACITANCE (Note 1)

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Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 2.0 V	V <sub>CC</sub> = 5.0 V T <sub>A</sub> = +25°C f = 1 MHz	7	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 2.0 V		8	

**Note:**

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

## SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description		Min. (Note 3)	Max.	Unit		
t <sub>PD</sub>	Input or Feedback to Combinatorial Output	1 Output Switching	20L8, 20R6 20R4	3	7.5	ns	
				3	7		
t <sub>S</sub>	Setup Time from Input or Feedback to Clock		20R8, 20R6, 20R4	7		ns	
t <sub>H</sub>	Hold Time			0		ns	
t <sub>CO</sub>	Clock to Output			3	6.5	ns	
t <sub>CF</sub>	Clock to Feedback (Note 4)				3	ns	
t <sub>SKEW</sub>	Skew Between Registered Outputs (Note 5)				1	ns	
t <sub>WL</sub>	Clock Width	LOW		5		ns	
t <sub>WH</sub>		HIGH		5		ns	
f <sub>MAX</sub>	Maximum Frequency (Note 6)	External Feedback		1/(t <sub>S</sub> + t <sub>CO</sub> )	74		MHz
		Internal Feedback		1/(t <sub>S</sub> + t <sub>CF</sub> )	100		MHz
		No Feedback		1/(t <sub>WH</sub> + t <sub>WL</sub> )	100		MHz
t <sub>PZX</sub>	$\overline{OE}$ to Output Enable		3	8	ns		
t <sub>PXZ</sub>	$\overline{OE}$ to Output Disable		3	8	ns		
t <sub>EA</sub>	Input to Output Enable Using Product Term Control		20L8, 20R6	3	10	ns	
t <sub>ER</sub>	Input to Output Disable Using Product Term Control		20R4	3	10	ns	

**Notes:**

2. See Switching Test Circuit for test conditions.
3. Output delay minimums are measured under best-case conditions.
4. Calculated from measured f<sub>MAX</sub> internal.
5. Skew is measured with all outputs switching in the same direction.
6. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-1.2 V to $V_{CC} + 0.5$ V
DC Output or I/O Pin Voltage	-0.5 V to $V_{CC} + 0.5$ V
Static Discharge Voltage	2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

## OPERATING RANGES

Military (M) Devices (Note 1)	T-46-19-13
Operating Case ( $T_C$ ) Temperature	-55°C to +125°C
Supply Voltage ( $V_{CC}$ ) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

### Note:

- Military products are tested at  $T_C = +25^\circ\text{C}$ ,  $+125^\circ\text{C}$ , and  $-55^\circ\text{C}$  per MIL-STD-883.

## DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -2$ mA, $V_{IN} = V_{IH}$ or $V_{IL}$ , $V_{CC} = \text{Min.}$	2.4		V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 12$ mA, $V_{IN} = V_{IH}$ or $V_{IL}$ , $V_{CC} = \text{Min.}$		0.5	V
$V_{IH}$	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
$V_{IL}$	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
$V_I$	Input Clamp Voltage	$I_{IN} = -18$ mA, $V_{CC} = \text{Min.}$		-1.2	V
$I_{IH}$	Input HIGH Current	$V_{IN} = 2.4$ V, $V_{CC} = \text{Max.}$ (Note 4)		25	$\mu\text{A}$
$I_{IL}$	Input LOW Current	$V_{IN} = 0.4$ V, $V_{CC} = \text{Max.}$ (Note 4)		-250	$\mu\text{A}$
$I_I$	Maximum Input Current	$V_{IN} = 5.5$ V, $V_{CC} = \text{Max.}$		1	mA
$I_{OZH}$	Off-State Output Leakage Current HIGH	$V_{OUT} = 2.4$ V, $V_{CC} = \text{Max.}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 4)		100	$\mu\text{A}$
$I_{OZL}$	Off-State Output Leakage Current LOW	$V_{OUT} = 0.4$ V, $V_{CC} = \text{Max.}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 4)		-100	$\mu\text{A}$
$I_{SC}$	Output Short-Circuit Current	$V_{OUT} = 0.5$ V, $V_{CC} = \text{Max.}$ (Note 5)	-30	-130	mA
$I_{CC}$	Supply Current	$V_{IN} = 0$ V, Outputs Open ( $I_{OUT} = 0$ mA), $V_{CC} = \text{Max.}$		210	mA

### Notes:

- For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
- $V_{IL}$  and  $V_{IH}$  are input conditions of output tests and are not themselves directly tested.  $V_{IL}$  and  $V_{IH}$  are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
- I/O pin leakage is the worst case of  $I_{IL}$  and  $I_{OZL}$  (or  $I_{IH}$  and  $I_{OZH}$ ).
- Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second.  $V_{OUT} = 0.5$  V has been chosen to avoid test problems caused by tester ground degradation.

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 2.0 V	V <sub>CC</sub> = 5.0 V T <sub>A</sub> = +25°C	9	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 2.0 V	f = 1 MHz	10	

**Note:**

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

**SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)**

Parameter Symbol	Parameter Description			Min. (Note 3)	Max.	Unit
t <sub>PD</sub>	Input or Feedback to Combinatorial Output		20L8, 20R6 20R4	3	12.5	ns
		1 Output Switching		3	12	
t <sub>s</sub>	Setup Time from Input or Feedback to Clock			12		ns
t <sub>H</sub>	Hold Time			0		ns
t <sub>CO</sub>	Clock to Output			3	11	ns
t <sub>CF</sub>	Clock to Feedback (Note 4)				6.5	ns
t <sub>SKEW</sub>	Skew Between Registered Outputs (Note 5)				1	ns
t <sub>WL</sub>	Clock Width	LOW	20R8, 20R6 20R4	10		ns
		HIGH		8		ns
f <sub>MAX</sub>	Maximum Frequency (Note 6)	External Feedback		43.4		MHz
		Internal Feedback		54		MHz
		No Feedback		55.5		MHz
t <sub>PZX</sub>	OE to Output Enable (Note 7)			3	20	ns
t <sub>PXZ</sub>	OE to Output Disable (Note 7)			3	20	ns
t <sub>EA</sub>	Input to Output Enable Using Product Term Control (Note 7)		20L8, 20R6 20R4	3	20	ns
t <sub>ER</sub>	Input to Output Disable Using Product Term Control (Note 7)			3	20	ns

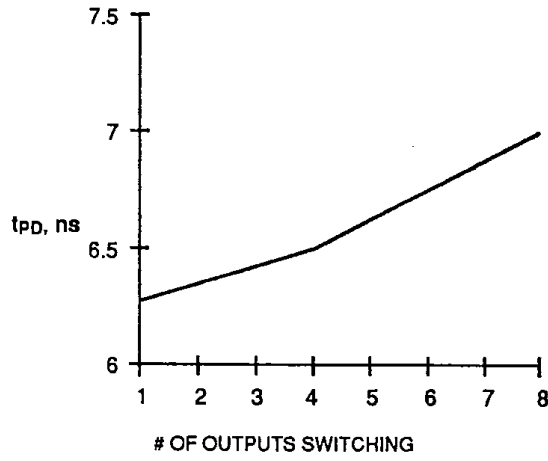
**Notes:**

2. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. Minimum value for t<sub>PD</sub>, t<sub>CO</sub>, t<sub>PZX</sub>, t<sub>PXZ</sub>, t<sub>EA</sub>, and t<sub>ER</sub> parameters should be used for simulation purposes only and are not tested.
4. Calculated from measured f<sub>MAX</sub> internal.
5. Skew is measured with all outputs switching in the same direction.
6. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
7. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

MEASURED SWITCHING CHARACTERISTICS

V<sub>CC</sub> = 5.25 V, T<sub>A</sub> = 75°C (Note 1)

T-46-19-13



tpD vs. Number of Outputs Switching

10294-005A

Note:

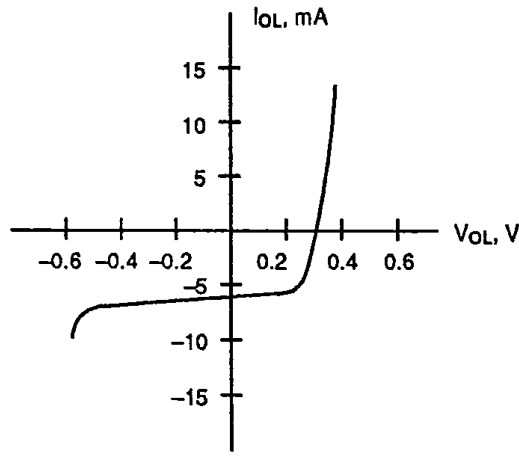
1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where tpD may be affected.

ADV MICRO PLAY/PLAY ARRAYS      EOE      SECTION

# CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

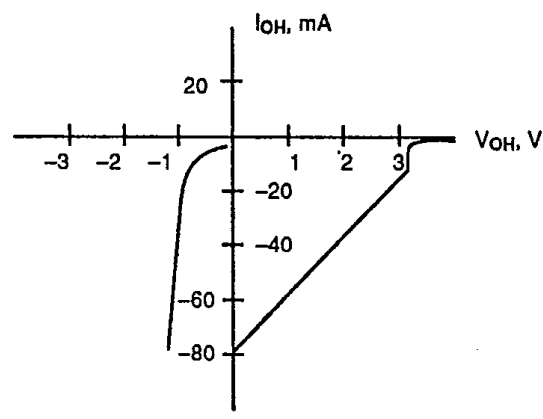
$V_{CC} = 5.0 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

T-46-19-13



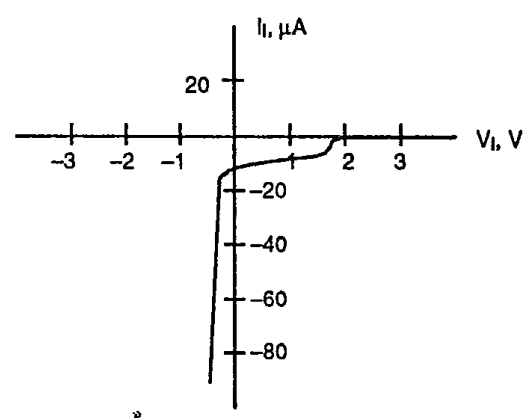
Output, LOW

10240-003A



Output, HIGH

10240-004A



Input

10240-005A



**ABSOLUTE MAXIMUM RATINGS**

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-0.5 V to $V_{CC} + 0.5$ V
DC Output or I/O Pin Voltage	-0.5 V to $V_{CC}$ Max.
DC Input Current	-30 mA to +5 mA

**OPERATING RANGES****T-46-19-13****Commercial (C) Devices**

Ambient Temperature ( $T_A$ )	0°C to +75°C
Operating in Free Air	0°C to +75°C
Supply Voltage ( $V_{CC}$ ) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

**DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified**

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -3.2$ mA $V_{IN} = V_{IH}$ or $V_{IL}$ $V_{CC} = \text{Min.}$	2.4		V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 24$ mA $V_{IN} = V_{IH}$ or $V_{IL}$ $V_{CC} = \text{Min.}$		0.5	V
$V_{IH}$	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all inputs (Note 1)	2.0		V
$V_{IL}$	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all inputs (Note 1)		0.8	V
$V_I$	Input Clamp Voltage	$I_{IN} = -18$ mA, $V_{CC} = \text{Min.}$		-1.5	V
$I_{IH}$	Input HIGH Current	$V_{IN} = 2.7$ V, $V_{CC} = \text{Max.}$ (Note 2)		25	$\mu$ A
$I_{IL}$	Input LOW Current	$V_{IN} = 0.4$ V, $V_{CC} = \text{Max.}$ (Note 2)		-250	$\mu$ A
$I_I$	Maximum Input Current	$V_{IN} = 5.5$ V, $V_{CC} = \text{Max.}$		100	$\mu$ A
$I_{OZH}$	Off-State Output Leakage Current HIGH	$V_{OUT} = 2.7$ V, $V_{CC} = \text{Max.}$ $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 2)		100	$\mu$ A
$I_{OLZ}$	Off-State Output Leakage Current LOW	$V_{OUT} = 0.4$ V, $V_{CC} = \text{Max.}$ $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 2)		-100	$\mu$ A
$I_{SC}$	Output Short-Circuit Current	$V_{OUT} = 0.5$ V, $V_{CC} = \text{Max.}$ (Note 3)	-30	-130	mA
$I_{CC}$	Supply Current	$V_{IN} = 0$ V, Outputs Open ( $I_{OUT} = 0$ mA) $V_{CC} = \text{Max.}$		210	mA

**Notes:**

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of  $I_{IL}$  and  $I_{OLZ}$  (or  $I_{IH}$  and  $I_{OZH}$ ).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second.  $V_{OUT} = 0.5$  V has been chosen to avoid test problems caused by tester ground degradation.

**CAPACITANCE (Note 1)**

T-46-19-13

Parameter Symbol	Parameter Description	Test Conditions			Typ.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 2.0 V	V <sub>CC</sub> = 5.0 V T <sub>A</sub> = 25°C	CLK, $\overline{OE}$	12	pF
				Other Inputs	7	
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 2.0 V	f = 1 MHz	Outputs	8	

**Note:**

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

**SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)**

Parameter Symbol	Parameter Description		Min. (Note 3)	Max.	Unit		
t <sub>PD</sub>	Input or Feedback to Combinatorial Output		20L8, 20R6 20R4	3	10	ns	
t <sub>s</sub>	Setup Time from Input or Feedback to Clock		20R8, 20R6 20R4	10		ns	
t <sub>H</sub>	Hold Time			0		ns	
t <sub>CO</sub>	Clock to Output			2	8	ns	
t <sub>CF</sub>	Clock to Feedback (Note 4)				7	ns	
t <sub>WL</sub>	Clock Width	LOW		7		ns	
		HIGH		7		ns	
f <sub>MAX</sub>	Maximum Frequency (Note 5)	External Feedback		1/(t <sub>s</sub> + t <sub>CO</sub> )	55.5		MHz
		Internal Feedback		1/(t <sub>s</sub> + t <sub>CF</sub> )	58.8		MHz
		No Feedback		1/(t <sub>WH</sub> + t <sub>WL</sub> )	71.4		MHz
t <sub>PZX</sub>	$\overline{OE}$ to Output Enable				1	10	ns
t <sub>PXZ</sub>	$\overline{OE}$ to Output Disable			1	10	ns	
t <sub>EA</sub>	Input to Output Enable Using Product Term Control		20L8, 20R6	3	10	ns	
t <sub>ER</sub>	Input to Output Disable Using Product Term Control		20R4	3	10	ns	



**Notes:**

2. See Switching Test Circuit for test conditions.
3. Output delay minimums are measured under best-case conditions.
4. Calculated from measured f<sub>MAX</sub> internal.
5. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.

**ABSOLUTE MAXIMUM RATINGS**

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-0.5 V to +5.5 V
DC Output or I/O Pin Voltage	-0.5 V to $V_{CC}$ Max.
DC Input Current	-30 mA to +5 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

**OPERATING RANGES**

Military (M) Devices (Note 1)	<b>T-46-19-13</b>
Ambient Temperature ( $T_A$ )	-55°C Min.
Operating in Free Air	
Operating Case ( $T_C$ ) Temperature	+125°C Max.
Supply Voltage ( $V_{CC}$ ) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

**Note:**

1. Military products are tested at  $T_C = +25^\circ\text{C}$ ,  $+125^\circ\text{C}$ , and  $-55^\circ\text{C}$  per MIL-STD-883.

**DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)**

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -2$ mA $V_{IN} = V_{IH}$ or $V_{IL}$ $V_{CC} = \text{Min.}$	2.4		V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 12$ mA $V_{IN} = V_{IH}$ or $V_{IL}$ $V_{CC} = \text{Min.}$		0.5	V
$V_{IH}$	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
$V_{IL}$	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
$V_I$	Input Clamp Voltage	$I_{IN} = -18$ mA, $V_{CC} = \text{Min.}$		-1.5	V
$I_{IH}$	Input HIGH Current	$V_{IN} = 2.4$ V, $V_{CC} = \text{Max.}$ (Note 4)		25	$\mu\text{A}$
$I_{IL}$	Input LOW Current	$V_{IN} = 0.4$ V, $V_{CC} = \text{Max.}$ (Note 4)		-250	$\mu\text{A}$
$I_I$	Maximum Input Current	$V_{IN} = 5.5$ V, $V_{CC} = \text{Max.}$		100	$\mu\text{A}$
$I_{OZH}$	Off-State Output Leakage Current HIGH	$V_{OUT} = 2.7$ V, $V_{CC} = \text{Max.}$ $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 4)		100	$\mu\text{A}$
$I_{OZL}$	Off-State Output Leakage Current LOW	$V_{OUT} = 0.4$ V, $V_{CC} = \text{Max.}$ $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 4)		-100	$\mu\text{A}$
$I_{SC}$	Output Short-Circuit Current	$V_{OUT} = 0.5$ V, $V_{CC} = \text{Max.}$ (Note 5)	-30	-130	mA
$I_{CC}$	Supply Current	$V_{IN} = 0$ V, Outputs Open ( $I_{OUT} = 0$ mA) $V_{CC} = \text{Max.}$		210	mA

**Notes:**

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3.  $V_{IL}$  and  $V_{IH}$  are input conditions of output tests and are not themselves directly tested.  $V_{IL}$  and  $V_{IH}$  are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of  $I_{IL}$  and  $I_{OZL}$  (or  $I_{IH}$  and  $I_{OZH}$ ).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second.  $V_{OUT} = 0.5$  V has been chosen to avoid test problems caused by tester ground degradation.



## CAPACITANCE (Note 1)

T-46-19-13

Parameter Symbol	Parameter Description	Test Conditions			Typ.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 2.0 V	V <sub>CC</sub> = 5.0 V T <sub>A</sub> = 25°C	CLK, $\overline{OE}$	12	pF
				Other Inputs	7	
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 2.0 V	f = 1 MHz	Outputs	8	

## Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

## SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description		Min. (Note 3)	Max.	Unit		
t <sub>PD</sub>	Input or Feedback to Combinatorial Output		20L8, 20R6 20R4	3	15	ns	
t <sub>s</sub>	Setup Time from Input or Feedback to Clock		20R8, 20R6 20R4	15		ns	
t <sub>H</sub>	Hold Time			0		ns	
t <sub>CO</sub>	Clock to Output			2	13	ns	
t <sub>CF</sub>	Clock to Feedback (Note 4)				12	ns	
t <sub>WL</sub>	Clock Width	LOW		10		ns	
		HIGH		10		ns	
f <sub>MAX</sub>	Maximum Frequency (Note 5)	External Feedback		1/(t <sub>s</sub> + t <sub>CO</sub> )	35.7		MHz
		Internal Feedback		1/(t <sub>s</sub> + t <sub>CF</sub> )	37		MHz
		No Feedback		1/(t <sub>WH</sub> + t <sub>WL</sub> )	50		MHz
t <sub>PZX</sub>	$\overline{OE}$ to Output Enable (Note 6)				1	15	ns
t <sub>PXZ</sub>	$\overline{OE}$ to Output Disable (Note 6)			1	15	ns	
t <sub>EA</sub>	Input to Output Enable Using Product Term Control (Note 6)		20L8, 20R6 20R4	3	15	ns	
t <sub>ER</sub>	Input to Output Disable Using Product Term Control (Note 6)			3	15	ns	

## Notes:

2. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. Minimum value for t<sub>PD</sub>, t<sub>CO</sub>, t<sub>PZX</sub>, t<sub>PXZ</sub>, t<sub>EA</sub>, and t<sub>ER</sub> parameters should be used for simulation purposes only and are not tested.
4. Calculated from measured f<sub>MAX</sub> internal.
5. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
6. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

**ABSOLUTE MAXIMUM RATINGS**

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-1.5 V to $V_{CC} + 0.5$ V
DC Output or I/O Pin Voltage	-0.5 V to $V_{CC} + 0.5$ V

**OPERATING RANGES**

Commercial (C) Devices	<b>T-46-19-13</b>
Ambient Temperature ( $T_A$ ) Operating in Free Air	0°C to +75°C
Supply Voltage ( $V_{CC}$ ) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

**DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified**

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -3.2$ mA, $V_{IN} = V_{IH}$ or $V_{IL}$ , $V_{CC} = \text{Min.}$	2.4		V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 24$ mA, $V_{IN} = V_{IH}$ or $V_{IL}$ , $V_{CC} = \text{Min.}$		0.5	V
$V_{IH}$	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
$V_{IL}$	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
$V_I$	Input Clamp Voltage	$I_{IN} = -18$ mA, $V_{CC} = \text{Min.}$		-1.5	V
$I_{IH}$	Input HIGH Current	$V_{IN} = 2.7$ V, $V_{CC} = \text{Max.}$ (Note 2)		25	$\mu$ A
$I_{IL}$	Input LOW Current	$V_{IN} = 0.4$ V, $V_{CC} = \text{Max.}$ (Note 2)		-250	$\mu$ A
$I_I$	Maximum Input Current	$V_{IN} = 5.5$ V, $V_{CC} = \text{Max.}$		100	$\mu$ A
$I_{OZH}$	Off-State Output Leakage Current HIGH	$V_{OUT} = 2.7$ V, $V_{CC} = \text{Max.}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 2)		100	$\mu$ A
$I_{OZL}$	Off-State Output Leakage Current LOW	$V_{OUT} = 0.4$ V, $V_{CC} = \text{Max.}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 2)		-100	$\mu$ A
$I_{SC}$	Output Short-Circuit Current	$V_{OUT} = 0.5$ V, $V_{CC} = \text{Max.}$ (Note 3)	-30	-130	mA
$I_{CC}$	Supply Current	$V_{IN} = 0$ V, Outputs Open ( $I_{OUT} = 0$ mA), $V_{CC} = \text{Max.}$		210	mA

**Notes:**

- These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
- I/O pin leakage is the worst case of  $I_{IL}$  and  $I_{OZL}$  (or  $I_{IH}$  and  $I_{OZH}$ ).
- Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second.  $V_{OUT} = 0.5$  V has been chosen to avoid test problems caused by tester ground degradation.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description		T-46-19-13	Min.	Max.	Unit	
t <sub>PD</sub>	Input or Feedback to Combinatorial Output		20L8, 20R6 20R4		15	ns	
t <sub>s</sub>	Setup Time from Input or Feedback to Clock		20R8 20R6 20R4	15		ns	
t <sub>H</sub>	Hold Time			0		ns	
t <sub>CO</sub>	Clock to Output or Feedback				12	ns	
t <sub>WL</sub>	Clock Width	LOW			10	ns	
t <sub>WH</sub>		HIGH			12	ns	
f <sub>MAX</sub>	Maximum Frequency (Note 2)	External Feedback			37	MHz	
		No Feedback			45	MHz	
t <sub>PZX</sub>	$\overline{OE}$ to Output Enable					15	ns
t <sub>PXZ</sub>	$\overline{OE}$ to Output Disable					12	ns
t <sub>EA</sub>	Input to Output Enable Using Product Term Control			20L8, 20R6		18	ns
t <sub>ER</sub>	Input to Output Disable Using Product Term Control		20R4		15	ns	

Notes:

1. See Switching Test Circuit for test conditions.
2. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

FOR CMOS CELL  
PALCE20V8



## ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-1.5 V to +5.5 V
DC Output or I/O Pin Voltage	5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

## OPERATING RANGES

Military (M) Devices (Note 1)	T-46-19-13
Ambient Temperature (T <sub>A</sub> )	-55°C Min.
Operating in Free Air	-55°C Min.
Operating Case (T <sub>C</sub> ) Temperature	+125°C Max.
Supply Voltage (V <sub>CC</sub> ) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

### Note:

1. Military products are tested at T<sub>C</sub> = +25°C, +125°C, and -55°C per MIL-STD-883.

## DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -2 mA, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>CC</sub> = Min.	2.4		V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 12 mA, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>CC</sub> = Min.		0.5	V
V <sub>IH</sub>	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V <sub>IL</sub>	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V <sub>I</sub>	Input Clamp Voltage	I <sub>IN</sub> = -18 mA, V <sub>CC</sub> = Min.		-1.5	V
I <sub>IH</sub>	Input HIGH Current	V <sub>IN</sub> = 2.4 V, V <sub>CC</sub> = Max. (Note 4)		25	μA
I <sub>IL</sub>	Input LOW Current	V <sub>IN</sub> = 0.4 V, V <sub>CC</sub> = Max. (Note 4)		-250	μA
I <sub>I</sub>	Maximum Input Current	V <sub>IN</sub> = 5.5 V, V <sub>CC</sub> = Max.		1	mA
I <sub>OZH</sub>	Off-State Output Leakage Current HIGH	V <sub>OUT</sub> = 2.4 V, V <sub>CC</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> (Note 4)		100	μA
I <sub>OZL</sub>	Off-State Output Leakage Current LOW	V <sub>OUT</sub> = 0.4 V, V <sub>CC</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> (Note 4)		-100	μA
I <sub>SC</sub>	Output Short-Circuit Current	V <sub>OUT</sub> = 0.5 V, V <sub>CC</sub> = Max. (Note 5)	-30	-130	mA
I <sub>CC</sub>	Supply Current	V <sub>IN</sub> = 0 V, Outputs Open (I <sub>OUT</sub> = 0 mA), V <sub>CC</sub> = Max.		210	mA

### Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V<sub>IL</sub> and V<sub>IH</sub> are input conditions of output tests and are not themselves directly tested. V<sub>IL</sub> and V<sub>IH</sub> are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I<sub>IL</sub> and I<sub>OZL</sub> (or I<sub>IH</sub> and I<sub>OZH</sub>).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V<sub>OUT</sub> = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 1)

T-46-19-13

Parameter Symbol	Parameter Description			Min.	Max.	Unit
t <sub>PD</sub>	Input or Feedback to Combinatorial Output				20	ns
t <sub>s</sub>	Setup Time from Input or Feedback to Clock			20		ns
t <sub>H</sub>	Hold Time			0		ns
t <sub>CO</sub>	Clock to Output or Feedback				15	ns
t <sub>WL</sub>	Clock Width	LOW		12		ns
t <sub>WH</sub>		HIGH		12		ns
f <sub>MAX</sub>	Maximum Frequency (Note 2)	External Feedback	1/(t <sub>s</sub> + t <sub>CO</sub> )	28.5		MHz
		No Feedback	1/(t <sub>WH</sub> + t <sub>WL</sub> )	41.6		MHz
t <sub>PZX</sub>	$\overline{OE}$ to Output Enable (Note 3)				20	ns
t <sub>PXZ</sub>	$\overline{OE}$ to Output Disable (Note 3)				20	ns
t <sub>EA</sub>	Input to Output Enable Using Product Term Control (Note 3)				25	ns
t <sub>ER</sub>	Input to Output Disable Using Product Term Control (Note 3)				20	ns

Notes:

1. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
2. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

FULL WADG SET  
 PALCE2018

2

**ABSOLUTE MAXIMUM RATINGS**

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-1.5 V to $V_{CC} + 0.5$ V
DC Output or I/O Pin Voltage	-0.5 V to $V_{CC} + 0.5$ V

**OPERATING RANGES****T-46-19-13****Commercial (C) Devices**

Ambient Temperature ( $T_A$ )	Operating in Free Air	0°C to +75°C
Supply Voltage ( $V_{CC}$ )	with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

**DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified**

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -3.2$ mA, $V_{IN} = V_{IH}$ or $V_{IL}$ , $V_{CC} = \text{Min.}$	2.4		V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 24$ mA, $V_{IN} = V_{IH}$ or $V_{IL}$ , $V_{CC} = \text{Min.}$		0.5	V
$V_{IH}$	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
$V_{IL}$	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
$V_I$	Input Clamp Voltage	$I_{IN} = -18$ mA, $V_{CC} = \text{Min.}$		-1.5	V
$I_{IH}$	Input HIGH Current	$V_{IN} = 2.7$ V, $V_{CC} = \text{Max.}$ (Note 2)		25	$\mu$ A
$I_{IL}$	Input LOW Current	$V_{IN} = 0.4$ V, $V_{CC} = \text{Max.}$ (Note 2)		-250	$\mu$ A
$I_I$	Maximum Input Current	$V_{IN} = 5.5$ V, $V_{CC} = \text{Max.}$		100	$\mu$ A
$I_{OZH}$	Off-State Output Leakage Current HIGH	$V_{OUT} = 2.7$ V, $V_{CC} = \text{Max.}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 2)		100	$\mu$ A
$I_{OZL}$	Off-State Output Leakage Current LOW	$V_{OUT} = 0.4$ V, $V_{CC} = \text{Max.}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 2)		-100	$\mu$ A
$I_{SC}$	Output Short-Circuit Current	$V_{OUT} = 0.5$ V, $V_{CC} = \text{Max.}$ (Note 3)	-30	-130	mA
$I_{CC}$	Supply Current	$V_{IN} = 0$ V, Outputs Open ( $I_{OUT} = 0$ mA), $V_{CC} = \text{Max.}$		105	mA

**Notes:**

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of  $I_{IL}$  and  $I_{OZL}$  (or  $I_{IH}$  and  $I_{OZH}$ ).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second.  $V_{OUT} = 0.5$  V has been chosen to avoid test problems caused by tester ground degradation.

**SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)**

Parameter Symbol	Parameter Description			T-46-19-13	Min.	Max.	Unit
t <sub>PD</sub>	Input or Feedback to Combinatorial Output			20L8, 20R6 20R4		25	ns
t <sub>s</sub>	Setup Time from Input or Feedback to Clock			20R8, 20R6 20R4	25		ns
t <sub>H</sub>	Hold Time				0		ns
t <sub>CO</sub>	Clock to Output					15	ns
t <sub>CF</sub>	Clock to Feedback (Note 2)					10	ns
t <sub>WL</sub>	Clock Width	LOW			15		ns
t <sub>WH</sub>		HIGH			15		ns
f <sub>MAX</sub>	Maximum Frequency (Note 3)	External Feedback	1/(t <sub>s</sub> + t <sub>CO</sub> )		25		MHz
		Internal Feedback	1/(t <sub>s</sub> + t <sub>CF</sub> )		28.5		MHz
		No Feedback	1/(t <sub>WH</sub> + t <sub>WL</sub> )		33.3		MHz
t <sub>PZX</sub>	OE to Output Enable					20	ns
t <sub>PXZ</sub>	OE to Output Disable				20	ns	
t <sub>EA</sub>	Input to Output Enable Using Product Term Control			20L8, 20R6		25	ns
t <sub>ER</sub>	Input to Output Disable Using Product Term Control			20R4		25	ns

**Notes:**

1. See Switching Test Circuit for test conditions.
2. Calculated from measured f<sub>MAX</sub> internal.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

FULL TIME RELEASE  
 PALCE20WB



### ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-1.5 V to $V_{CC} + 0.5$ V
DC Output or I/O Pin Voltage	-0.5 V to $V_{CC} + 0.5$ V

### OPERATING RANGES

#### Commercial (C) Devices

Ambient Temperature ( $T_A$ )	0°C to +75°C
Operating in Free Air	0°C to +75°C
Supply Voltage ( $V_{CC}$ ) with Respect to Ground	+4.75 V to +5.25 V

T-46-19-13

Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

### DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -3.2$ mA, $V_{IN} = V_{IH}$ or $V_{IL}$ , $V_{CC} = \text{Min.}$	2.4		V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 24$ mA, $V_{IN} = V_{IH}$ or $V_{IL}$ , $V_{CC} = \text{Min.}$		0.5	V
$V_{IH}$	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
$V_{IL}$	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
$V_I$	Input Clamp Voltage	$I_{IN} = -18$ mA, $V_{CC} = \text{Min.}$		-1.5	V
$I_{IH}$	Input HIGH Current	$V_{IN} = 2.7$ V, $V_{CC} = \text{Max.}$ (Note 2)		25	$\mu$ A
$I_{IL}$	Input LOW Current	$V_{IN} = 0.4$ V, $V_{CC} = \text{Max.}$ (Note 2)		-250	$\mu$ A
$I_I$	Maximum Input Current	$V_{IN} = 5.5$ V, $V_{CC} = \text{Max.}$		100	$\mu$ A
$I_{OZH}$	Off-State Output Leakage Current HIGH	$V_{OUT} = 2.7$ V, $V_{CC} = \text{Max.}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 2)		100	$\mu$ A
$I_{OLZ}$	Off-State Output Leakage Current LOW	$V_{OUT} = 0.4$ V, $V_{CC} = \text{Max.}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 2)		-100	$\mu$ A
$I_{SC}$	Output Short-Circuit Current	$V_{OUT} = 0.5$ V, $V_{CC} = \text{Max.}$ (Note 3)	-30	-130	mA
$I_{CC}$	Supply Current	$V_{IN} = 0$ V, Outputs Open ( $I_{OUT} = 0$ mA), $V_{CC} = \text{Max.}$		210	mA

#### Notes:

- These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
- I/O pin leakage is the worst case of  $I_{IL}$  and  $I_{OLZ}$  (or  $I_{IH}$  and  $I_{OZH}$ ).
- Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second.  $V_{OUT} = 0.5$  V has been chosen to avoid test problems caused by tester ground degradation.



## SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description		T-46-19-13		Min.	Max.	Unit	
t <sub>PD</sub>	Input or Feedback to Combinatorial Output		20L8, 20R6 20R4			25	ns	
t <sub>s</sub>	Setup Time from Input or Feedback to Clock		20R8, 20R6 20R4		25		ns	
t <sub>H</sub>	Hold Time				0		ns	
t <sub>CO</sub>	Clock to Output					15	ns	
t <sub>CF</sub>	Clock to Feedback (Note 2)					10	ns	
t <sub>WL</sub>	Clock Width	LOW				15	ns	
t <sub>WH</sub>		HIGH				15	ns	
f <sub>MAX</sub>	Maximum Frequency (Note 3)	External Feedback			1/(t <sub>s</sub> + t <sub>CO</sub> )	25		MHz
		Internal Feedback			1/(t <sub>s</sub> + t <sub>CF</sub> )	28.5		MHz
		No Feedback			1/(t <sub>WH</sub> + t <sub>WL</sub> )	33		MHz
t <sub>PZX</sub>	$\overline{OE}$ to Output Enable							20
t <sub>PXZ</sub>	$\overline{OE}$ to Output Disable					20	ns	
t <sub>EA</sub>	Input to Output Enable Using Product Term Control		20L8, 20R6			25	ns	
t <sub>ER</sub>	Input to Output Disable Using Product Term Control		20R4			25	ns	

## Notes:

1. See Switching Test Circuit for test conditions.
2. Calculated from measured f<sub>MAX</sub> internal.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

2

**ABSOLUTE MAXIMUM RATINGS**

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-1.5 V to +5.5 V
DC Output or I/O Pin Voltage	5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

**OPERATING RANGES****Military (M) Devices (Note 1)**

Ambient Temperature (T <sub>A</sub> )	-55°C Min.
Operating in Free Air	-55°C Min.
Operating Case (T <sub>C</sub> ) Temperature	+125°C Max.
Supply Voltage (V <sub>CC</sub> ) with Respect to Ground	+4.50 V to +5.50 V

T-46-19-13

Operating ranges define those limits between which the functionality of the device is guaranteed.

**Note:**

1. Military products are tested at T<sub>C</sub> = +25°C, +125°C, and -55°C per MIL-STD-883.

**DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)**

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -2 mA, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>CC</sub> = Min.	2.4		V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 12 mA, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>CC</sub> = Min.		0.5	V
V <sub>IH</sub>	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V <sub>IL</sub>	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V <sub>I</sub>	Input Clamp Voltage	I <sub>IN</sub> = -18 mA, V <sub>CC</sub> = Min.		-1.5	V
I <sub>IH</sub>	Input HIGH Current	V <sub>IN</sub> = 2.4 V, V <sub>CC</sub> = Max. (Note 4)		25	μA
I <sub>IL</sub>	Input LOW Current	V <sub>IN</sub> = 0.4 V, V <sub>CC</sub> = Max. (Note 4)		-250	μA
I <sub>I</sub>	Maximum Input Current	V <sub>IN</sub> = 5.5 V, V <sub>CC</sub> = Max.		1	mA
I <sub>OZH</sub>	Off-State Output Leakage Current HIGH	V <sub>OUT</sub> = 2.4 V, V <sub>CC</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> (Note 4)		100	μA
I <sub>OZL</sub>	Off-State Output Leakage Current LOW	V <sub>OUT</sub> = 0.4 V, V <sub>CC</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> (Note 4)		-100	μA
I <sub>SC</sub>	Output Short-Circuit Current	V <sub>OUT</sub> = 0.5 V, V <sub>CC</sub> = Max. (Note 5)	-30	-130	mA
I <sub>CC</sub>	Supply Current	V <sub>IN</sub> = 0 V, Outputs Open (I <sub>OUT</sub> = 0 mA), V <sub>CC</sub> = Max.		210	mA

**Notes:**

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V<sub>IL</sub> and V<sub>IH</sub> are input conditions of output tests and are not themselves directly tested. V<sub>IL</sub> and V<sub>IH</sub> are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I<sub>IL</sub> and I<sub>OZL</sub> (or I<sub>IH</sub> and I<sub>OZH</sub>).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V<sub>OUT</sub> = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

## SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 1)

Parameter Symbol	Parameter Description		Min.	Max.	Unit
$t_{PD}$	Input or Feedback to Combinatorial Output			30	ns
$t_s$	Setup Time from Input or Feedback to Clock		30		ns
$t_H$	Hold Time		0		ns
$t_{CO}$	Clock to Output or Feedback			20	ns
$t_{WL}$	Clock Width	LOW	20		ns
$t_{WH}$		HIGH	20		ns
$f_{MAX}$	Maximum Frequency (Note 2)	External Feedback	$1/(t_s + t_{CO})$	20	MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	25	MHz
$t_{PZX}$	$\overline{OE}$ to Output Enable (Note 3)			25	ns
$t_{PXZ}$	$\overline{OE}$ to Output Disable (Note 3)			25	ns
$t_{EA}$	Input to Output Enable Using Product Term Control (Note 3)			30	ns
$t_{ER}$	Input to Output Disable Using Product Term Control (Note 3)			30	ns

## Notes:

1. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
2. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

2

**ABSOLUTE MAXIMUM RATINGS**

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-1.5 V to $V_{CC} + 0.5$ V
DC Output or I/O Pin Voltage	-0.5 V to $V_{CC} + 0.5$ V

**OPERATING RANGES**

T-46-19-13

**Commercial (C) Devices**

Ambient Temperature ( $T_A$ )	0°C to +75°C
Operating in Free Air	0°C to +75°C
Supply Voltage ( $V_{CC}$ ) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

**DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified**

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -3.2$ mA, $V_{IN} = V_{IH}$ or $V_{IL}$ , $V_{CC} = \text{Min.}$	2.4		V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 24$ mA, $V_{IN} = V_{IH}$ or $V_{IL}$ , $V_{CC} = \text{Min.}$		0.5	V
$V_{IH}$	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
$V_{IL}$	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
$V_I$	Input Clamp Voltage	$I_{IN} = -18$ mA, $V_{CC} = \text{Min.}$		-1.5	V
$I_{IH}$	Input HIGH Current	$V_{IN} = 2.7$ V, $V_{CC} = \text{Max.}$ (Note 2)		25	$\mu$ A
$I_{IL}$	Input LOW Current	$V_{IN} = 0.4$ V, $V_{CC} = \text{Max.}$ (Note 2)		-250	$\mu$ A
$I_I$	Maximum Input Current	$V_{IN} = 5.5$ V, $V_{CC} = \text{Max.}$		100	$\mu$ A
$I_{OZH}$	Off-State Output Leakage Current HIGH	$V_{OUT} = 2.7$ V, $V_{CC} = \text{Max.}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 2)		100	$\mu$ A
$I_{OLZ}$	Off-State Output Leakage Current LOW	$V_{OUT} = 0.4$ V, $V_{CC} = \text{Max.}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 2)		-100	$\mu$ A
$I_{SC}$	Output Short-Circuit Current	$V_{OUT} = 0.5$ V, $V_{CC} = \text{Max.}$ (Note 3)	-30	-130	mA
$I_{CC}$	Supply Current	$V_{IN} = 0$ V, Outputs Open ( $I_{OUT} = 0$ mA), $V_{CC} = \text{Max.}$		105	mA

**Notes:**

- These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
- I/O pin leakage is the worst case of  $I_{IL}$  and  $I_{OLZ}$  (or  $I_{IH}$  and  $I_{OZH}$ ).
- Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second.  $V_{OUT} = 0.5$  V has been chosen to avoid test problems caused by tester ground degradation.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description		T-46-19-13		Min.	Max.	Unit	
t <sub>PD</sub>	Input or Feedback to Combinatorial Output		20L8, 20R6 20R4			35	ns	
t <sub>s</sub>	Setup Time from Input or Feedback to Clock		20R8, 20R6 20R4		35		ns	
t <sub>H</sub>	Hold Time				0		ns	
t <sub>CO</sub>	Clock to Output or Feedback					25	ns	
t <sub>wL</sub>	Clock Width	LOW				25	ns	
t <sub>wH</sub>		HIGH				25	ns	
f <sub>MAX</sub>	Maximum Frequency (Note 2)	External Feedback			1/(t <sub>s</sub> + t <sub>CO</sub> )	16		MHz
		No Feedback			1/(t <sub>wH</sub> + t <sub>wL</sub> )	20		MHz
t <sub>PZx</sub>	$\overline{OE}$ to Output Enable					25	ns	
t <sub>pxz</sub>	$\overline{OE}$ to Output Disable					25	ns	
t <sub>EA</sub>	Input to Output Enable Using Product Term Control		20L8, 20R6			35	ns	
t <sub>ER</sub>	Input to Output Disable Using Product Term Control		20R4			35	ns	

Notes:

1. See Switching Test Circuit for test conditions.
2. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

FOR CMOS  
PALCE20V8



**ABSOLUTE MAXIMUM RATINGS**

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-1.5 V to +5.5 V
DC Output or I/O Pin Voltage	5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

**OPERATING RANGES**

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<b>Military (M) Devices (Note 1)</b>	
Ambient Temperature (T <sub>A</sub> )	-55°C to +125°C
Operating in Free Air	-55°C to +125°C
Supply Voltage (V <sub>CC</sub> ) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

**Note:**

1. Military products are tested at T<sub>C</sub> = +25°C, +125°C, and -55°C per MIL-STD-883.

**DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)**

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -2 mA, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>CC</sub> = Min.	2.4		V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 12 mA, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>CC</sub> = Min.		0.5	V
V <sub>IH</sub>	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V <sub>IL</sub>	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V <sub>I</sub>	Input Clamp Voltage	I <sub>IN</sub> = -18 mA, V <sub>CC</sub> = Min.		-1.5	V
I <sub>IH</sub>	Input HIGH Current	V <sub>IN</sub> = 2.4 V, V <sub>CC</sub> = Max. (Note 4)		25	μA
I <sub>IL</sub>	Input LOW Current	V <sub>IN</sub> = 0.4 V, V <sub>CC</sub> = Max. (Note 4)		-250	μA
I <sub>I</sub>	Maximum Input Current	V <sub>IN</sub> = 5.5 V, V <sub>CC</sub> = Max.		1	mA
I <sub>ozH</sub>	Off-State Output Leakage Current HIGH	V <sub>OUT</sub> = 2.4 V, V <sub>CC</sub> = Max. V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> (Note 4)		100	μA
I <sub>ozL</sub>	Off-State Output Leakage Current LOW	V <sub>OUT</sub> = 0.4 V, V <sub>CC</sub> = Max. V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> (Note 4)		-100	μA
I <sub>sc</sub>	Output Short-Circuit Current	V <sub>OUT</sub> = 0.5 V, V <sub>CC</sub> = Max. (Note 5)	-30	-130	mA
I <sub>cc</sub>	Supply Current	V <sub>IN</sub> = 0 V, Outputs Open (I <sub>OUT</sub> = 0 mA) V <sub>CC</sub> = Max.		105	mA

**Notes:**

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V<sub>IL</sub> and V<sub>IH</sub> are input conditions of output tests and are not themselves directly tested. V<sub>IL</sub> and V<sub>IH</sub> are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I<sub>IL</sub> and I<sub>ozL</sub> (or I<sub>IH</sub> and I<sub>ozH</sub>).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V<sub>OUT</sub> = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

## SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 1)

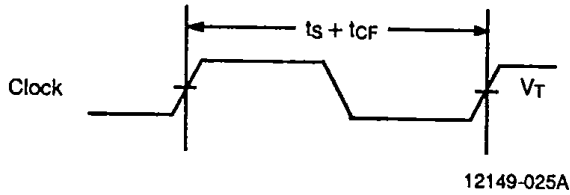
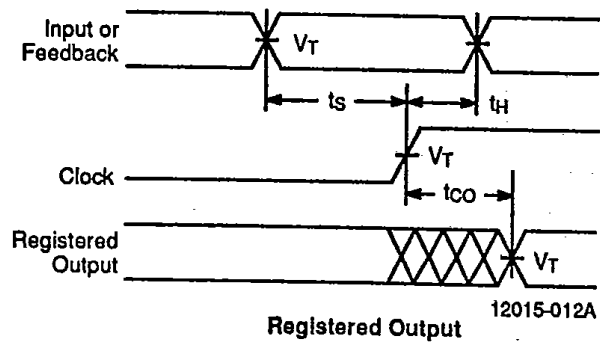
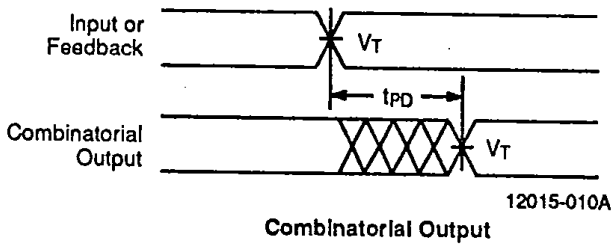
Parameter Symbol	Parameter Description		Min.	Max.	Unit
$t_{PD}$	Input or Feedback to Combinatorial Output			50	ns
$t_s$	Setup Time from Input or Feedback to Clock		50		ns
$t_H$	Hold Time		0		ns
$t_{CO}$	Clock to Output or Feedback			25	ns
$t_{WL}$	Clock Width	LOW	25		ns
$t_{WH}$		HIGH	25		ns
$f_{MAX}$	Maximum Frequency (Note 2)	External Feedback	$1/(t_s + t_{CO})$	13.3	MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	20	MHz
$t_{PZX}$	$\overline{OE}$ to Output Enable (Note 3)			25	ns
$t_{PXZ}$	$\overline{OE}$ to Output Disable (Note 3)			25	ns
$t_{EA}$	Input to Output Enable Using Product Term Control (Note 3)			45	ns
$t_{ER}$	Input to Output Disable Using Product Term Control (Note 3)			45	ns

## Notes:

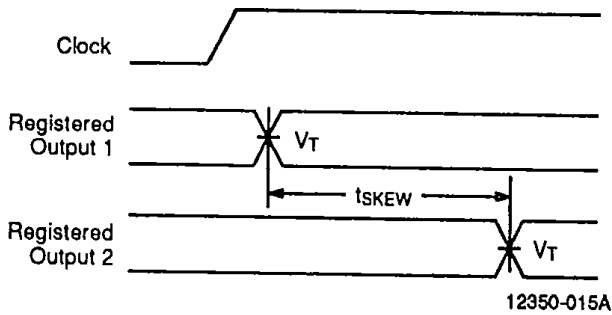
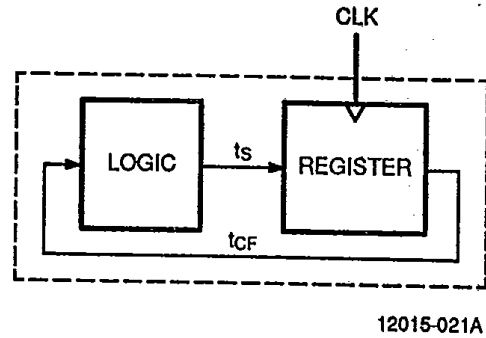
- See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
- These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
- These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

# SWITCHING WAVEFORMS

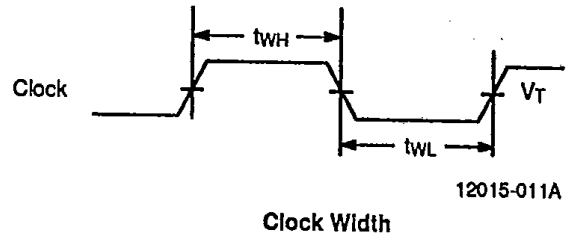
T-46-19-13



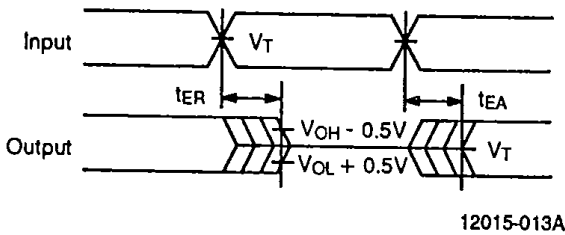
**Clock to Feedback ( $f_{MAX}$  Internal)**  
See Path at Right



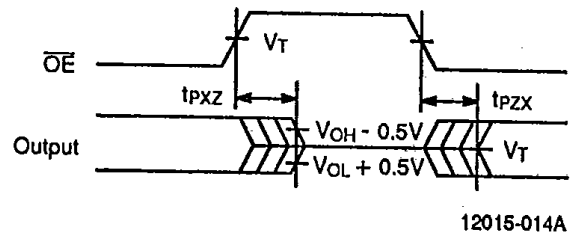
**Registered Output Skew for Outputs Switching in the Same Direction**



**Clock Width**



**Input to Output Disable/Enable**

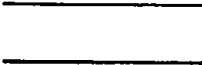



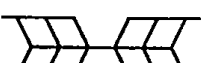


**$\overline{OE}$  to Output Disable/Enable**

**Notes:**

1.  $V_T = 1.5\text{ V}$
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2-5 ns typical.  
(2-4 ns for -7 (-12 Mil) and -10 (-15 Mil) Series)

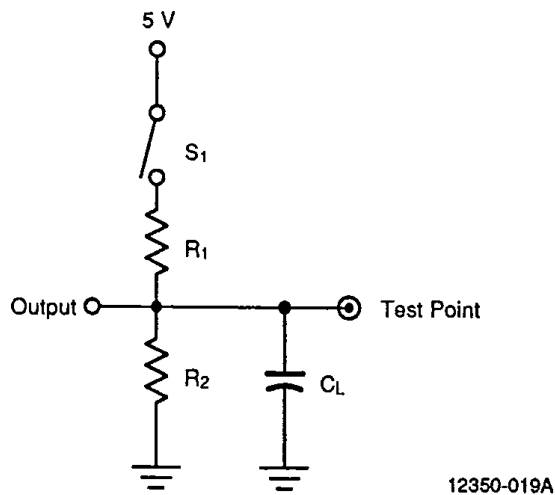


WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State



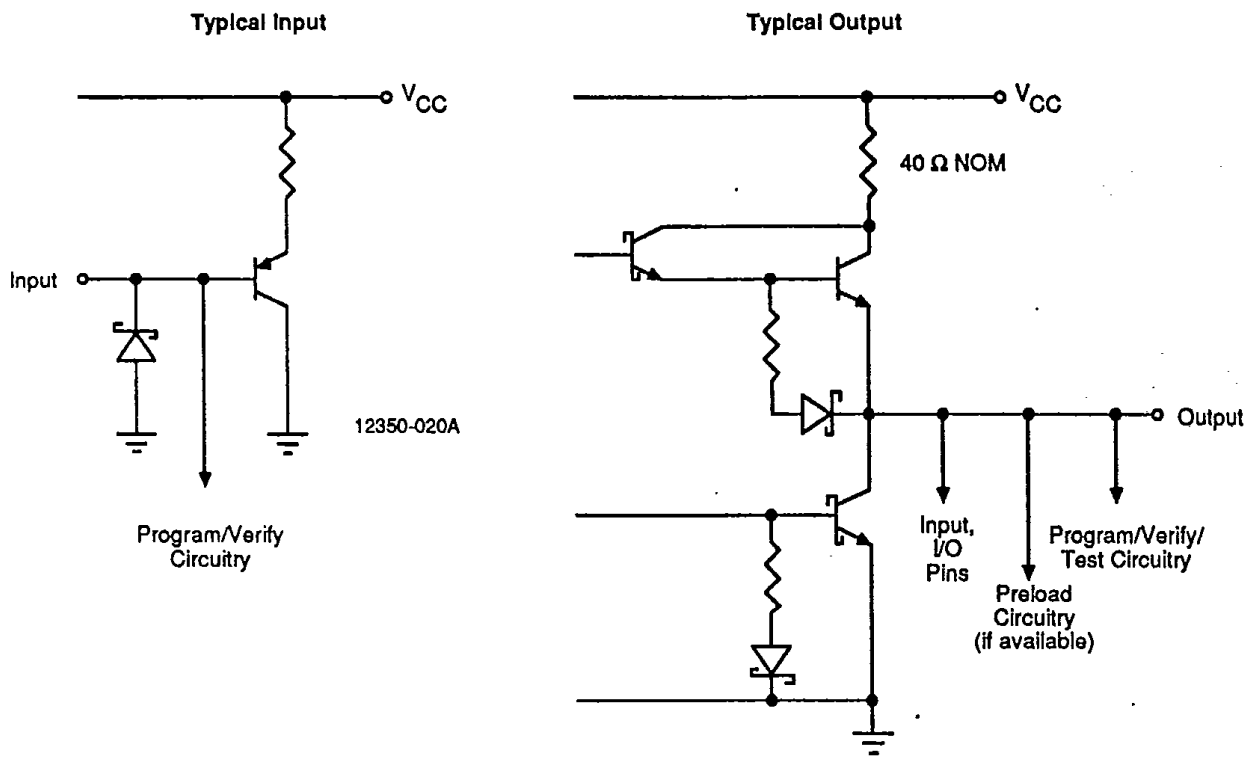
KS000010-PAL

SWITCHING TEST CIRCUIT



Specification	S <sub>1</sub>	C <sub>L</sub>	Commercial		Military		Measured Output Value
			R <sub>1</sub>	R <sub>2</sub>	R <sub>1</sub>	R <sub>2</sub>	
t <sub>PD</sub> , t <sub>CO</sub> , t <sub>CF</sub>	Closed	50 pF	200 Ω	390 Ω	390 Ω	750 Ω	1.5 V
t <sub>PZX</sub> , t <sub>EA</sub>	Z → H: Open Z → L: Closed						1.5 V
t <sub>PXZ</sub> , t <sub>ER</sub>	H → Z: Open L → Z: Closed	5 pF					H → Z: V <sub>OH</sub> - 0.5 V L → Z: V <sub>OL</sub> + 0.5 V

## INPUT/OUTPUT EQUIVALENT SCHEMATICS



**OUTPUT REGISTER PRELOAD****Applies to -7 (-12 Mil) Series Only**

The preload function allows the register to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for preloading follows.

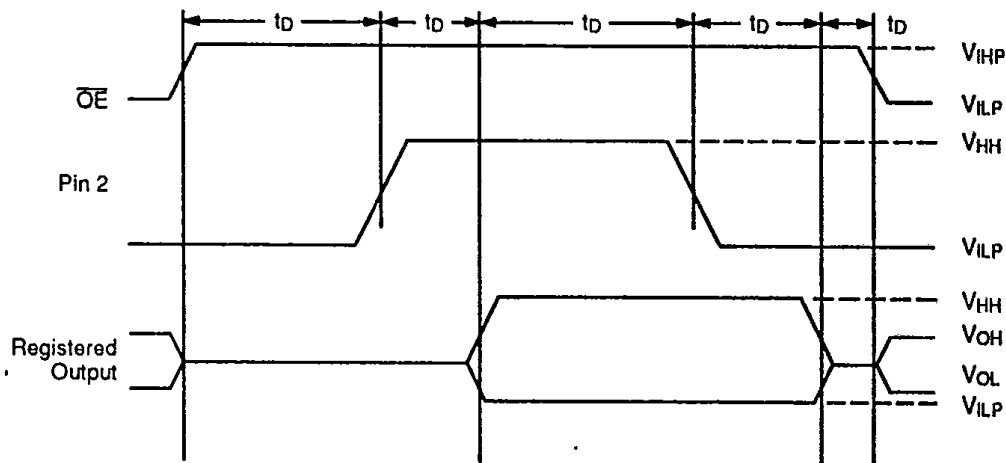
1. Raise  $V_{CC}$  to  $V_{CCH}$ .
2. Set  $\overline{OE}$  to  $V_{IHP}$  to disable output registers.
3. Raise pin 2 to  $V_{HH}$  to enter preload mode.
4. Apply either  $V_{HH}$  or  $V_{ILP}$  to all registered outputs. Use  $V_{HH}$  to preload a LOW in the flip-flop; use  $V_{ILP}$  to

preload a HIGH in the flip-flop. Leave combinatorial outputs floating.

5. Lower pin 2 to  $V_{ILP}$ .
6. Remove  $V_{ILP}/V_{HH}$  from all registered output pins.
7. Lower  $\overline{OE}$  to  $V_{ILP}$  to enable the output registers.
8. Verify  $V_{OL}/V_{OH}$  at all registered output pins. Note that because of the output inverter, a register that has been preloaded HIGH will provide a LOW at the output.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
$V_{HH}$	Super-level input voltage	10	11	12	V
$V_{ILP}$	Low-level input voltage	0	0	0.5	V
$V_{IHP}$	High-level input voltage	2.4	5.0	5.5	V
$V_{CCH}$	Power supply during preload	5.4	5.7	6.0	V
$t_D$	Delay time	100	200	1000	ns

2



10294-003A

Output Register Preload Waveform

**OUTPUT REGISTER PRELOAD****Applies to -10 (-15 MII) Series Only**

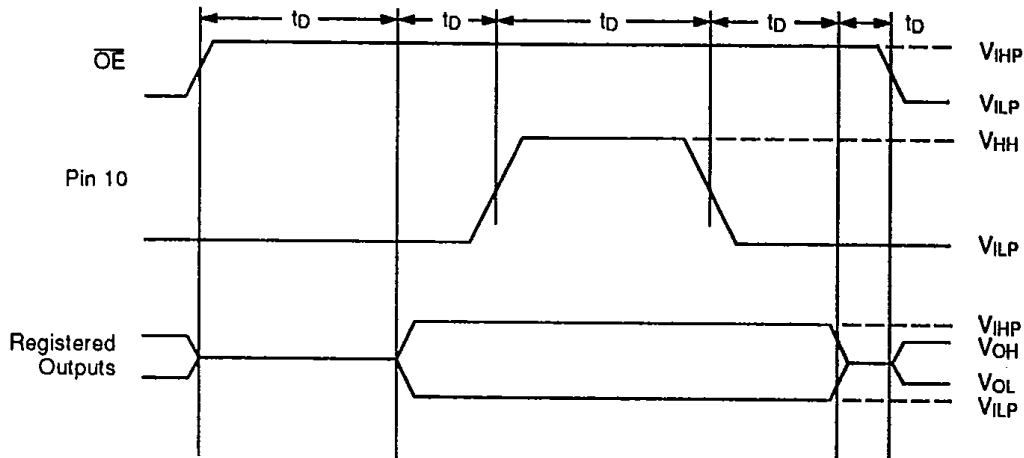
The preload function allows the register to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for preloading follows.

1. Raise  $V_{CC}$  to 4.5 V.
2. Set  $\overline{OE}$  to  $V_{IHP}$  to disable output registers.
3. Apply either  $V_{IHP}$  or  $V_{ILP}$  to all registered outputs. Use  $V_{IHP}$  to preload a HIGH in the flip-flop; use  $V_{ILP}$  to

preload a LOW in the flip-flop. Leave combinatorial outputs floating.

4. Pulse pin 10 to  $V_{HH}$ , then back to 0 V.
5. Remove  $V_{ILP}/V_{IHP}$  from all registered output pins.
6. Lower  $\overline{OE}$  to  $V_{ILP}$  to enable the output registers.
7. Verify  $V_{OL}/V_{OH}$  at all registered output pins. Note that because of the output inverter, a register that has been preloaded HIGH will provide a LOW at the output.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
$V_{HH}$	Super-level input voltage	19	20	21	V
$V_{ILP}$	Low-level input voltage	0	0	0.5	V
$V_{IHP}$	High-level input voltage	2.4	5.0	5.5	V
$t_D$	Delay time	100	200	1000	ns



10294-004A

Output Register Preload Waveform

## POWER-UP RESET

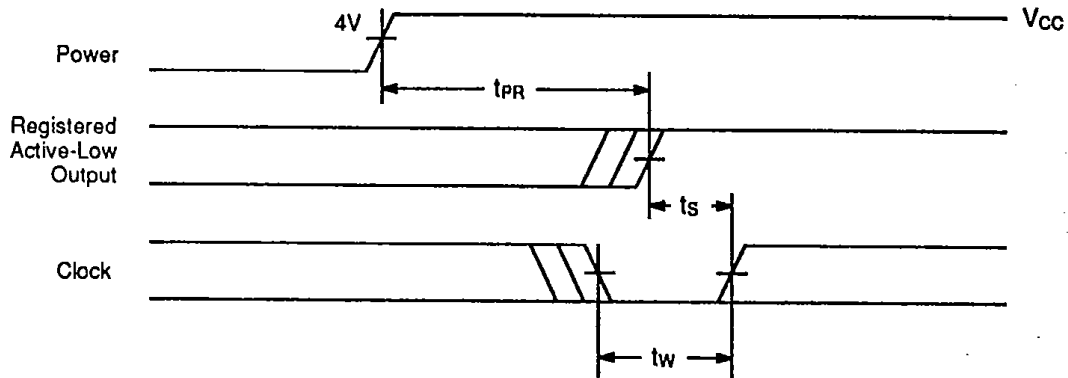
T-46-19-13

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will be HIGH due to the inverting output buffer. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways  $V_{CC}$

can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The  $V_{CC}$  rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max.	Unit
$t_{PR}$	Power-up Reset Time	1000	ns
$t_s$	Input or Feedback Setup Time	See Switching Characteristics	
$t_{wL}$	Clock Width LOW		



12350-024A

Power-Up Reset Waveform